MROD-Out PCB Options

JTAG over S-LINK URL or RS485 electrical.

By default the S-LINK return lines are used as JTAG interface. Three of the four return lines need to be used for TCK, TMS and TDI. Note that the TDO bit is received in the separator word of the MROD-In.
When Jumper J13 (respectively J23, J33, J43, J53 and J63 for each MROD-In input channel) is closed then electrical JTAG over RS485 option is selected. Have a look at figure 1 to find out where these jumpers are located on the board. Table 1 shows the definition of the URL lines in this case. By default the URL lines on the MROD-In FPGA are outputs. Because URL3 is an input for the FPGA, the FPGA needs to be refitted. In any case, there is no danger for contention on the URL3 line because a safety resistor is placed between the RS485 output and the FPGA pin.
Note that the URL lines are still connected to the S-LINK.
Note also that TDI is defined as the output, and TDO as input.

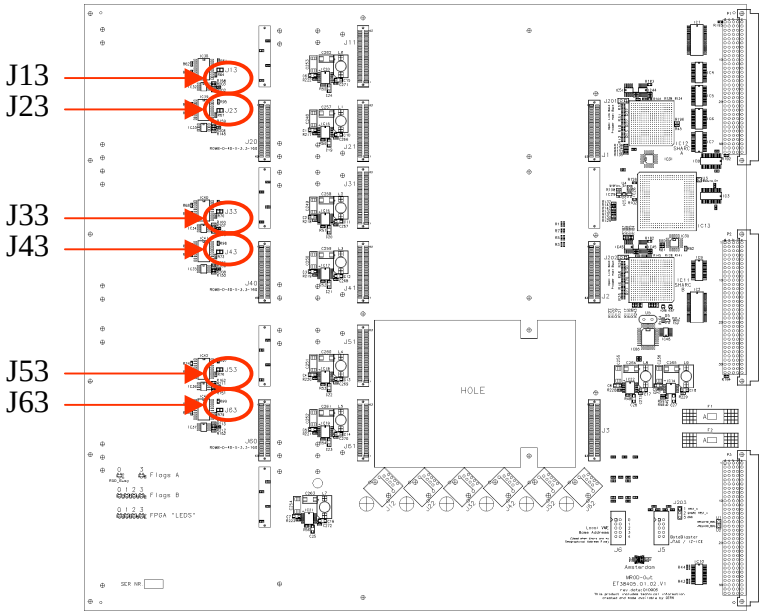

Figure 1: RS485 Jumper locations.

URL	Direction (as seen by MROD-In)	Function
0	Output	TCK
1	Output	TDI
2	Output	TMS
3	Input	TDO

Table 1: Definition of the JTAG lines when using the RS485 option.

BootBoard

The BootBoard may be placed on J4 to make it possible to boot SHARC A or SHARC B via Link 4.
It is also possible to place the BootBoard on J1, J2 or J3 whenever one or more of the MROD-In boards is missing. All four routed SHARC link ports to the neighbouring MROD-Ins and/or the MROD-Out SHARCs are then available via connectors on the BootBoard.

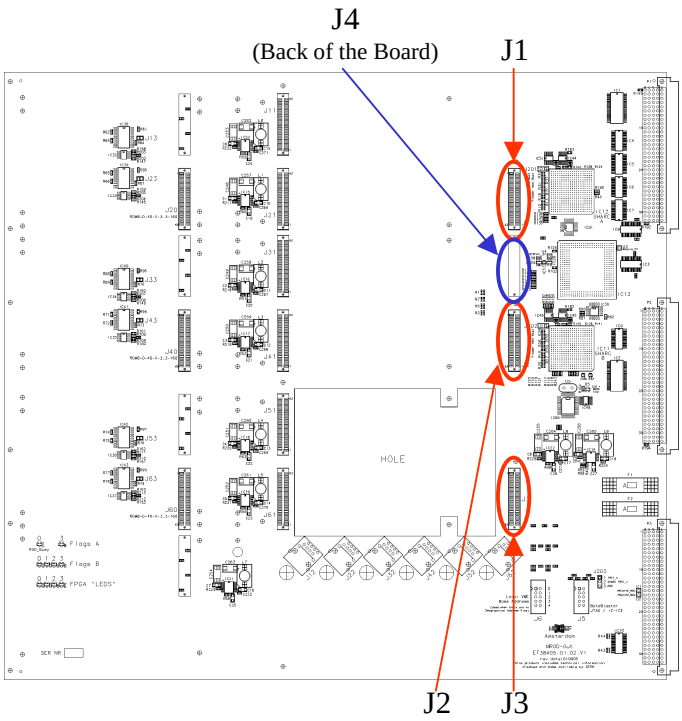

Figure 2: BootBoard can be placed on J1, J2, J3 and J4.

Single or Multiple SHARC(s)

The MROD-Out is made to support two SHARCs (A and B) in a cluster. SHARC A has its ID fixed on ‘001’, SHARC B has its ID fixed on ‘010’.
When two SHARCs are mounted then the pull-up resistors on the BR1_n and BR2_n signals (R142 and R143, see figure 3) should not be placed because they are used by both SHARCs for bus arbitration.
In a Single processor system all BR#_n lines should be pulled up.
Table 2 lists the options.

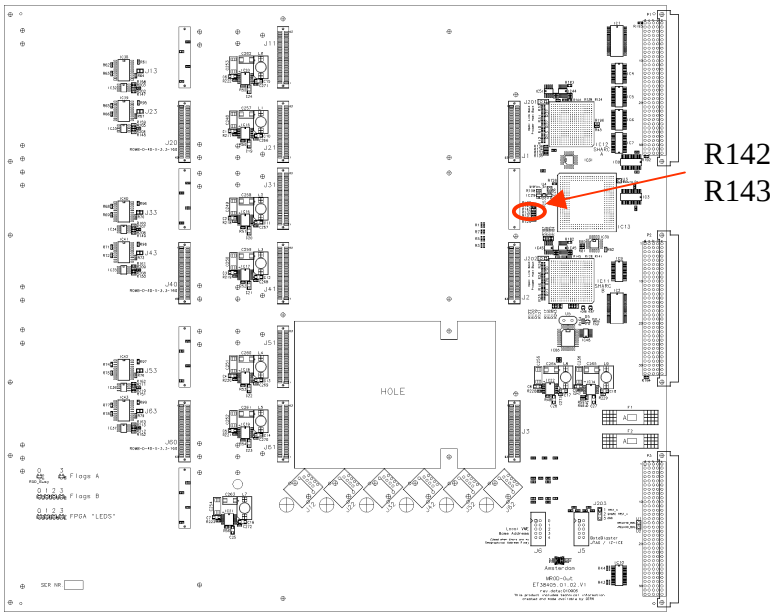

Figure 3: Locations of R142 and R143

Option	SHARCs to be mounted	BR2_n and BR1_n Pull-Up resistors
Single Processor	A only	Place R142 and R143
Multi Processor	A and B	Do **not** Place R142, R143

Table 2: Single, Multi Processor options.

SHARC Bus Arbitration Priority

Either fixed priority (SHARC A has priority over SHARC B) or rotating priority can be selected. The MROD-Out PCB is assembled for fixed priority by default.
When rotating priority should be selected R242 should be removed and R241 should be replaced by a 0 ohm resistor (see figure 4).

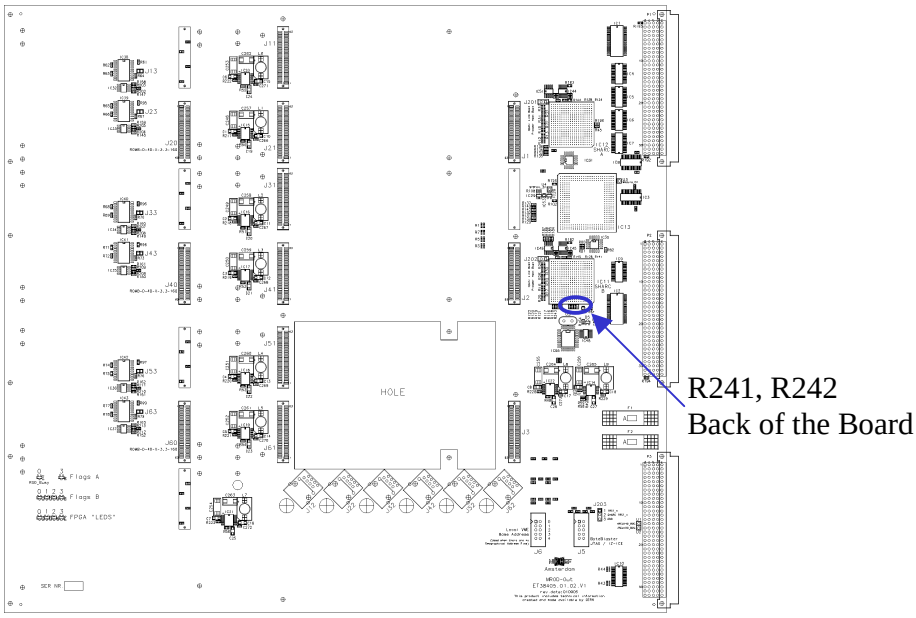

Figure 4: Locations of R241 and R242

VME64(x) Base Address Register (BAR)

LocalBAR jumper J6 (see figure 5) defines the Base Address Register when the module is put into a VME or VME64 back plane. This is detected because the geographical address pins in such crates are open.

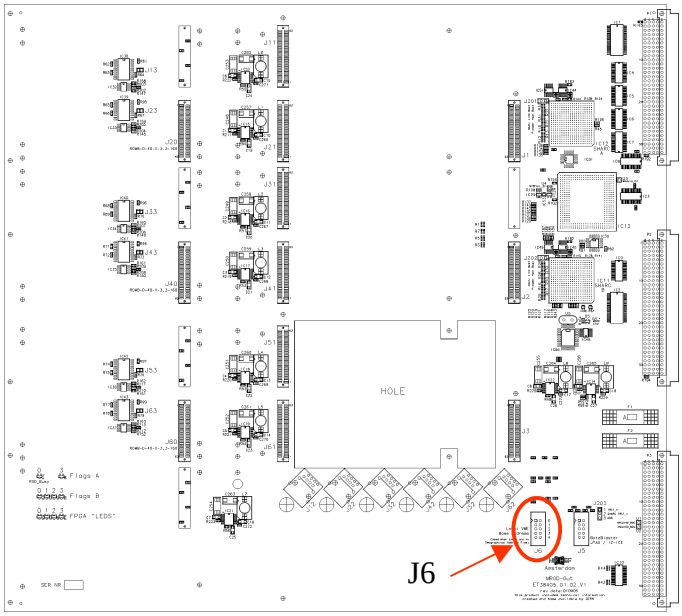

Figure 5: Locations of LocalBAR jumper J6

This means they will be pulled high on the board so the slot number will be zero with a parity error (VME64x, Observation 3.6). When this is the case, BAR[7..3] is loaded with the value of a LocalBAR jumper J6.

Use internal XTAL or TIM CLK40

For proper communication of with the TTC system (via the TIM and over P3 back plane), the system clock for the MROD-Out needs to be the TIM distributed 40 MHz clock. Whenever this clock is detected on the P3 back plane, this clock is used as system clock. When there is no distributed 40 MHz clock detected (no TIM in the system), then automatically a XTAL on the board is activated and generated the system clock. When the XTAL is generating the system clock, then the Yellow ‘MROD XTAL’ LED light up (see figure 6).

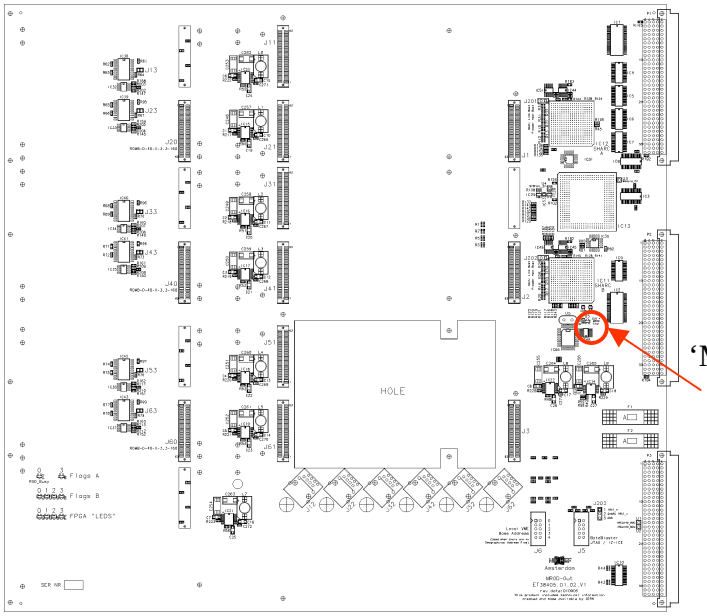

Figure 6: Location of the Yellow ‘MROD XTAL’ LED

JTAG Chain

The JTAG chain on the MROD-Out includes 4 devices as listed in table 3:

JTAG no	Device	Device Function	Download File
1	EPC2	Configuration device for FPGA	FPGA.POF
2	EP20K100EBC356-1x	FPGA	FPGA.SOF
3	ADSP-21160	SHARC A	
4	ADSP-21160	SHARC B	

Table 3: JTAG Chain

ByteBlaster connector J5

Connector J5 is used to connect the ByteBlaster to the MROD_Out. By default, the ByteBlaster doesn't drive the TRST_n line so the TRST_n signal is de-asserted (pulled '1' by a pull-up resistor). This should be the case in order to program the EPC2 and/or the FPGA devices.
The ADSP-21160 (SHARC) datasheet states however that "TRST_n must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21160".
This is a conflicting situation.
To satisfy the rule for the SHARC described above, the TRST_n line of both SHARCs is connected to GND by placing a jumper over pin 2 and 3 of J203 (see figure 7).
Note that according to the JTAG standard (IEEE Std 1149.1), TRST_n is optional. The TAP controller can always be put into the "Test-Logic-Rest" state by holding TMS high while at least five rising-edged are applied to TCK.
Pin 2 of the ByteBlaster connector is not used and is left unconnected by the ByteBlaster itself.

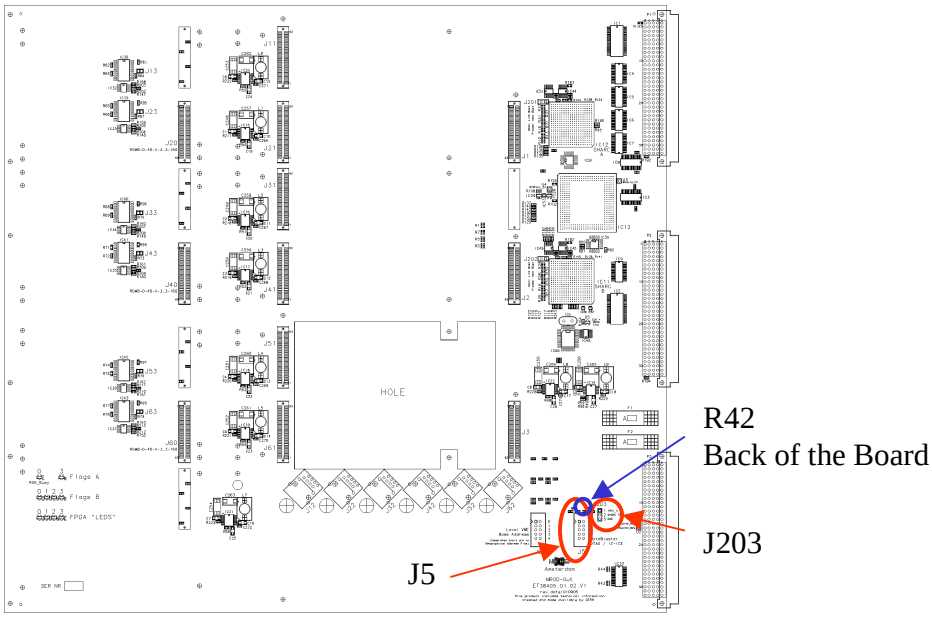

Figure 7: Location of J5, J203 and R42

EZ-ICE

When the EZ-ICE is used for simulation of the SHARC it might be necessary to drive TRST_n. If so, place the jumper over pin 1 and 2 of J203 (see figure 7). This will connect the TRST_n signal from the J5 connector to SHARC_TRST_n signal. Note that the SHARC might not function properly after power-up when J5 is left open (See ByteBlaster connector J5 above). Make sure an EZ-ICE connector is put into J5, which is driving TRST_n in a proper way.
The EMU_n signal of the SHARC is available on pin 2 of J5 (which is not used by the ByteBlaster). When 0 ohm resistor R42 (see figure 7) is removed, pin 2 of J5 is left unconnected on the MROD-Out board.
Make sure that the EZ-ICE connector fits J5!

SHARC Booting

By default both SHARCs are configured for Link Booting.
Both SHARCs can be accessed through VME so the DMA controllers used for booting can be initialised under software control. This means that it should be possible to select Link Booting or Host Booting through VME accesses.
When Host Booting should be selected by default, then close jumper J201 to select Host Booting for SHARC A, and close jumper J202 to select Host Booting for SHARC B.
See figure 8 for the locations of jumper J201 and J202.

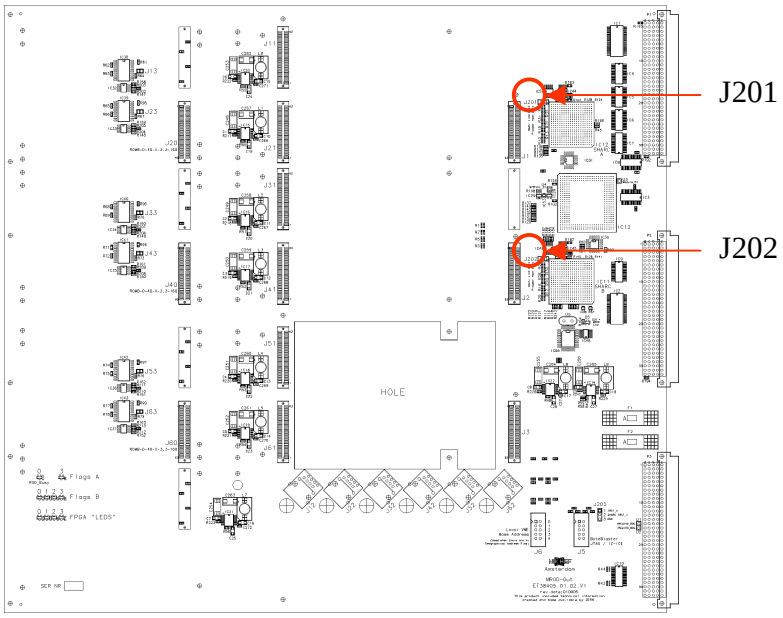

Figure 8: Location of J201 and J202