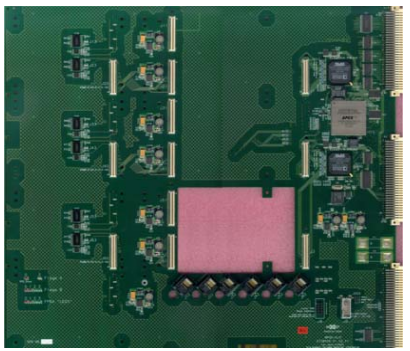
MROD-1 Hardware Overview

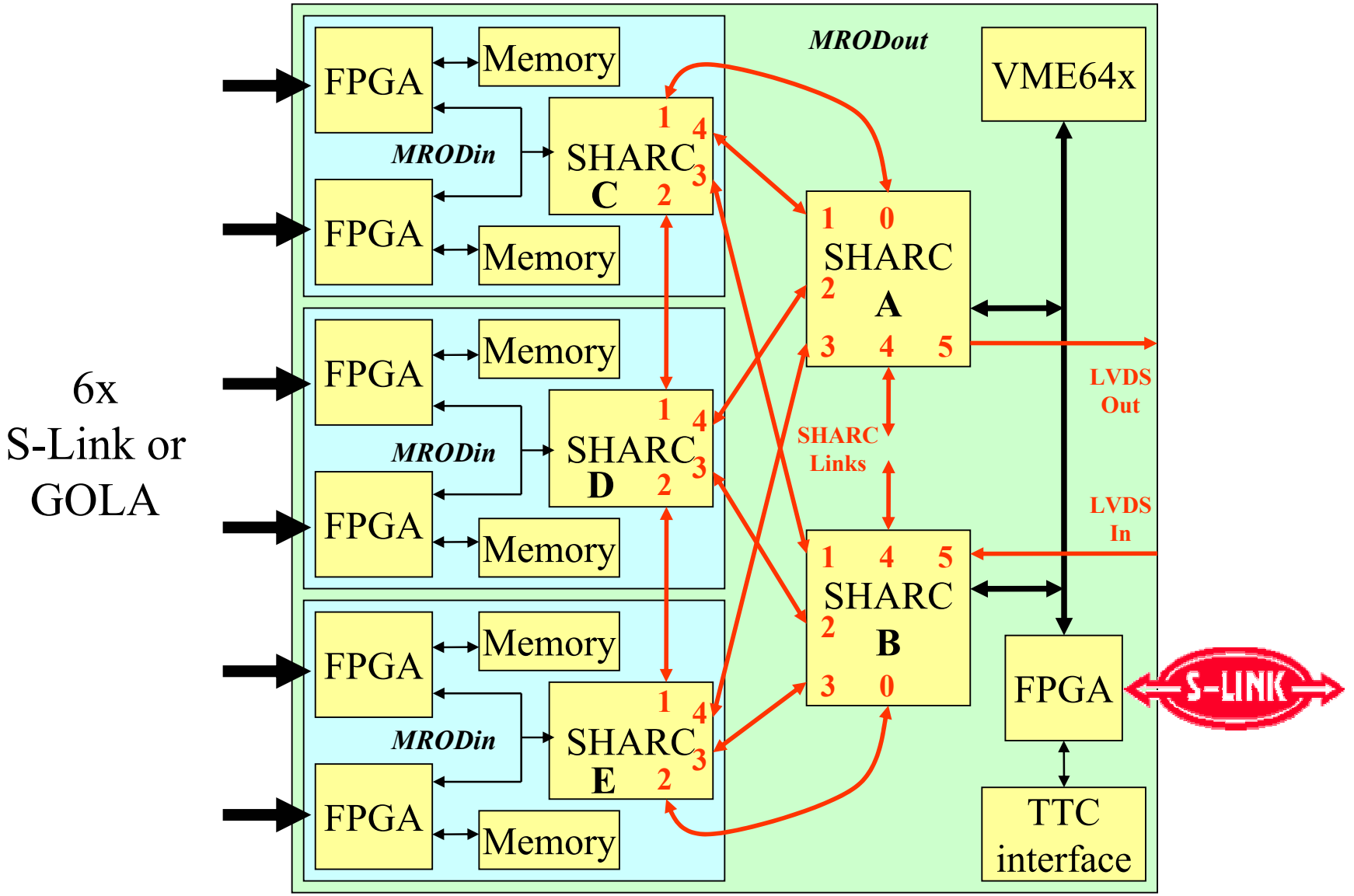
- MRODin

- MRODout



- MROD-1 = 3 x MRODin + 1 x MRODout

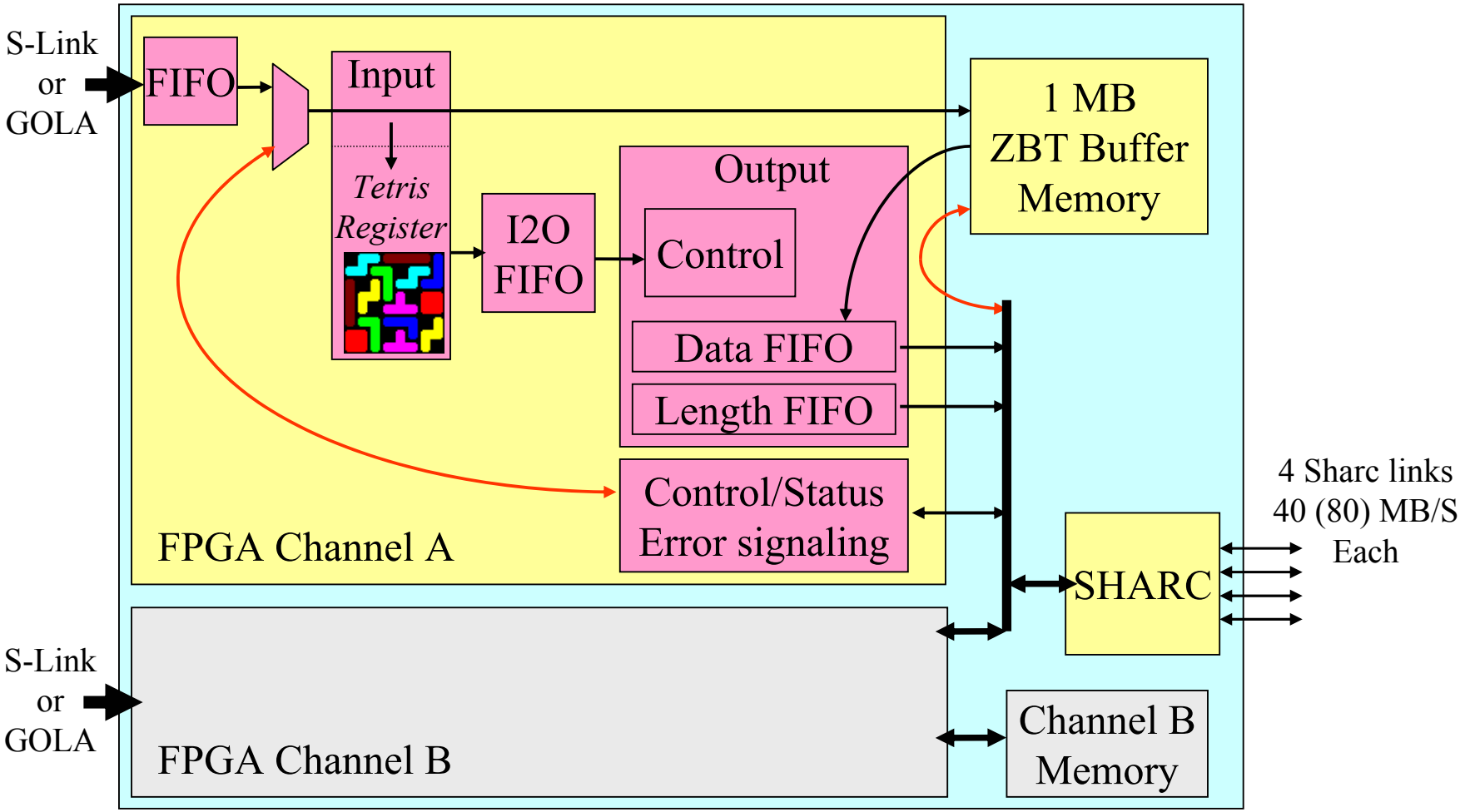
MROD-1 Hardware Overview



MRODin

- Buffer memory, Separate partition per TDC, Dataflow into the buffer memory
- Tetris register, I2O-FIFO, Fault tolerance, Error signaling and handling , Resynchronization
- Dataflow out of buffer memory, DMA, Zero suppression, Length FIFO
- Data format, TDC-ID, Parity errors
- Interrupt sources
- FPGA registers

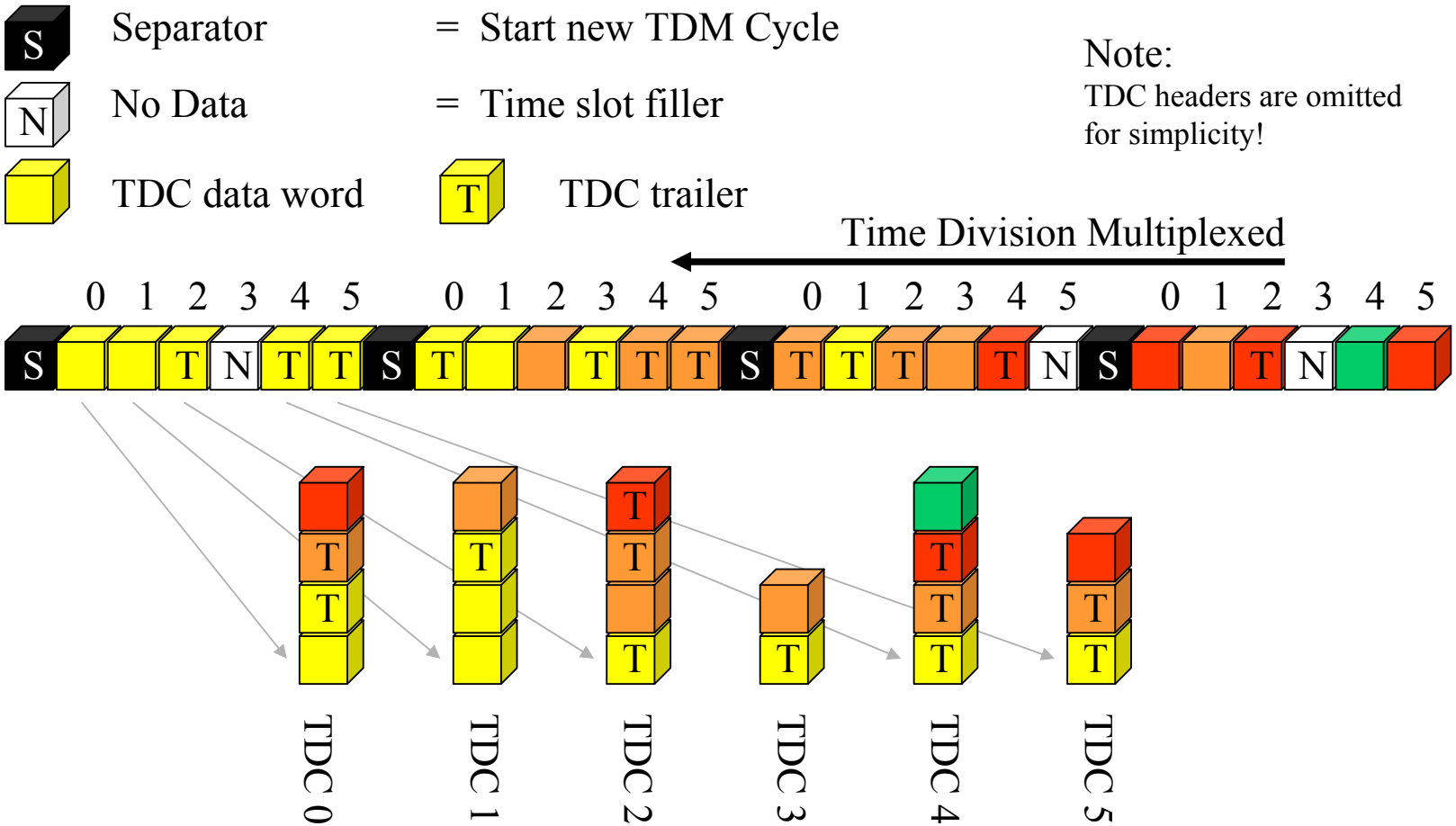
MRODin Overview



MDT Readout chain wooden model

Buffer Memory Partitions

Dataflow into buffer memory

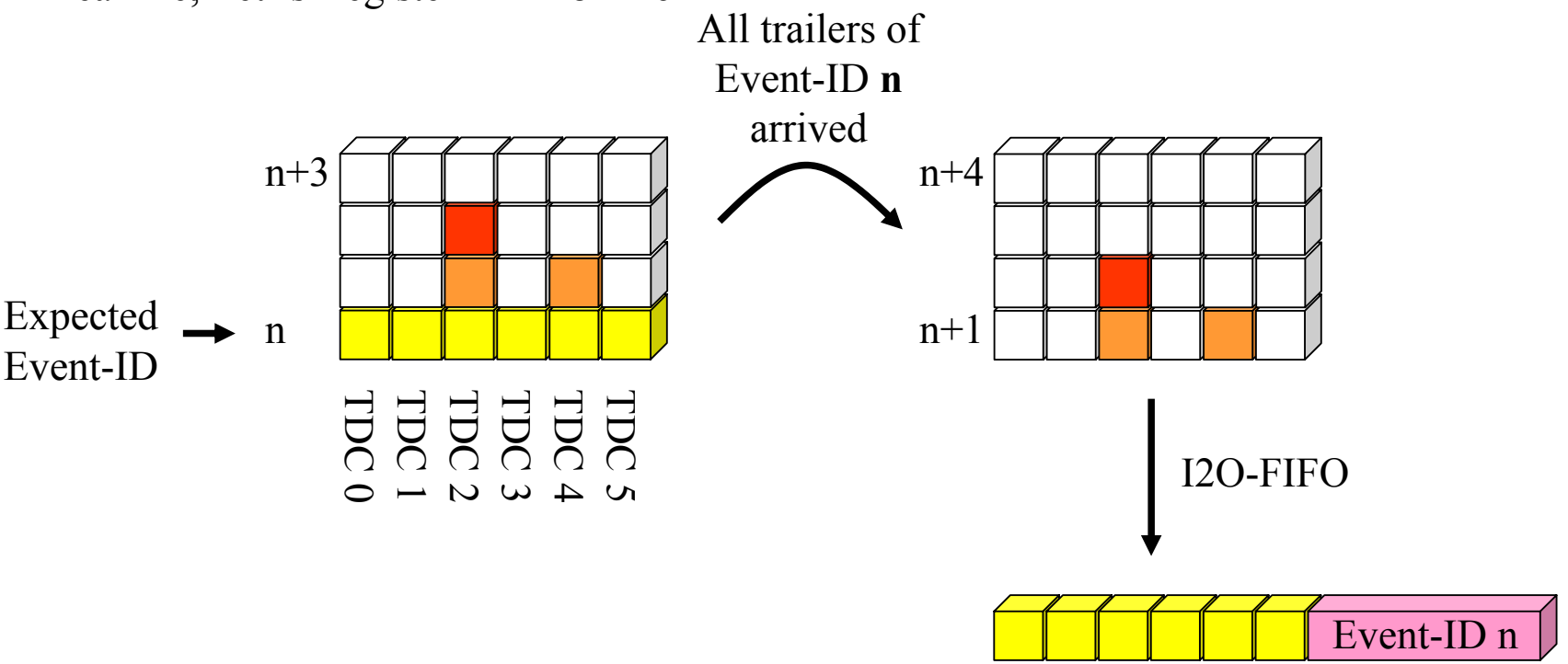


In real life: 18 Buffer Memory Partitions (8 K words each)

Tetris Register

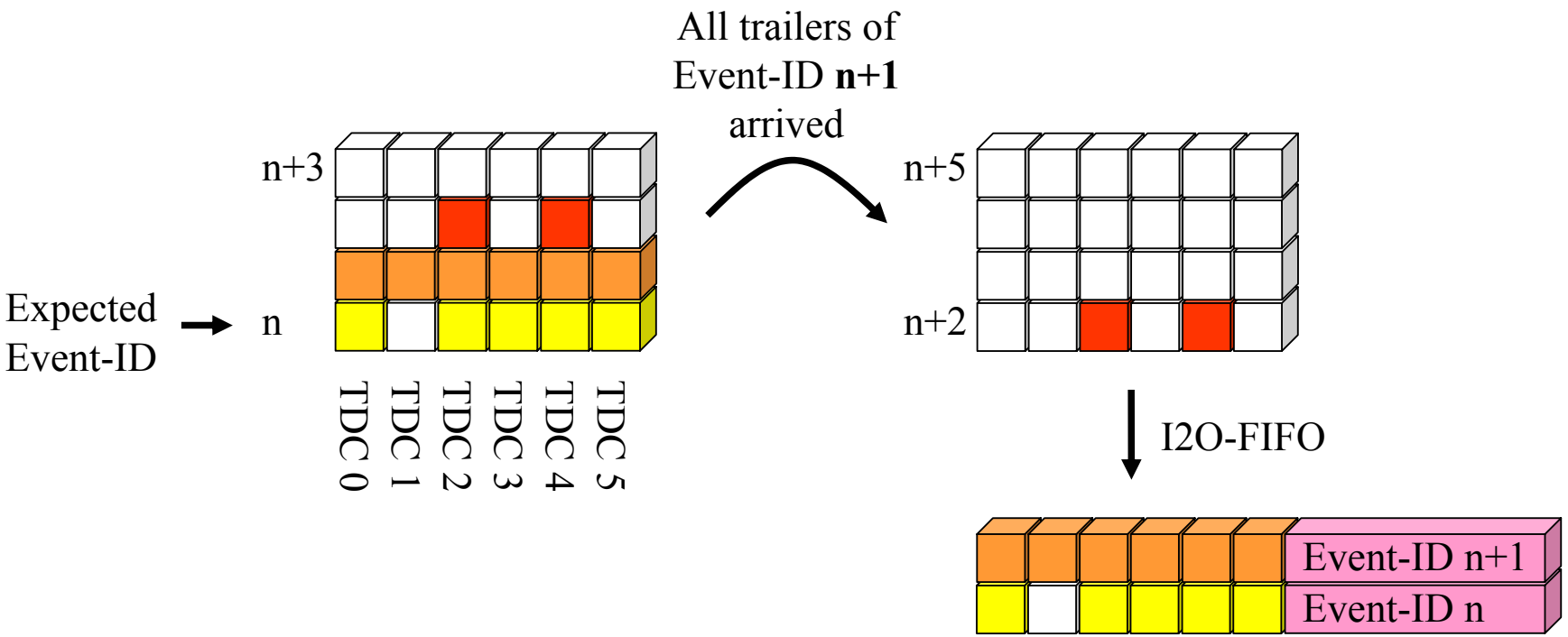
Normal operation

Example Tetris Register = 6 x 4
In real life, Tetris Register = 18 x 16



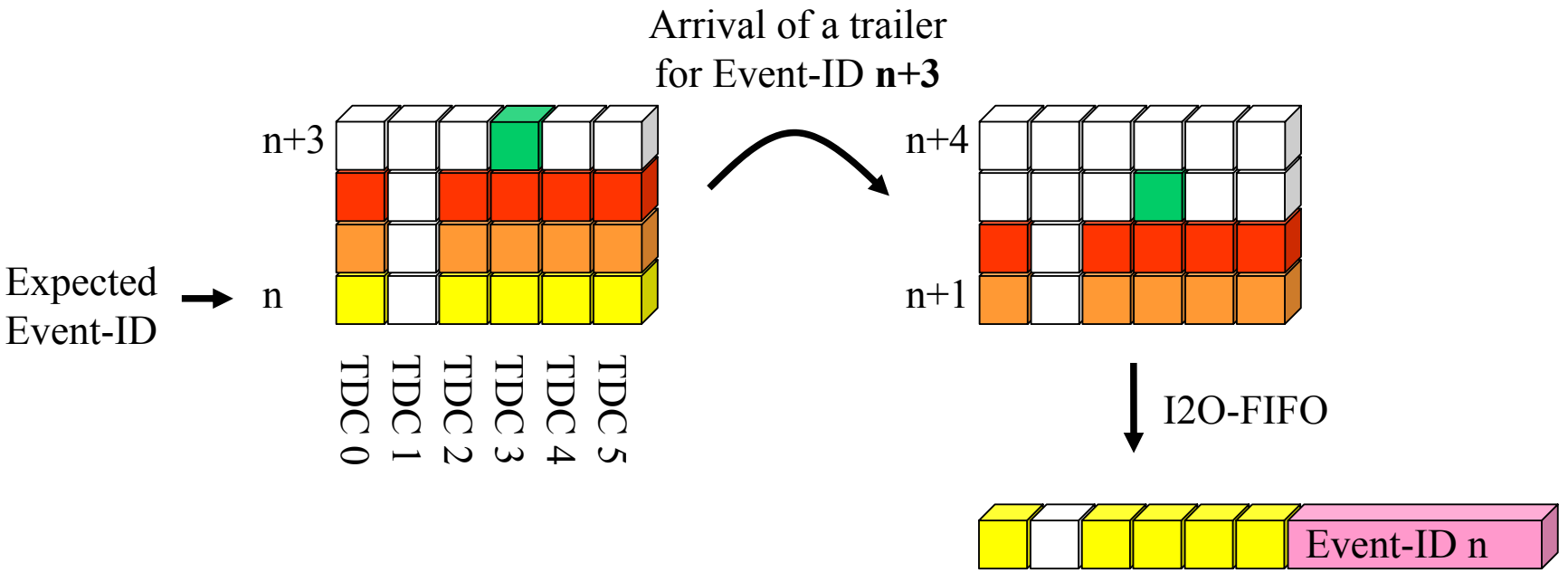
Tetris Register

TDC trailer missed



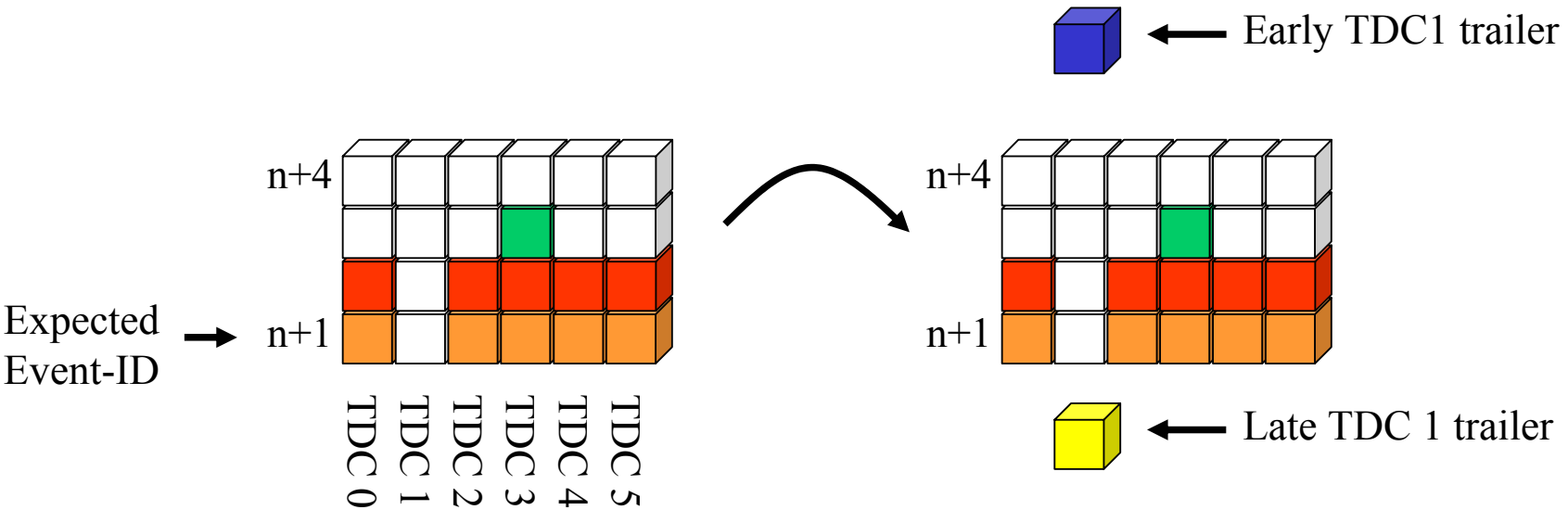
Tetris Register

Notorious absence of TDC (panic mode)



Tetris Register

Early / Late

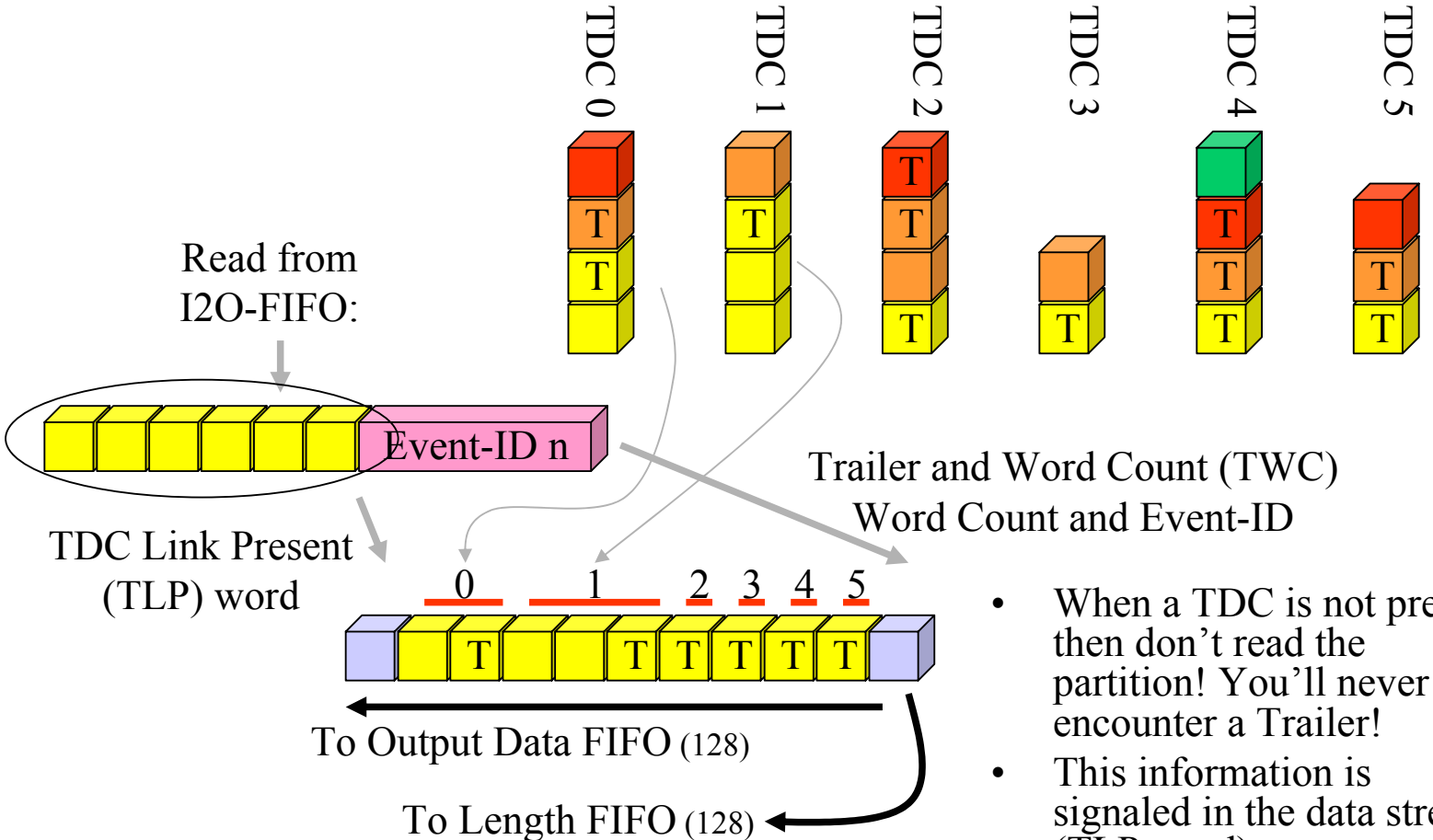


Notes:

- Expected Event-ID can be set by the SHARC during MRODin initialization
- Expected Event-ID is hardware updated
- Resynchronization for an MRODin channel should be possible.

Buffer Memory Partitions

Dataflow out of buffer memory



- When a TDC is not present then don't read the partition! You'll never encounter a Trailer!
- This information is signaled in the data stream (TLP word)

Dataflow out of buffer memory
Continued

- Output Data FIFO is read with continuous DMA by the SHARC
- Length FIFO provides event summary
- While reading TDC data from buffer memory, data can be zero suppressed
  (i.e. TDC header immediately followed by TDC trailer)

Data Format:
TDC-ID in TDC Header word

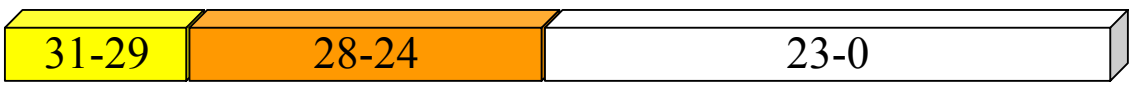
TDC-ID (4-bit)

Upper Nibble = TDC data type

0x1010 TDC Header

0x1011 End Of TDC Group (used by AMT-1; **Not used** by AMT-2/3 chip)

When the MRODin encounters a TDC Header, it reformats the TDC-ID bits:



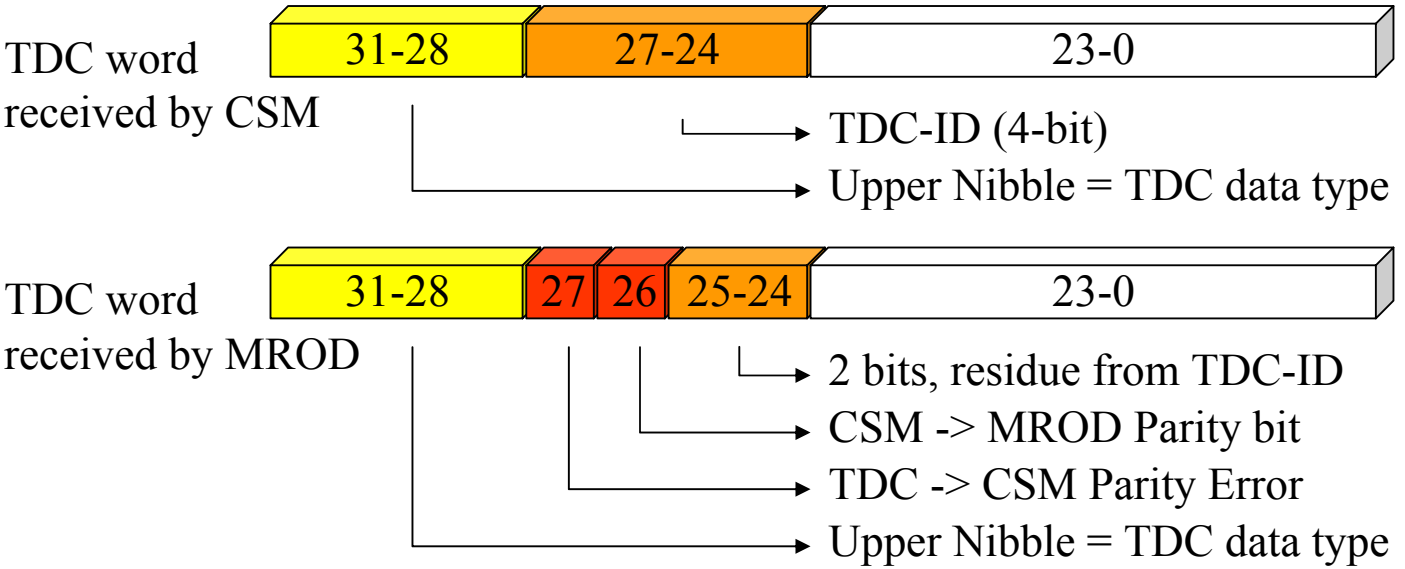
5-bit TDC-ID based on TDM time slot

TDC Header

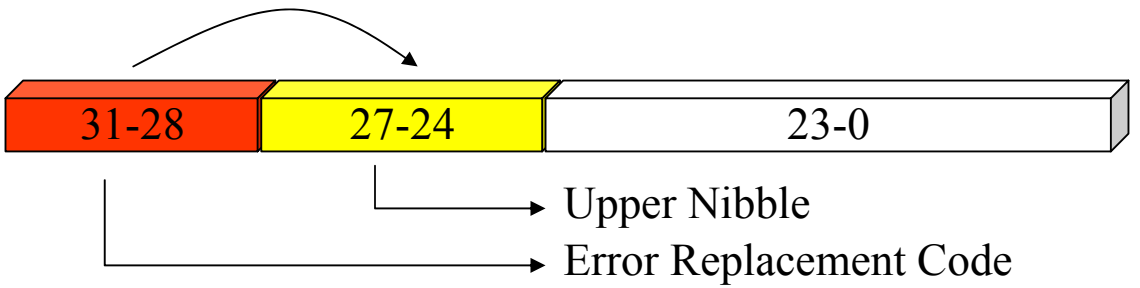
With 5-bits, 18 TDCs can be coded

See: T. Wijnen, "The MROD data format", (ATL-COM-MUON-2003-011)
http://www.hef.kun.nl/atlas/

Data Format: Parity errors



When the MRODin encounters a TDC Parity Error or an Input Link Parity Error, it replaces the upper nibble with an Error replacement code (programmable)



MRODin Interrupts

- IRQ0
  - X — I2O_FIFO Full (128 entries)
  - X S — Buffer Memory Partition Full (8 K words)
  - S — Read Out Maximum
  - TDC Parity error (+ Overrun)
- IRQ1
  - Input Link Parity error (+ Overrun)
  - Input Link Down
- IRQ2
  - TDC Early, Late (+ Overrun)

Notes:

X: Fatal

S: Shutdown Read-out for particular TDC

All interrupt sources are individually mask-able

MRODin FPGA Registers

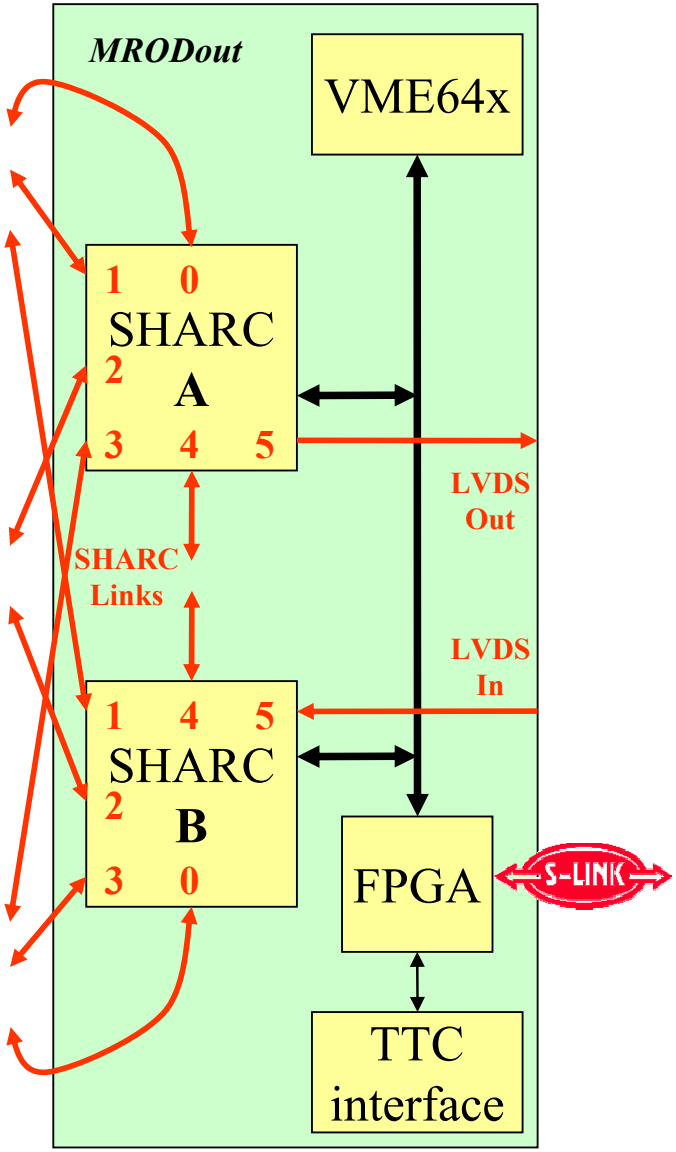
- Separator
  - Pattern
  - Control Bit Pattern
  - Mask
  - Control Bit Mask
- TDC Header
  - Pattern
  - Control Bit Pattern
  - Mask
  - Control Bit Mask
- TDC Trailer
  - Pattern
  - Control Bit Pattern
  - Mask
  - Control Bit Mask
- No Data
  - Pattern
  - Control Bit Pattern
  - Mask
  - Control Bit Mask
- Error-Code Replace Patterns
- msb's MRODin Header Pattern (TLP)
- msb's MRODin Trailer Pattern (TWC)
- Event Length FIFO
- Interrupt Control IRQ0
  - I2O_FIFO Full
  - Buffer Memory Partition Full
  - Read-out Maximum
  - TDC Parity Error (Overrun)
- TDC Parity Error Individual Interrupt Mask
- Input Link Interrupt IRQ1
  - Input Link Parity error (Overrun)
  - Input Link Down
- Early and Late Event-ID IRQ2
  - TDC number, Event-ID (Overrun)
- Test & Input Link Control Status Register
- Test Link Data Register
- Test Link Control Register
- Maximum Event Size
- Expected Event-ID
- TDC Mask Register
- Partition Read-out Enable
- Separator Flags Register

Summary MRODin

- Event building of TDC data
- Tetris register creates a fault tolerant design
- FPGAs supply SHARCs with appropriate (error) information
- Testable by SHARC via access to registers and memory

MRODout

- VME64x Interface
- TTC Interface via TIM
- FIFO and Flow control via ROL
- Interrupt sources
- FPGA registers



VME64x Slave Interface

VME64x

Guideline; Chris Parkman, “ATLAS Read Out Driver VMEbus Implementation”:
http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/documents/ROD_VME83.pdf

- CR/CSR (AM 0x2F)
  - A24/D32 — Single Cycle — Mandatory
  - A24/D32/D16/D08(EO)/D08(O) — Single Cycle, RMW — Optional
- SHARCs
  - A32/D32 — Single Cycle, RMW, BLT — Preferred
- CR full VME64x range, currently filled with the VME64 subset
- CSR BAR/BitSet/BitClr registers
- SHARC may generate a VMEbus Interrupt
  - Selectable IRQ level [1..7] — {I(n) D08(O) where n=1..7}
  - Programmable 8-bit Status-ID
  - ROACK — Preferred
- AM 0x10 (User Defined) used as HARD Reset for the SHARCs

TTC Interface

TIM Designed by  University College London

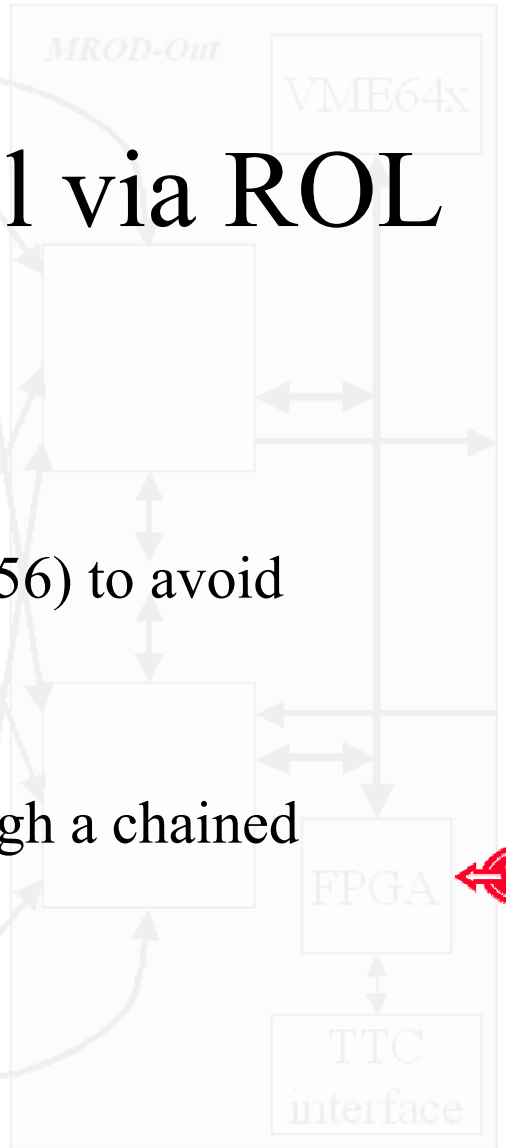
http://www.hep.ucl.ac.uk/atlas/sct/tim/

- Uses a special P3 backplane with a so called TTC-bus (8 serial signals)
- TIM Distributes:
  - Event-ID / Bunch-ID — Put into a FIFO that can be read by the SHARC
  - Trigger-Type — Put into a FIFO that can be read by the SHARC
  - ECR — Connected to SHARC IRQ1
  - BCR — not used by MROD
  - L1A — not used by MROD
- TIM Incorporates Busy Logic to throttle the CTP

TTC interface

FIFO and Flow control via ROL

- Output S-Link interface 160 MB/s
- FPGA contains S-Link Output FIFO (256) to avoid local bus stall due to an XOFF
- SHARCs can transfer output data through a chained DMA



MRODout Interrupts

- IRQ0 S-Link Return Lines (LRL) Change
  S-Link LDOWN
- IRQ1 Event Counter Reset (ECR)
- IRQ2 Event/Bunch-ID FIFO Full
  Trigger Type FIFO Full

All interrupt sources are individually mask-able

MRODout FPGA Registers

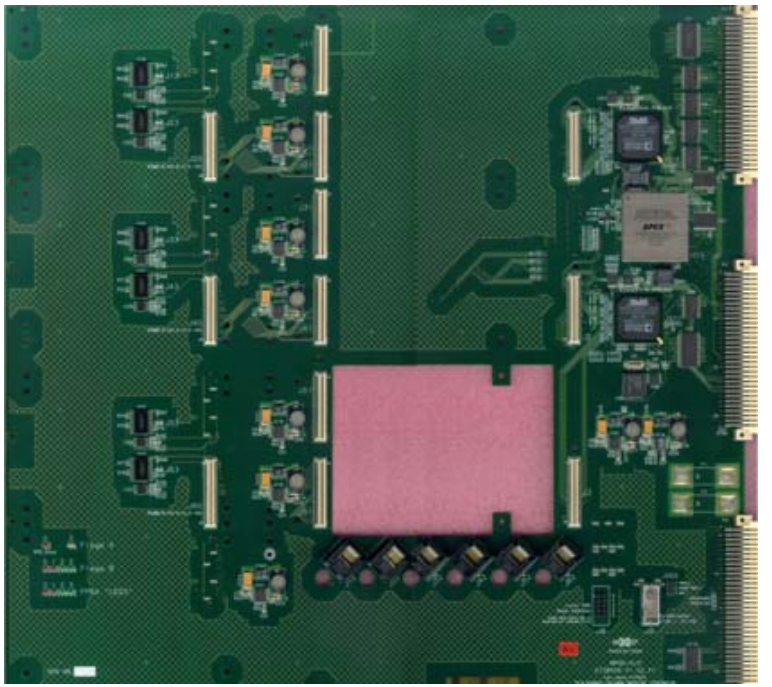
- VMEbus IRQ
  - IRQ Level
  - 8-bit Status-ID Pattern
- VMEbus BAR and IRQ
  - Trigger VMEbus IRQ
  - IRQ Pending Status
  - BAR
- S-LINK Status and Interrupt Register
  - Link Return Lines (LRL)
  - LRL Change Interrupt
  - Link Down Interrupt
- TTC Control/Status and Interrupt Register
  - Event-ID/Bunch-ID/Trigger Type FIFO Empty/Full status
  - Event-ID/Bunch-ID/Trigger Type FIFO Full Interrupt
  - FIFO Flush select (Software or ECR)
- Resets and LEDs

Summary MRODout

- Event building of data from 3 (/4) MRODin boards
- Formatting of the output data for the ROL
- Testable by SHARC via access to register

Questions?

MRODin



MRODout

MROD-1 Reset Topology