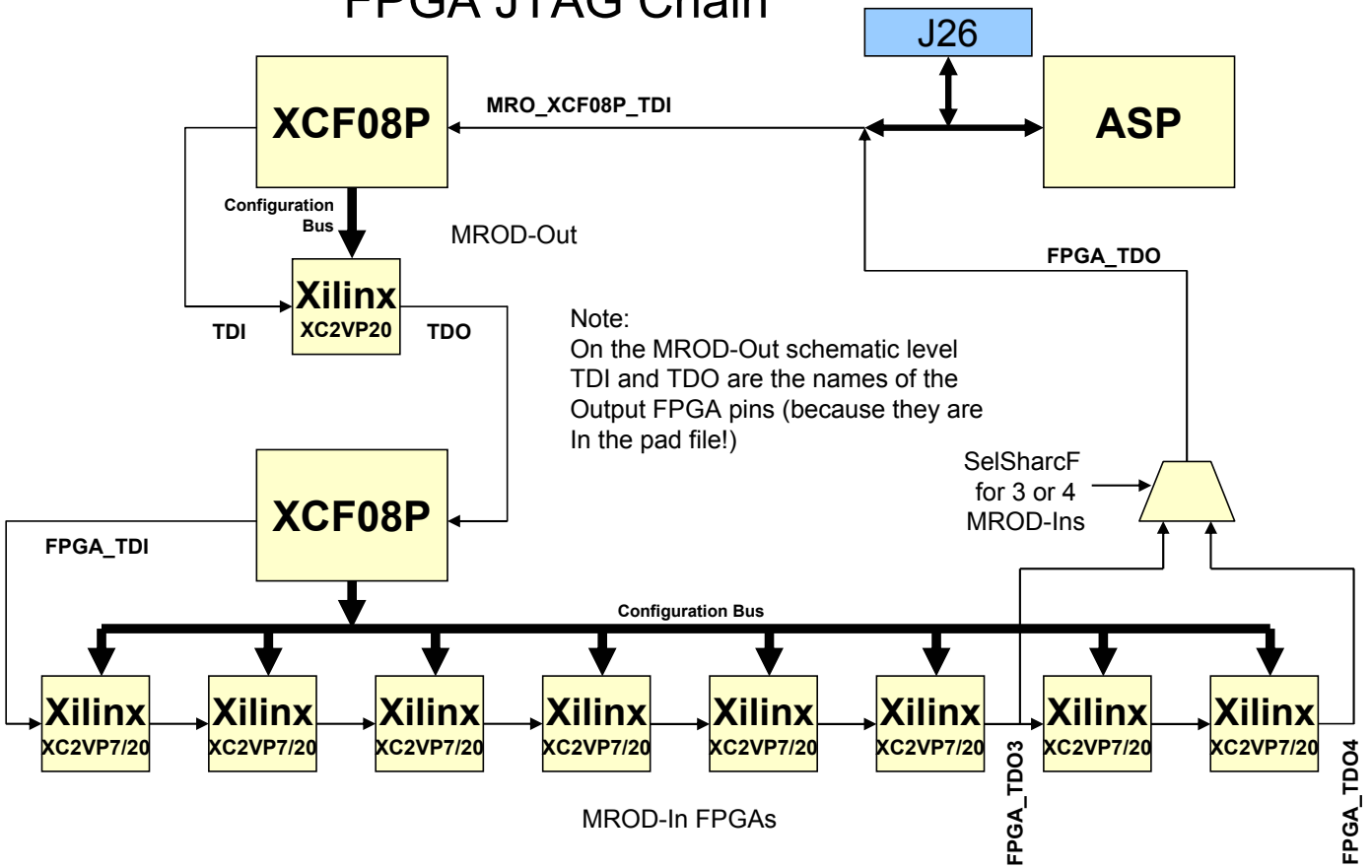
FPGA JTAG Chain



Note:
Slave SelectMAP **must** be used because CCLK must be driven by the one and only configuration device, not by multiple FPGAs!

M2	M1	M0	
0	1	1	Master SelectMap
1	1	0	Slave SelectMap
1	0	1	Boundary Scan