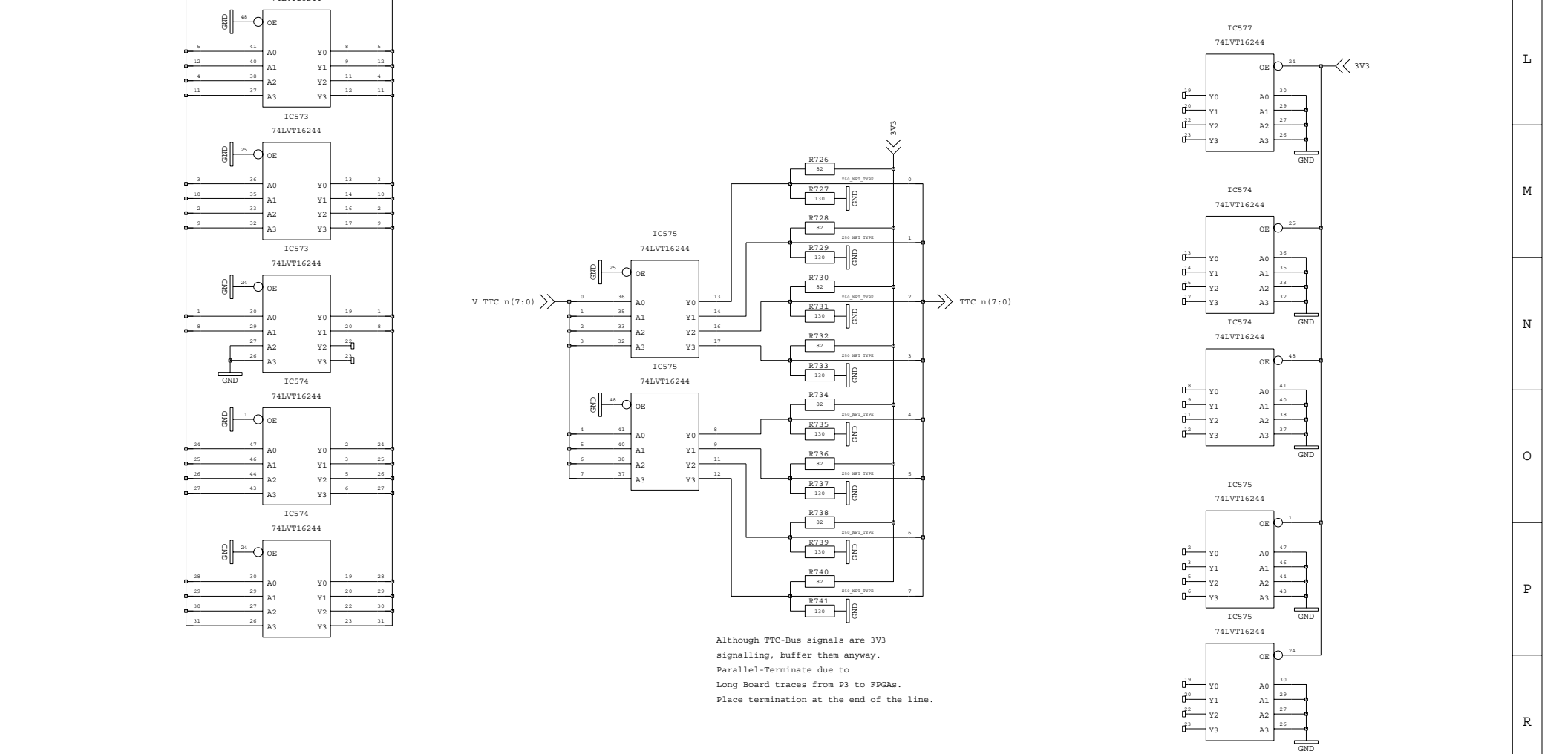
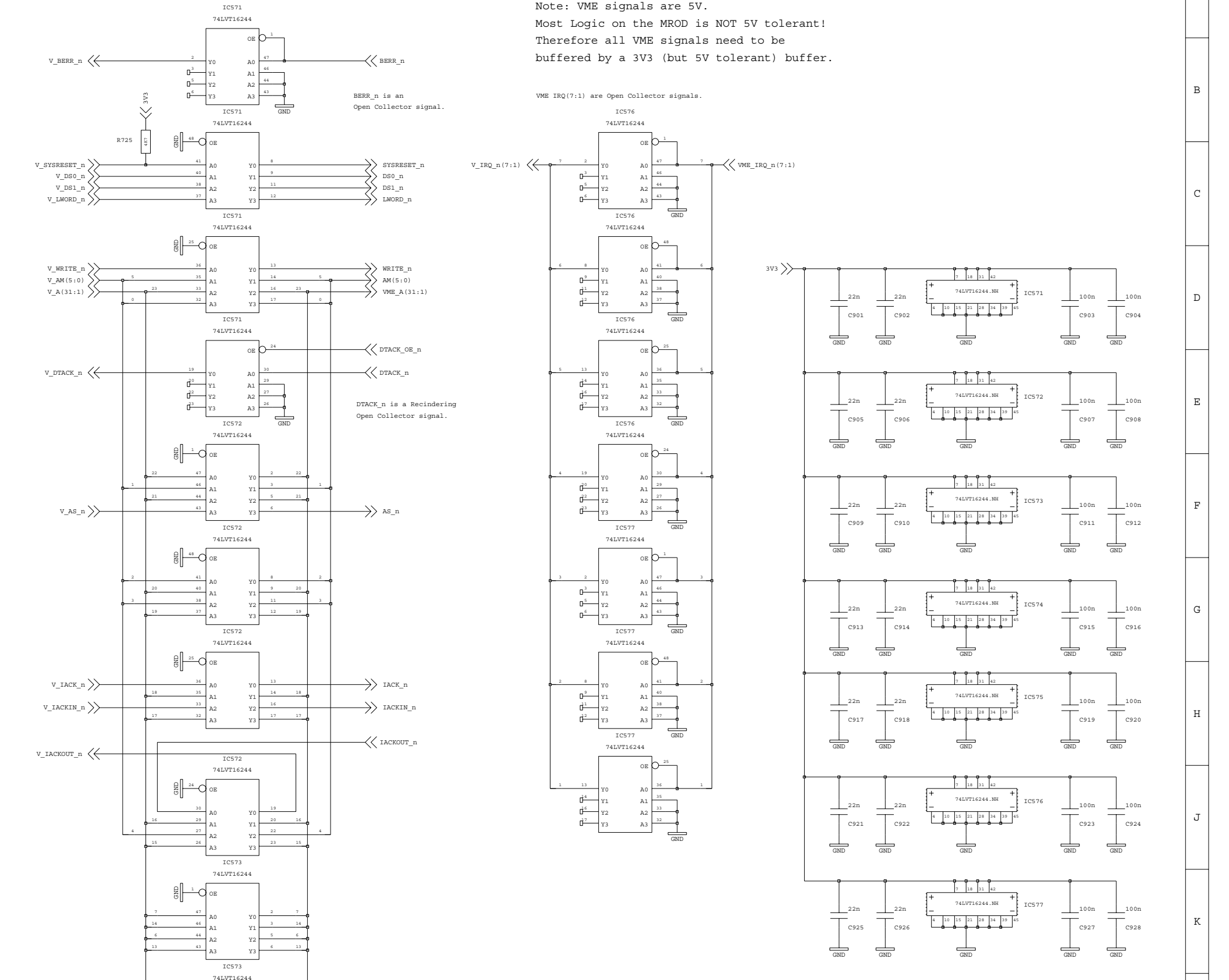
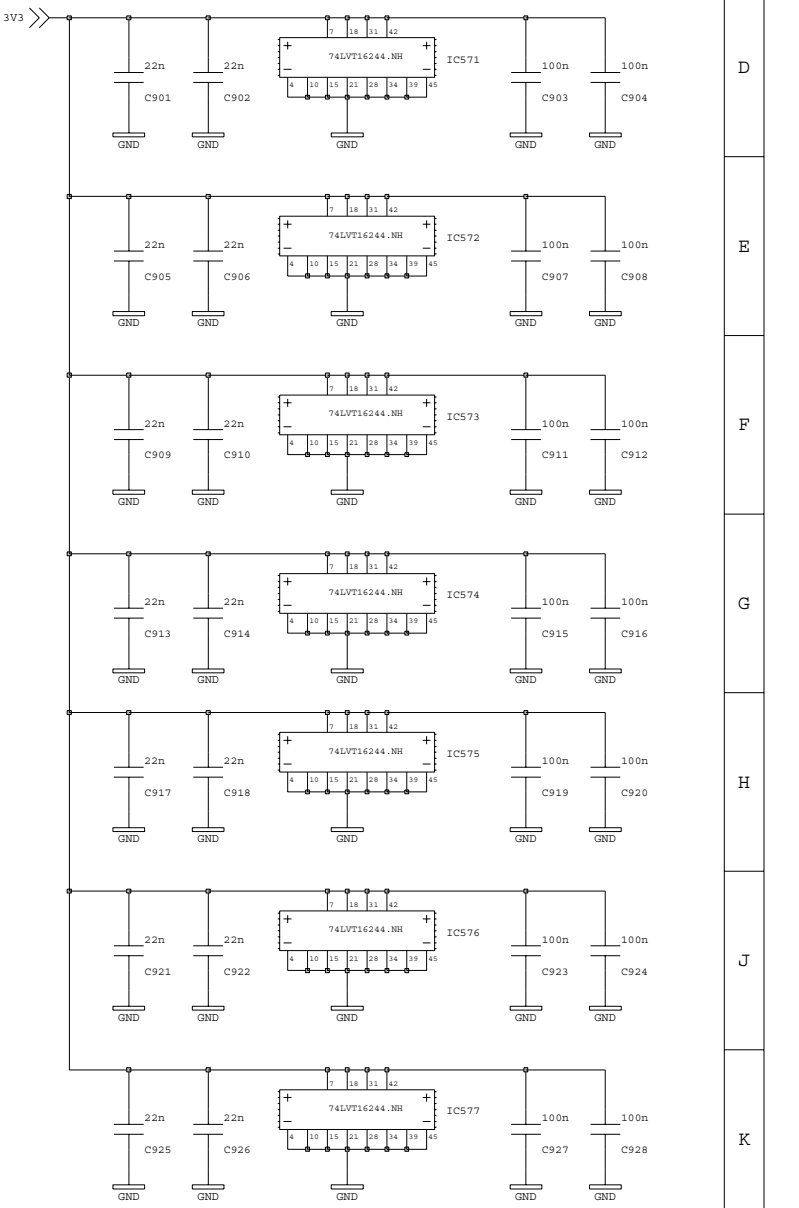


Note: VME signals are 5V.
Most Logic on the MROD is NOT 5V tolerant!
Therefore all VME signals need to be buffered by a 3V3 (but 5V tolerant) buffer.

VME IRQ(7:1) are Open Collector signals.



Although TTC-Bus signals are 3V3 signalling, buffer them anyway.
Parallel-Terminate due to Long Board traces from P3 to FPGAs.
Place termination at the end of the line.



MROD-Out		Rev	V2	3	
		Date	7 Feb 2006		
VME Bus Other Buffers		Time	1:35:25 pm		
Proj:	MROD-X	Proj.No:			
Peter Jansweijer		peterj@nikhef.nl			
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA		Size	A3	4 1 4 A
	KRUISLAAN 409, 020-592 2000		Dim	297 x 420 mm	
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