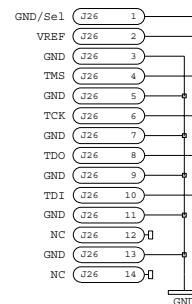
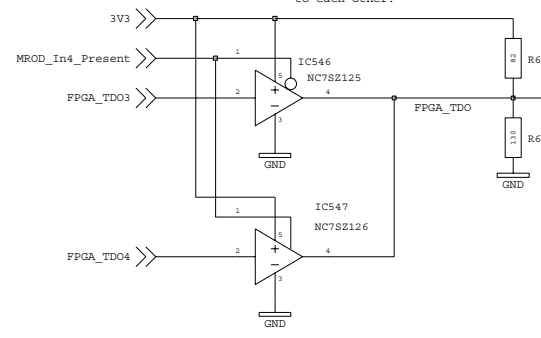


JTAG Parallel IV Connector

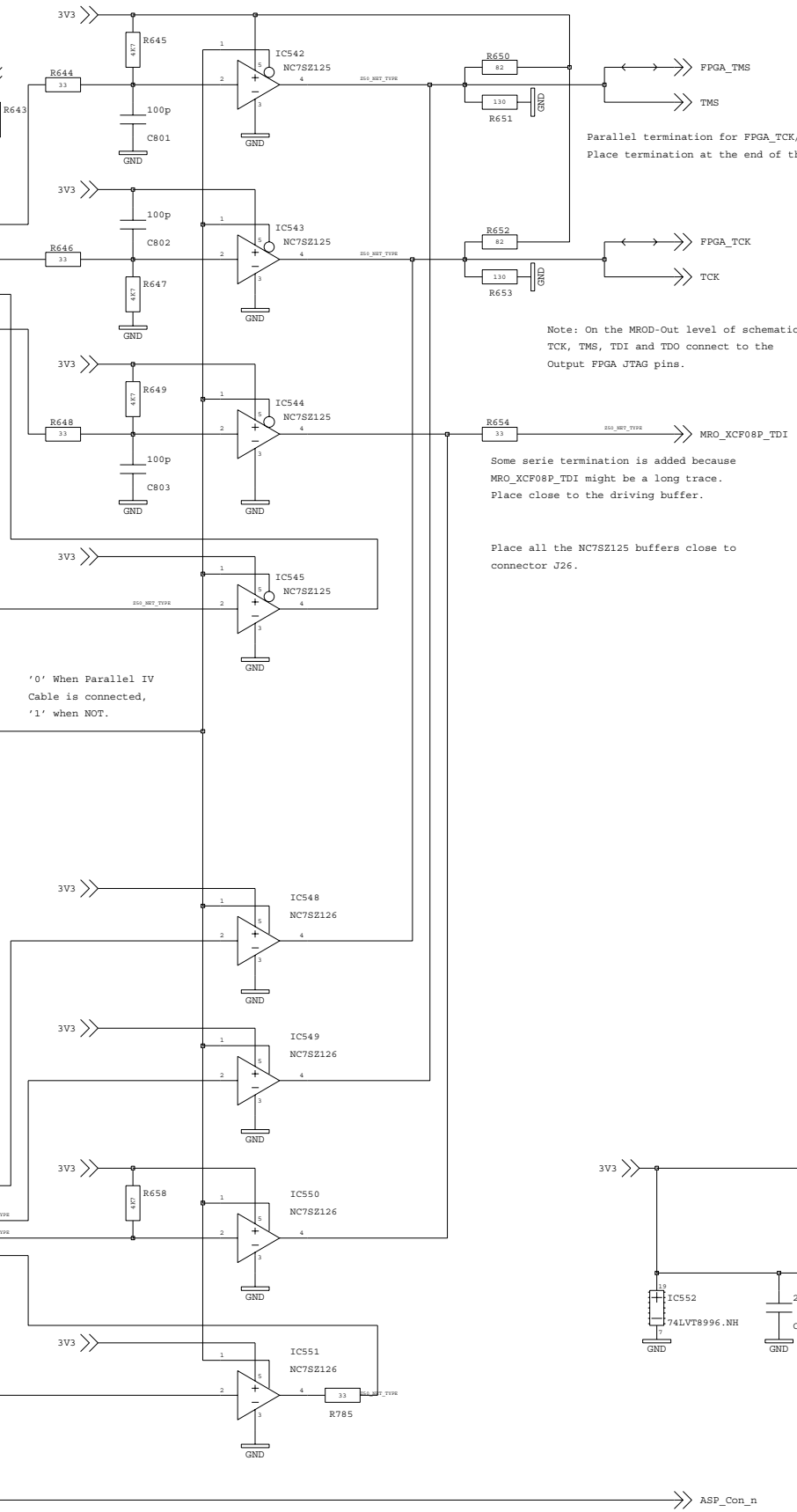
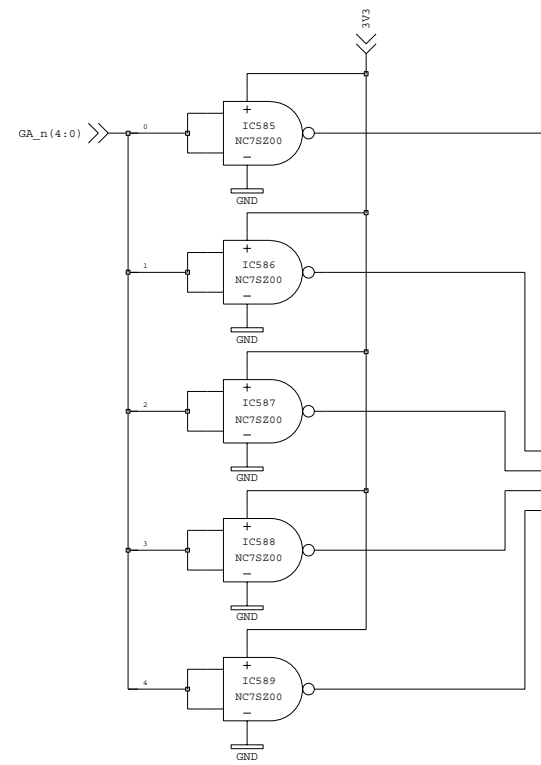
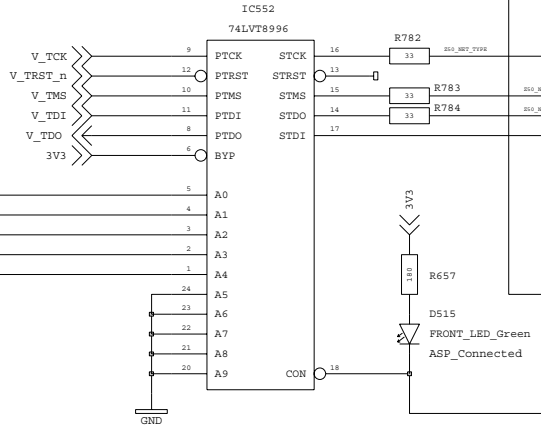


Parallel termination is added because FPGA\_TDO might be a long traces. Place termination at end of the line; driving buffers close to each other.



Select either FPGA\_TDO3 or 4 depending on whether input FPGA 7 and 8 (MROD\_In4) are placed on the board.  
 MROD\_In4\_Present = '0' => Input FPGA 7&8 are absent.  
 MROD\_In4\_Present = '1' => Input FPGA 7&8 are present.

MTM-Bus ASP Connection



Parallel termination for FPGA\_TCK/TMS. Place termination at the end of the line.

Note: On the MROD-Out level of schematic TCK, TMS, TDI and TDO connect to the Output FPGA JTAG pins.

Some serie termination is added because MRO\_XCF08P\_TDI might be a long trace. Place close to the driving buffer.

Place all the NC7SZ125 buffers close to connector J26.

'0' When Parallel IV Cable is connected, '1' when NOT.

<b>MROD-Out</b>		Rev	V2	4
		Date	7 Feb 2006	
FPGA JTAG Chain		Time	1:32:17 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
<b>NIKHEF</b> © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	11 of 19	