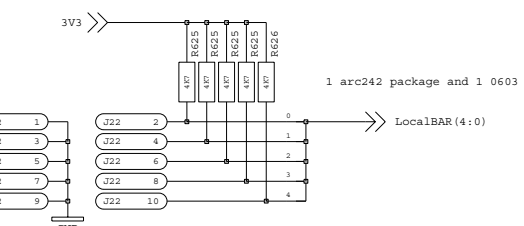
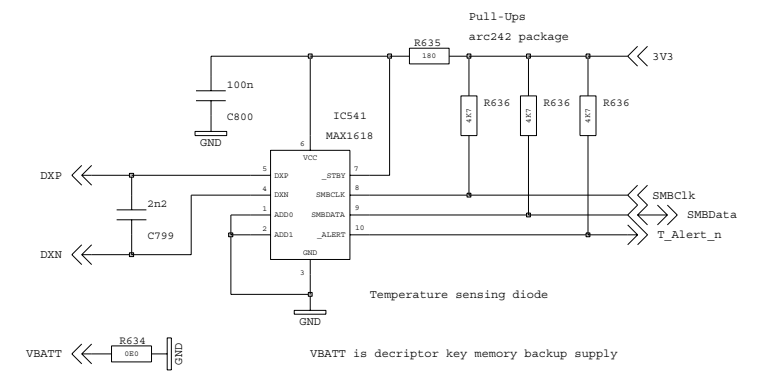
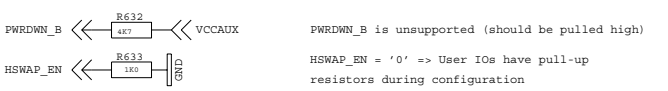
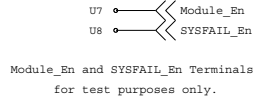
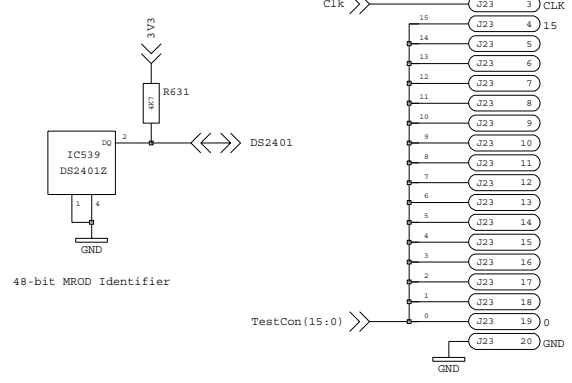


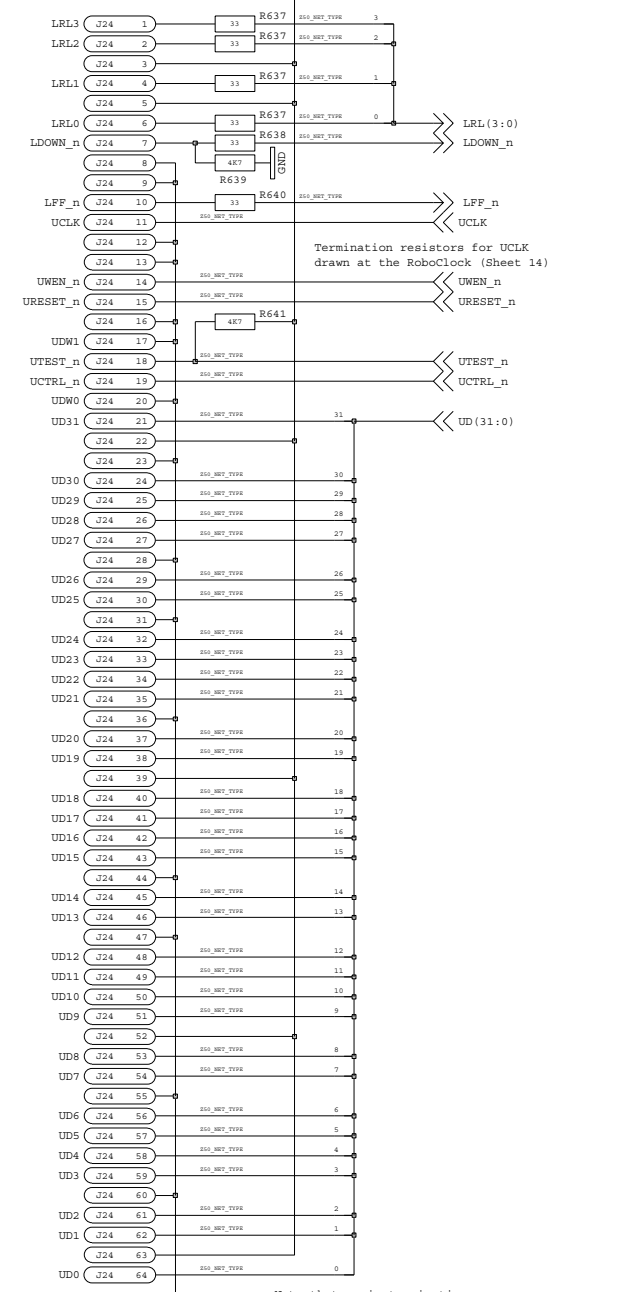
GA\_n(4:0) and GAP\_n are either 'open' or 'ground' on the VME64x Back Plane.



LocalBAR  
These settings are used for BAR at power-up when this module is plugged into a non-VME64x backplane (without GA pins).



Note that the 33 ohm series termination resistors for the LRL, LDOWN\_n and LFF\_n signals should be placed near the S-Link connector.



Note that series termination is incorporated by the Digital Contolled Impedance (DCI) feature of the Output FPGA.

S-LINK FEMBE Connector Receptable

S-Link and Outp. FPGA Auxiliary Connections		Rev V2 8	
		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:29:59 pm	
Peter Jansweijer		Name tonvr	
peterj@nikhef.nl		Size A3	4 1 4 A
<b>NIKHEF</b> NATIONAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Dim 420 x 297 mm	
		Page 10 of 19	

