

IC201
ADSP21160N

A1	DATA(14)	A2	DATA(13)	A3	DATA(10)	A4	DATA(8)	A5	DATA(4)	A6	DATA(2)	A7	TDI	A8	TRST_n	A9	RESET_n	A10	PPBA	A11	IRQ0_n	A12	FLAG1	A13	TMEXF	A14	NC_A14	A15	NC_A15	A16	TPF1	A17	SPF1	A18	RCLK0	A19	DT0	A20	LOGAT(4)
B1	DATA(22)	B2	DATA(16)	B3	DATA(15)	B4	DATA(9)	B5	DATA(6)	B6	DATA(3)	B7	DATA(0)	B8	TCK	B9	Sharc_BMU_n	B10	IRQ0_n	B11	FLAG3	B12	FLAG0	B13	NC_B13	B14	NC_B14	B15	DT1	B16	RCLK1	B17	RFS0	B18	TCCLK0	B19	LOGAT(5)	B20	LOGAT(2)
C1	DATA(24)	C2	DATA(18)	C3	DATA(17)	C4	DATA(11)	C5	DATA(7)	C6	DATA(5)	C7	DATA(1)	C8	TMS	C9	TDO	C10	IRQ1_n	C11	FLAG2	C12	NC_C12	C13	NC_C13	C14	TCCLK1	C15	DT2	C16	DT0	C17	LOGAT(7)	C18	LOGAT(6)	C19	LSACK	C20	LOGAT(8)
D1	DATA(28)	D2	DATA(25)	D3	DATA(20)	D4	DATA(19)	D5	DATA(12)	D6	VDDEXT_04	D7	VDDINT_07	D8	VDDEXT_08	D9	VDDEXT_09	D10	VDDEXT_10	D11	VDDEXT_11	D12	VDDEXT_12	D13	VDDINT_13	D14	VDDEXT_14	D15	TPF0	D16	L1DAT(7)	D17	LOCLK	D18	LOGAT(3)	D19	LOGAT(1)	D20	L1CLK
E1	DATA(30)	E2	DATA(29)	E3	DATA(23)	E4	DATA(21)	E5	VDDEXT_05	E6	VDDINT_04	E7	VDDINT_07	E8	VDDEXT_08	E9	VDDINT_09	E10	VDDINT_10	E11	GND_B11	E12	VDDINT_12	E13	VDDINT_13	E14	VDDINT_14	E15	VDDINT_15	E16	VDDEXT_16	E17	L1DAT(6)	E18	L1DAT(5)	E19	LIACK	E20	L1DAT(1)
F1	DATA(34)	F2	DATA(33)	F3	DATA(27)	F4	DATA(26)	F5	VDDEXT_05	F6	VDDINT_04	F7	GND_F7	F8	GND_F8	F9	GND_F9	F10	GND_F10	F11	GND_F11	F12	GND_F12	F13	GND_F13	F14	GND_F14	F15	VDDINT_15	F16	VDDEXT_16	F17	L1DAT(4)	F18	L1DAT(3)	F19	L1DAT(0)	F20	L2DAT(7)
G1	DATA(38)	G2	DATA(35)	G3	DATA(32)	G4	DATA(31)	G5	VDDEXT_05	G6	VDDINT_04	G7	GND_G7	G8	GND_G8	G9	GND_G9	G10	GND_G10	G11	GND_G11	G12	GND_G12	G13	GND_G13	G14	GND_G14	G15	VDDINT_15	G16	VDDEXT_16	G17	L1DAT(2)	G18	L2DAT(6)	G19	L2DAT(4)	G20	L1CLK
H1	DATA(40)	H2	DATA(39)	H3	DATA(37)	H4	DATA(34)	H5	VDDEXT_05	H6	VDDINT_04	H7	GND_H7	H8	GND_H8	H9	GND_H9	H10	GND_H10	H11	GND_H11	H12	GND_H12	H13	GND_H13	H14	GND_H14	H15	VDDINT_15	H16	VDDEXT_16	H17	L1DAT(2)	H18	L2DAT(6)	H19	L2DAT(4)	H20	L2CLK
I1	DATA(44)	I2	DATA(43)	I3	DATA(42)	I4	DATA(41)	I5	VDDEXT_05	I6	VDDINT_04	I7	GND_I7	I8	GND_I8	I9	GND_I9	I10	GND_I10	I11	GND_I11	I12	GND_I12	I13	GND_I13	I14	GND_I14	I15	VDDINT_15	I16	VDDEXT_16	I17	L1DAT(2)	I18	L2DAT(0)	I19	HBG_n	I20	VDDEXT
J1	DATA(44)	J2	DATA(43)	J3	DATA(42)	J4	DATA(41)	J5	VDDEXT_05	J6	VDDINT_04	J7	GND_J7	J8	GND_J8	J9	GND_J9	J10	GND_J10	J11	GND_J11	J12	GND_J12	J13	GND_J13	J14	GND_J14	J15	VDDINT_15	J16	VDDEXT_16	J17	L1DAT(2)	J18	L2DAT(0)	J19	HBG_n	J20	VDDEXT
K1	CLK_CFG_0	K2	DATA(44)	K3	DATA(45)	K4	DATA(47)	K5	VDDEXT_05	K6	VDDINT_04	K7	GND_K7	K8	GND_K8	K9	GND_K9	K10	GND_K10	K11	GND_K11	K12	GND_K12	K13	GND_K13	K14	GND_K14	K15	VDDINT_15	K16	VDDEXT_16	K17	BReq_n	K18	BReq_n	K19	BReq_n	K20	BReq_n
L1	CLKIN	L2	CLK_CFG_1	L3	AGND	L4	CLK_CFG_2	L5	VDDEXT_15	L6	VDDINT_14	L7	GND_L7	L8	GND_L8	L9	GND_L9	L10	GND_L10	L11	GND_L11	L12	GND_L12	L13	GND_L13	L14	GND_L14	L15	VDDINT_15	L16	VDDEXT_16	L17	BReq_n	L18	BReq_n	L19	BReq_n	L20	BReq_n
M1	AVDD	M2	CLK_CFG_3	M3	CLKOUT	M4	NC_M4	M5	VDDEXT_05	M6	VDDINT_04	M7	GND_M7	M8	GND_M8	M9	GND_M9	M10	GND_M10	M11	GND_M11	M12	GND_M12	M13	GND_M13	M14	GND_M14	M15	VDDINT_15	M16	VDDEXT_16	M17	BReq_n	M18	BReq_n	M19	PA_n	M20	L3DAT(7)
N1	AVDD	GND	NC_B2	DATA(48)	M4	DATA(51)	M5	VDDEXT_05	M6	VDDINT_04	M7	GND_M7	M8	GND_M8	M9	GND_M9	M10	GND_M10	M11	GND_M11	M12	GND_M12	M13	GND_M13	M14	GND_M14	M15	VDDINT_15	M16	VDDEXT_16	M17	L3DAT(5)	M18	L3DAT(6)	M19	L3DAT(4)	M20	L3CLK	
O1	DATA(49)	O2	DATA(50)	O3	DATA(52)	O4	DATA(55)	O5	VDDEXT_05	O6	VDDINT_04	O7	GND_O7	O8	GND_O8	O9	GND_O9	O10	GND_O10	O11	GND_O11	O12	GND_O12	O13	GND_O13	O14	GND_O14	O15	VDDINT_15	O16	VDDEXT_16	O17	L3DAT(2)	O18	L3DAT(1)	O19	L3DAT(3)	O20	L3ACK
P1	DATA(17)	P2	DATA(18)	P3	DATA(20)	P4	DATA(23)	P5	VDDEXT_05	P6	VDDINT_04	P7	GND_P7	P8	GND_P8	P9	GND_P9	P10	GND_P10	P11	GND_P11	P12	GND_P12	P13	GND_P13	P14	GND_P14	P15	VDDINT_15	P16	VDDEXT_16	P17	L3DAT(2)	P18	L3DAT(1)	P19	L3DAT(3)	P20	L3ACK
Q1	DATA(53)	Q2	DATA(54)	Q3	DATA(57)	Q4	DATA(60)	Q5	VDDEXT_05	Q6	VDDINT_04	Q7	GND_Q7	Q8	GND_Q8	Q9	GND_Q9	Q10	GND_Q10	Q11	GND_Q11	Q12	GND_Q12	Q13	GND_Q13	Q14	GND_Q14	Q15	GND_Q15	Q16	VDDEXT_16	Q17	VDDEXT_16	Q18	L4DAT(5)	Q19	L4DAT(6)	Q20	L4DAT(7)
R1	DATA(21)	R2	DATA(22)	R3	DATA(25)	R4	DATA(28)	R5	VDDEXT_05	R6	VDDINT_04	R7	GND_R7	R8	GND_R8	R9	GND_R9	R10	GND_R10	R11	GND_R11	R12	GND_R12	R13	GND_R13	R14	GND_R14	R15	GND_R15	R16	VDDEXT_16	R17	VDDEXT_16	R18	L4DAT(5)	R19	L4DAT(6)	R20	L4DAT(7)
S1	DATA(56)	S2	DATA(58)	S3	DATA(59)	S4	DATA(63)	S5	VDDEXT_05	S6	VDDINT_04	S7	VDDINT_07	S8	VDDINT_08	S9	VDDINT_09	S10	VDDINT_10	S11	VDDINT_11	S12	VDDINT_12	S13	VDDINT_13	S14	VDDINT_14	S15	VDDINT_15	S16	VDDEXT_16	S17	L4DAT(3)	S18	L4ACK	S19	L4CLK	S20	L4DAT(4)
T1	DATA(24)	T2	DATA(26)	T3	DATA(27)	T4	DATA(31)	T5	VDDEXT_05	T6	VDDINT_04	T7	VDDINT_07	T8	VDDINT_08	T9	VDDINT_09	T10	VDDINT_10	T11	VDDINT_11	T12	VDDINT_12	T13	VDDINT_13	T14	VDDINT_14	T15	VDDINT_15	T16	VDDEXT_16	T17	L4DAT(3)	T18	L4ACK	T19	L4CLK	T20	L4DAT(4)
U1	DATA(61)	U2	DATA(62)	U3	ADDR(3)	U4	ADDR(2)	U5	VDDEXT_05	U6	VDDEXT_04	U7	VDDEXT_07	U8	VDDEXT_08	U9	VDDEXT_09	U10	VDDEXT_10	U11	VDDEXT_11	U12	VDDEXT_12	U13	VDDEXT_13	U14	VDDEXT_14	U15	VDDEXT_15	U16	VDDEXT_16	U17	L4DAT(7)	U18	L4DAT(0)	U19	L4DAT(1)	U20	L4DAT(2)
V1	ADDR(4)	V2	ADDR(6)	V3	ADDR(17)	V4	ADDR(10)	V5	ADDR(14)	V6	ADDR(18)	V7	ADDR(22)	V8	ADDR(25)	V9	ADDR(28)	V10	ADDR(28)	V11	ADDR(1)	V12	MS1_n	V13	MS1_n	V14	MS1_n	V15	MS1_n	V16	MS1_n	V17	L5DAT(2)	V18	L5ACK	V19	L5DAT(4)	V20	L5DAT(6)
W1	ADDR(5)	W2	ADDR(8)	W3	ADDR(12)	W4	ADDR(15)	W5	ADDR(17)	W6	ADDR(20)	W7	ADDR(23)	W8	ADDR(26)	W9	ADDR(29)	W10	ADDR(29)	W11	ADDR(0)	W12	BMS_n	W13	BMS_n	W14	BMS_n	W15	BMS_n	W16	BMS_n	W17	L5DAT(1)	W18	L5DAT(3)	W19	L5DAT(5)	W20	L5CLK
X1	ADDR(8)	X2	ADDR(11)	X3	ADDR(13)	X4	ADDR(14)	X5	ADDR(19)	X6	ADDR(21)	X7	ADDR(24)	X8	ADDR(27)	X9	ADDR(30)	X10	ADDR(31)	X11	ADDR(1)	X12	MS2_n	X13	MS2_n	X14	MS2_n	X15	MS2_n	X16	MS2_n	X17	MS2_n	X18	MS2_n	X19	MS2_n	X20	MS2_n
Y1	ADDR(8)	Y2	ADDR(11)	Y3	ADDR(13)	Y4	ADDR(14)	Y5	ADDR(19)	Y6	ADDR(21)	Y7	ADDR(24)	Y8	ADDR(27)	Y9	ADDR(30)	Y10	ADDR(31)	Y11	ADDR(1)	Y12	MS2_n	Y13	MS2_n	Y14	MS2_n	Y15	MS2_n	Y16	MS2_n	Y17	MS2_n	Y18	MS2_n	Y19	MS2_n	Y20	MS2_n
Z1	ADDR(8)	Z2	ADDR(11)	Z3	ADDR(13)	Z4	ADDR(14)	Z5	ADDR(19)	Z6	ADDR(21)	Z7	ADDR(24)	Z8	ADDR(27)	Z9	ADDR(30)	Z10	ADDR(31)	Z11	ADDR(1)	Z12	MS2_n	Z13	MS2_n	Z14	MS2_n	Z15	MS2_n	Z16	MS2_n	Z17	MS2_n	Z18	MS2_n	Z19	MS2_n	Z20	MS2_n

Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

ID = "000"

Booting Mode:
EBOOT = '0', LBOOT = '1', BMS_n = '1' (Input)
=> Link Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

MROD- In		Rev	V2	2
		Date	7 Feb 2006	
SHARC		Time	1:46:33 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>©-Nikhef Amsterdam</small>		<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		
		Dim	420 x 297 mm	
		Page	2 of 4	