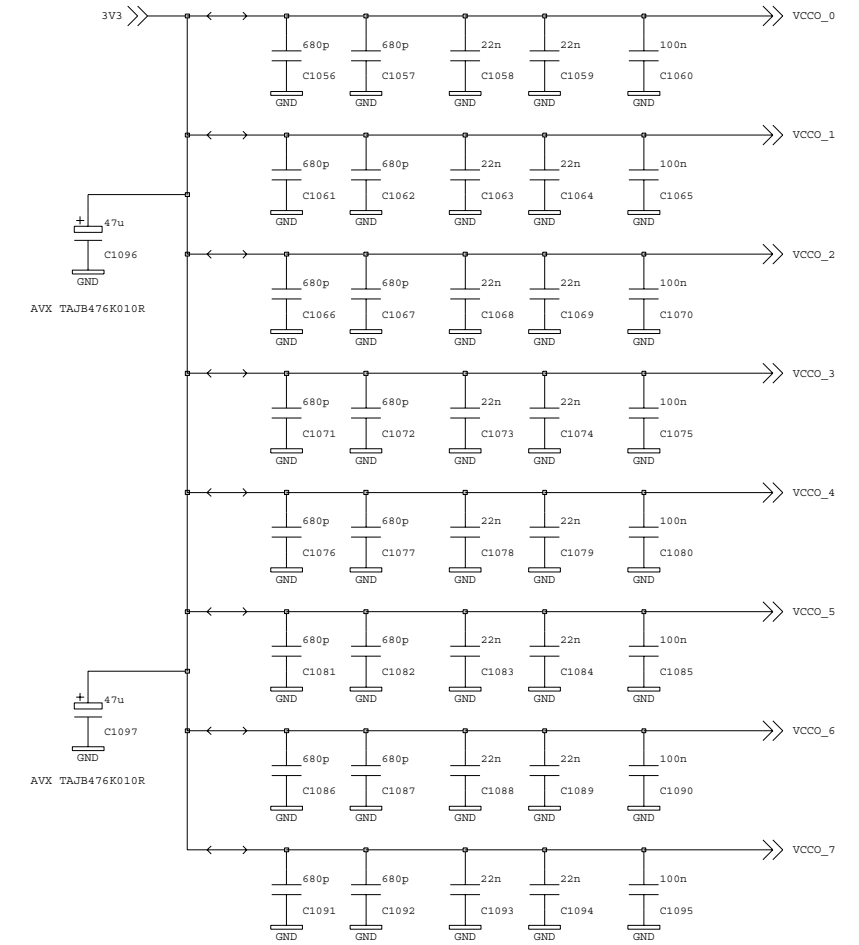
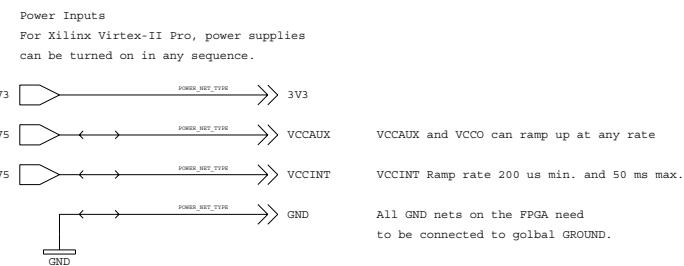
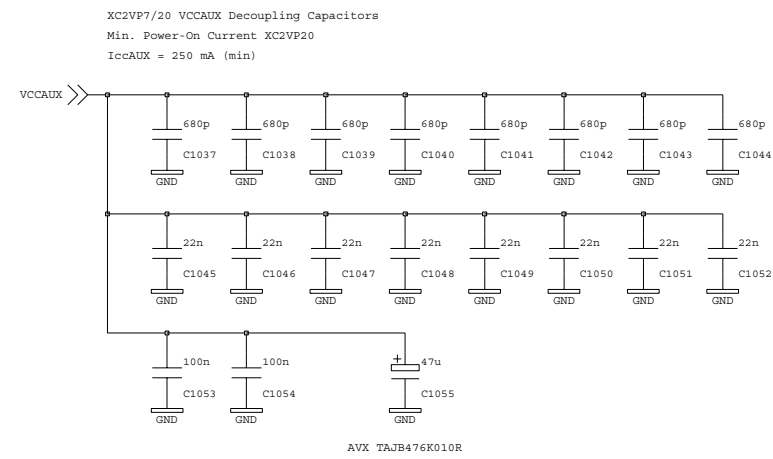
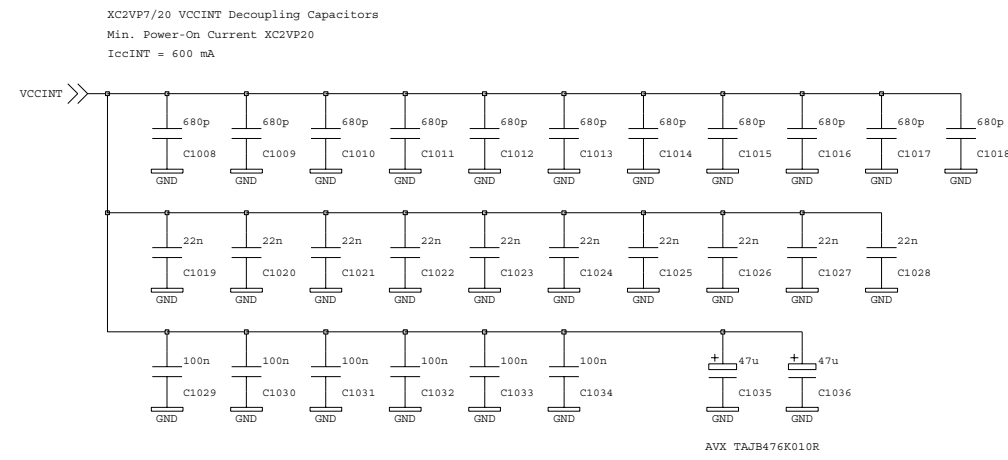


channel_in		Rev	V2	2
		Date	7 Feb 2006	
GOL Input		Time	1:50:33 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Dim	420 x 297 mm	
		Page	1 of 6	

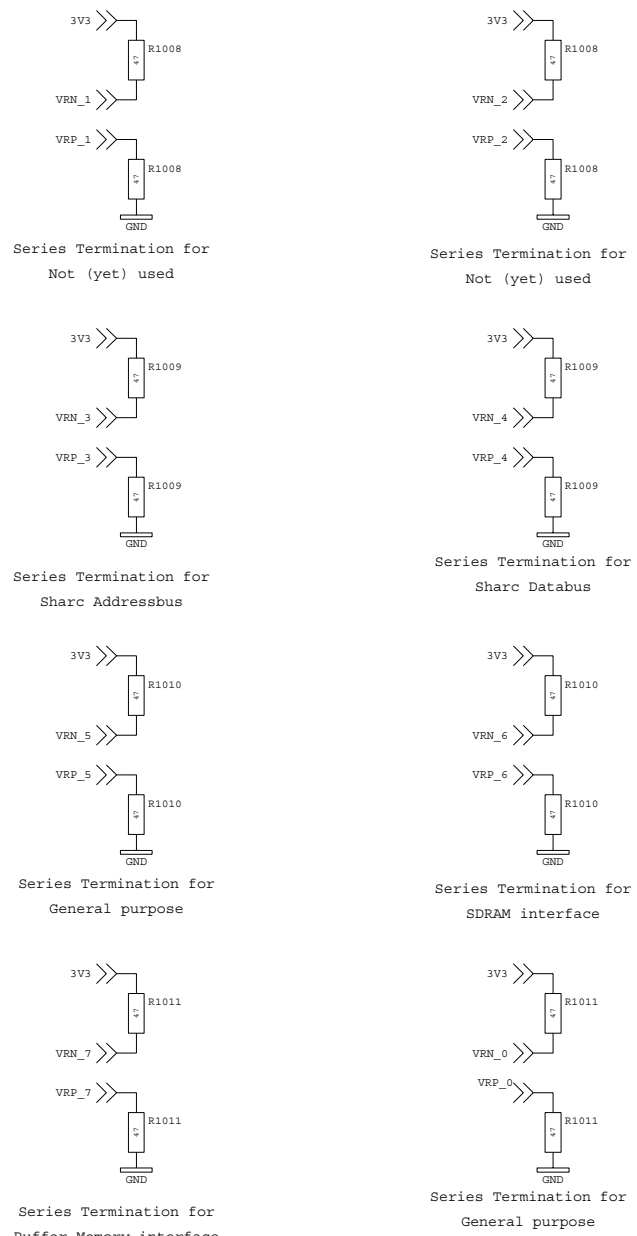
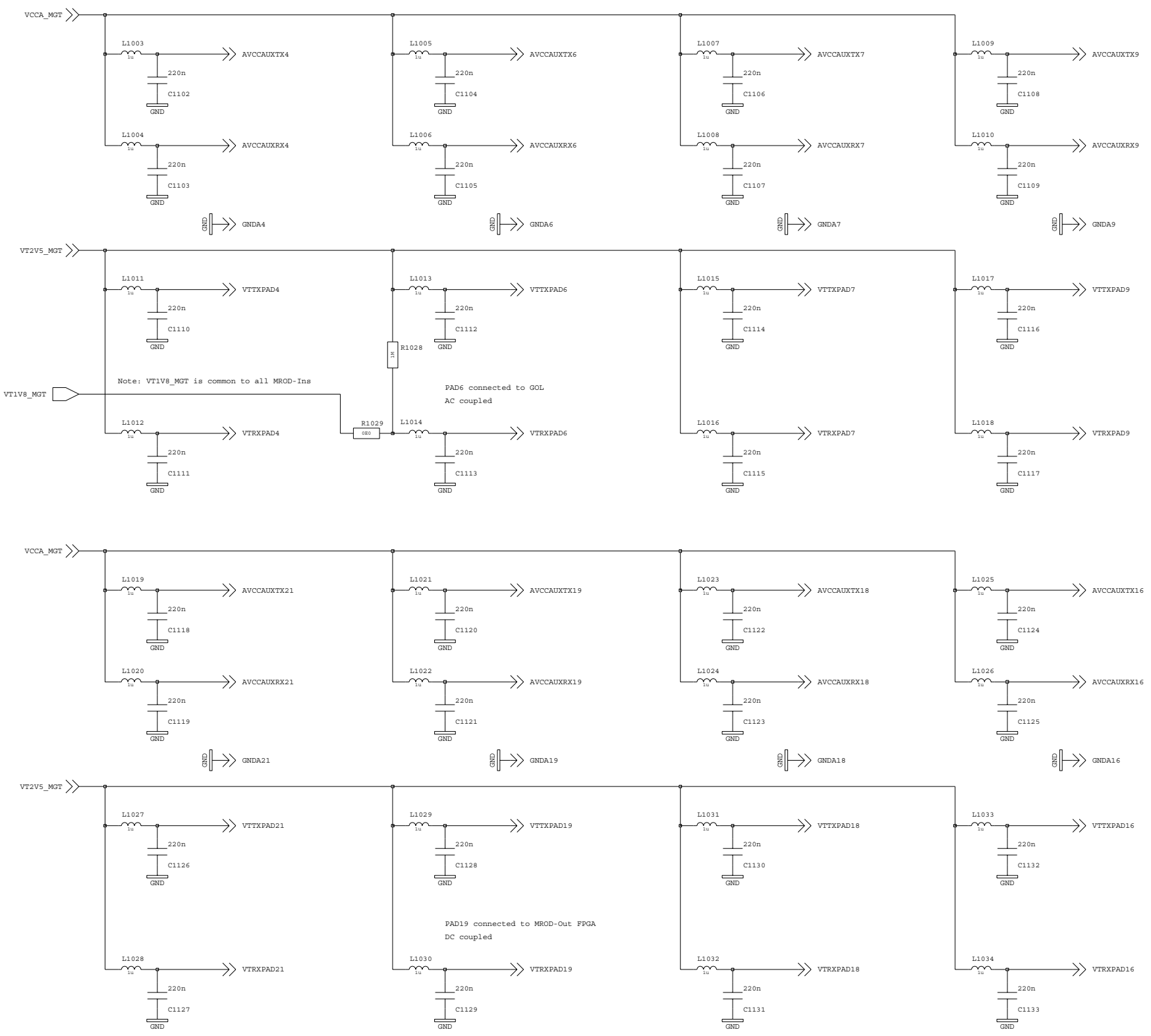
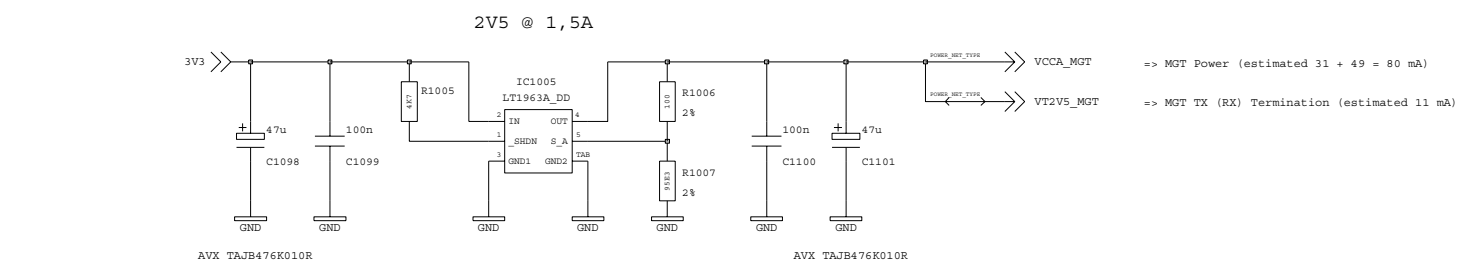
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B1	VCCAUX	B2	VRP_2	B4	AVCCAUXK9	B6	VTRXPAD9	B8	GND	B10	AVCCAUXK7	B12	AVCCAUXK7	B14	GOL_Xclk	B16	AVCCAUXK6	B18	AVCCAUXK6	B20	VTRXPAD6	B22	LEDB(0)	B24	AVCCAUXK4	B26	VTRXPAD4	B28	AVCCAUXK4	B30	VCCAUX
C1	GND	C2	GND	C4	GND	C6	GND	C8	GND	C10	GND	C12	GND	C14	GND	C16	GND	C18	GND	C20	GND	C22	GND	C24	GND	C26	GND	C28	GND	C30	GND
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E1	GND	E2	GND	E4	GND	E6	GND	E8	GND	E10	GND	E12	GND	E14	GND	E16	GND	E18	GND	E20	GND	E22	GND	E24	GND	E26	GND	E28	GND	E30	GND
F1	GND	F2	GND	F4	GND	F6	GND	F8	GND	F10	GND	F12	GND	F14	GND	F16	GND	F18	GND	F20	GND	F22	GND	F24	GND	F26	GND	F28	GND	F30	GND
G1	GND	G2	GND	G4	GND	G6	GND	G8	GND	G10	GND	G12	GND	G14	GND	G16	GND	G18	GND	G20	GND	G22	GND	G24	GND	G26	GND	G28	GND	G30	GND
H1	GND	H2	GND	H4	GND	H6	GND	H8	GND	H10	GND	H12	GND	H14	GND	H16	GND	H18	GND	H20	GND	H22	GND	H24	GND	H26	GND	H28	GND	H30	GND
I1	GND	I2	GND	I4	GND	I6	GND	I8	GND	I10	GND	I12	GND	I14	GND	I16	GND	I18	GND	I20	GND	I22	GND	I24	GND	I26	GND	I28	GND	I30	GND
J1	GND	J2	GND	J4	GND	J6	GND	J8	GND	J10	GND	J12	GND	J14	GND	J16	GND	J18	GND	J20	GND	J22	GND	J24	GND	J26	GND	J28	GND	J30	GND
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L1	GND	L2	GND	L4	GND	L6	GND	L8	GND	L10	GND	L12	GND	L14	GND	L16	GND	L18	GND	L20	GND	L22	GND	L24	GND	L26	GND	L28	GND	L30	GND
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P1	GND	P2	GND	P4	GND	P6	GND	P8	GND	P10	GND	P12	GND	P14	GND	P16	GND	P18	GND	P20	GND	P22	GND	P24	GND	P26	GND	P28	GND	P30	GND
Q1	GND	Q2	GND	Q4	GND	Q6	GND	Q8	GND	Q10	GND	Q12	GND	Q14	GND	Q16	GND	Q18	GND	Q20	GND	Q22	GND	Q24	GND	Q26	GND	Q28	GND	Q30	GND
R1	GND	R2	GND	R4	GND	R6	GND	R8	GND	R10	GND	R12	GND	R14	GND	R16	GND	R18	GND	R20	GND	R22	GND	R24	GND	R26	GND	R28	GND	R30	GND
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X1	MS0_n	X2	MS1_n	X4	MS2_n	X6	MS3_n	X8	MS4_n	X10	MS5_n	X12	MS6_n	X14	MS7_n	X16	MS8_n	X18	MS9_n	X20	MS10_n	X22	MS11_n	X24	MS12_n	X26	MS13_n	X28	MS14_n	X30	GND
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AA1	MS0_n	AA2	MS1_n	AA4	MS2_n	AA6	MS3_n	AA8	MS4_n	AA10	MS5_n	AA12	MS6_n	AA14	MS7_n	AA16	MS8_n	AA18	MS9_n	AA20	MS10_n	AA22	MS11_n	AA24	MS12_n	AA26	MS13_n	AA28	MS14_n	AA30	GND
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AF1	MS0_n	AF2	MS1_n	AF4	MS2_n	AF6	MS3_n	AF8	MS4_n	AF10	MS5_n	AF12	MS6_n	AF14	MS7_n	AF16	MS8_n	AF18	MS9_n	AF20	MS10_n	AF22	MS11_n	AF24	MS12_n	AF26	MS13_n	AF28	MS14_n	AF30	GND
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AH1	MS0_n	AH2	MS1_n	AH4	MS2_n	AH6	MS3_n	AH8	MS4_n	AH10	MS5_n	AH12	MS6_n	AH14	MS7_n	AH16	MS8_n	AH18	MS9_n	AH20	MS10_n	AH22	MS11_n	AH24	MS12_n	AH26	MS13_n	AH28	MS14_n	AH30	GND
AI1	MS0_n	AI2	MS1_n	AI4	MS2_n	AI6	MS3_n	AI8	MS4_n	AI10	MS5_n	AI12	MS6_n	AI14	MS7_n	AI16	MS8_n	AI18	MS9_n	AI20	MS10_n	AI22	MS11_n	AI24	MS12_n	AI26	MS13_n	AI28	MS14_n	AI30	GND
AJ1	MS0_n	AJ2	MS1_n	AJ4	MS2_n	AJ6	MS3_n	AJ8	MS4_n	AJ10	MS5_n	AJ12	MS6_n	AJ14	MS7_n	AJ16	MS8_n	AJ18	MS9_n	AJ20	MS10_n	AJ22	MS11_n	AJ24	MS12_n	AJ26	MS13_n	AJ28	MS14_n	AJ30	GND
AK1	MS0_n	AK2	MS1_n	AK4	MS2_n	AK6	MS3_n	AK8	MS4_n	AK10	MS5_n	AK12	MS6_n	AK14	MS7_n	AK16	MS8_n	AK18	MS9_n	AK20	MS10_n	AK22	MS11_n	AK24	MS12_n	AK26	MS13_n	AK28	MS14_n	AK30	GND

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

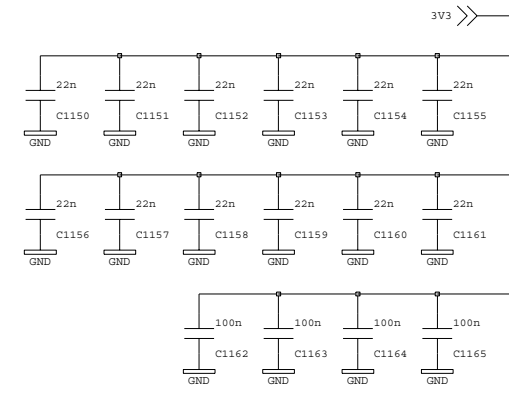
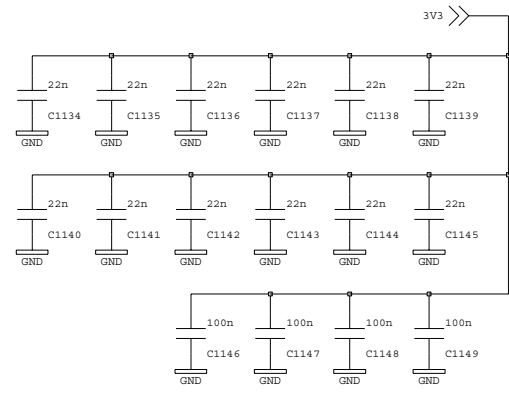
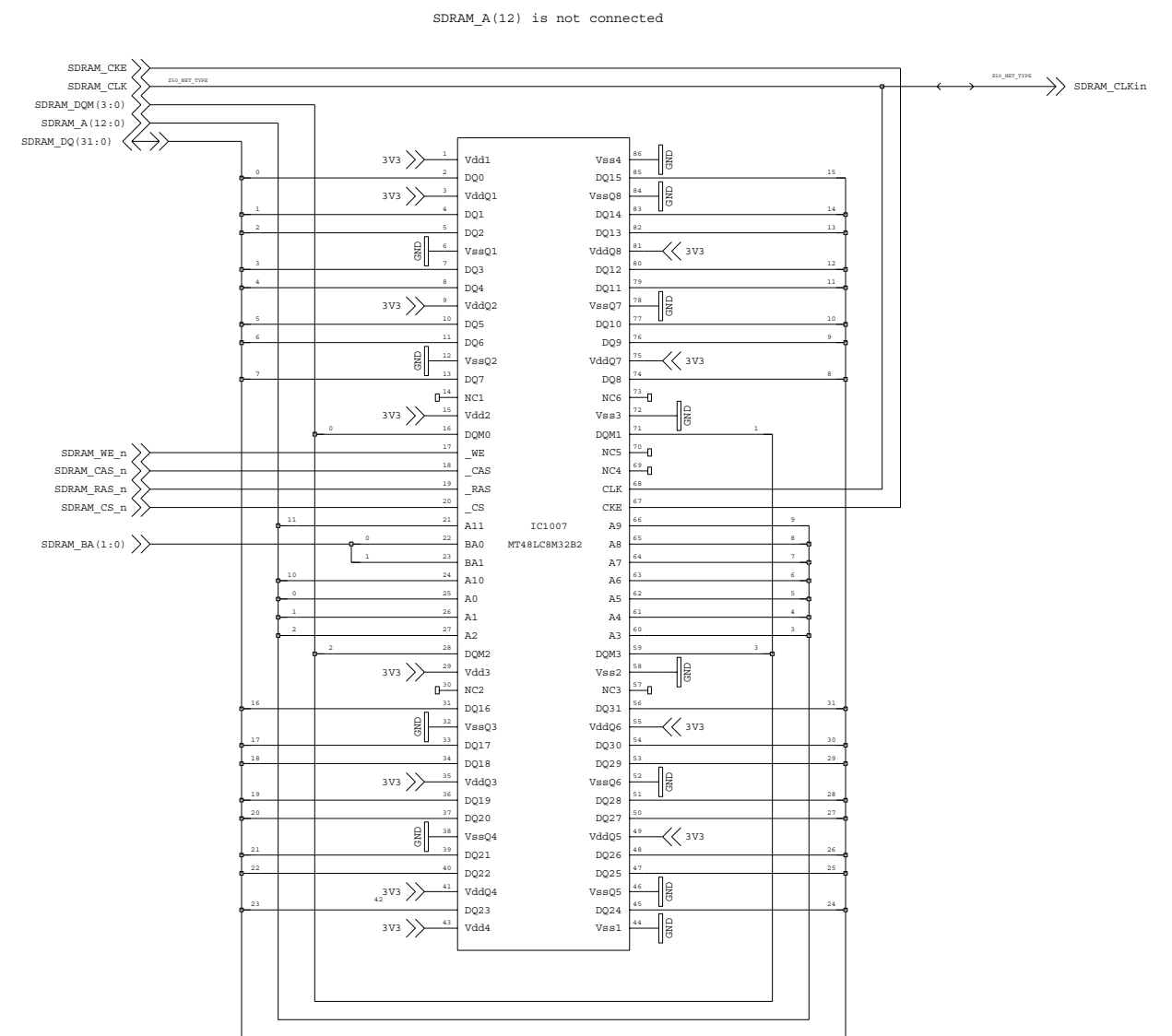
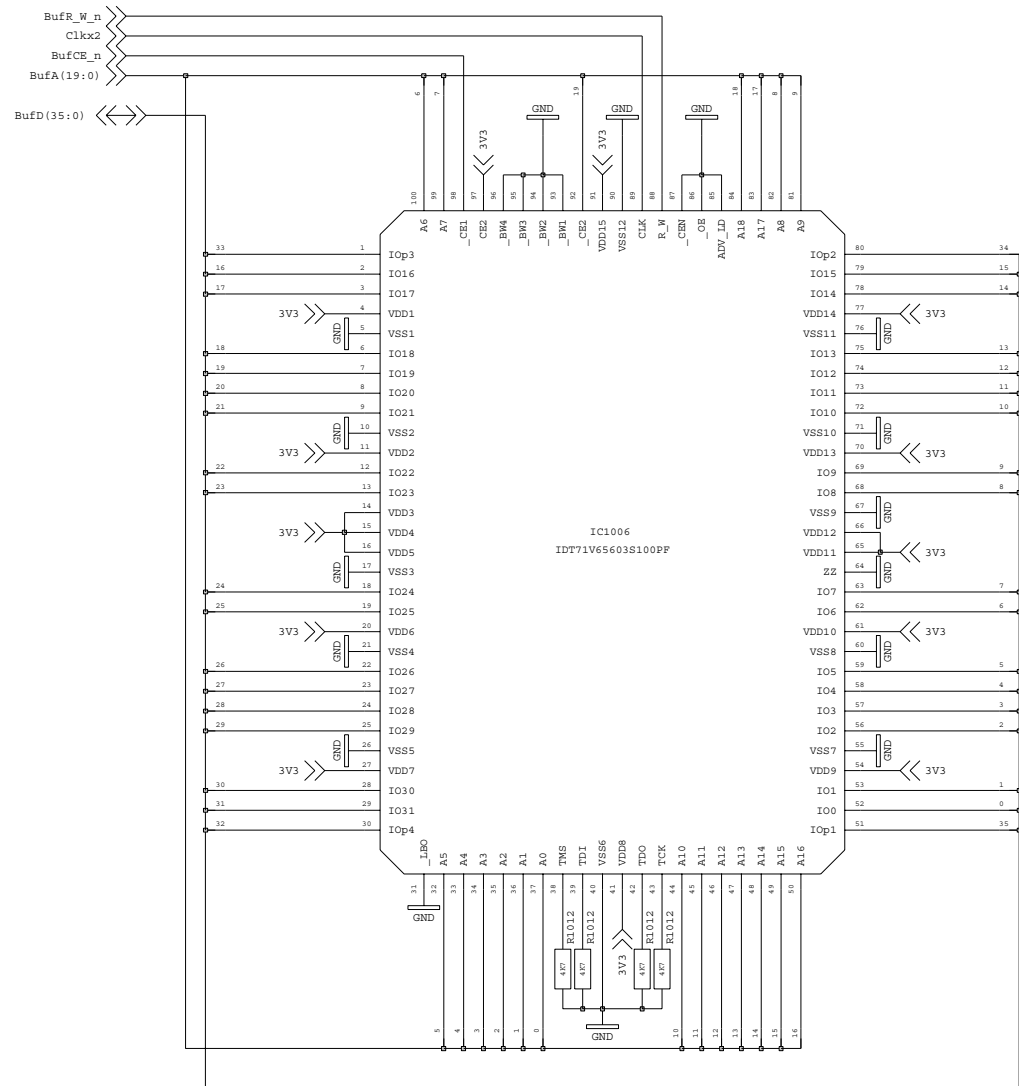
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		Date	7 Feb 2006	
Input: FPGA		Time	1:50:53 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Dim	420 x 297 mm	
		Page	2 of 6	



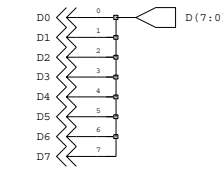
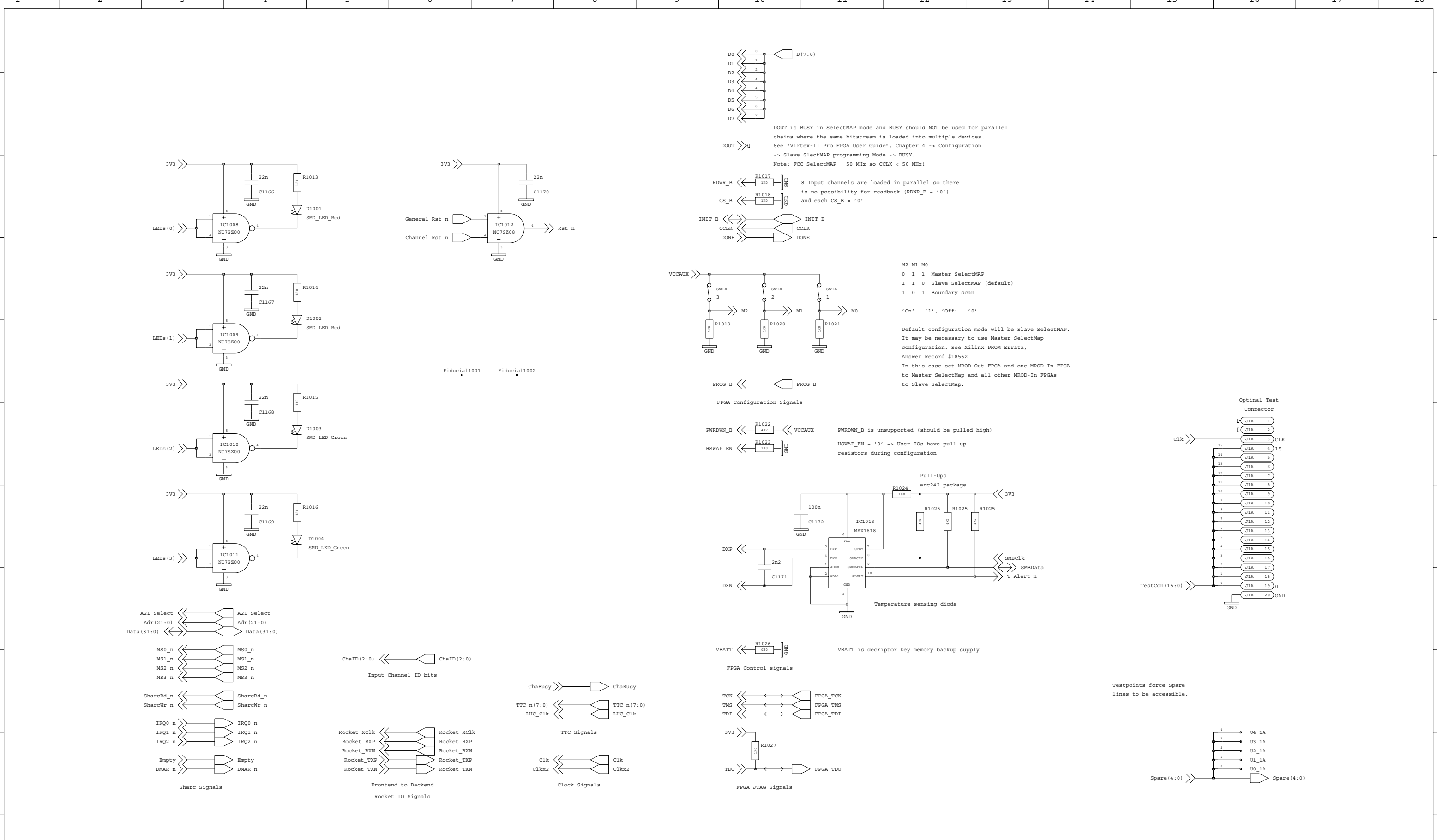
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		Date	7 Feb 2006				
Input FPGA Power Supply Decoupling		Time	1:51:34 pm				
Proj:	MROD-X	Proj.No:	38405				
Peter Jansweijer		peterj@nikhef.nl					
NIKHEF <small>© ET-Nikhef Amsterdam</small>		<small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>					
					Size	A3	4 1 4 A
					Dim	420 x 297 mm	
		Page	3	of 6			



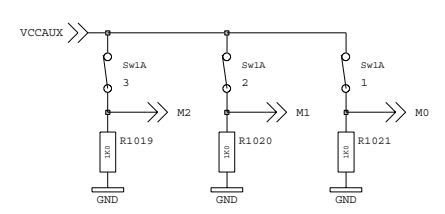
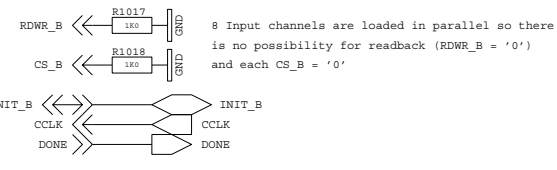
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time	1:52:01 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF <small>© Nikhef Amsterdam</small>		<small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	4	of 6



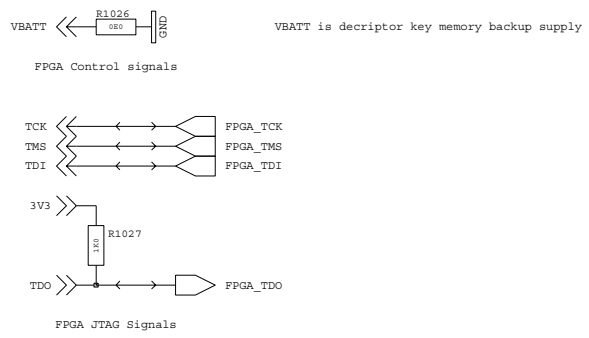
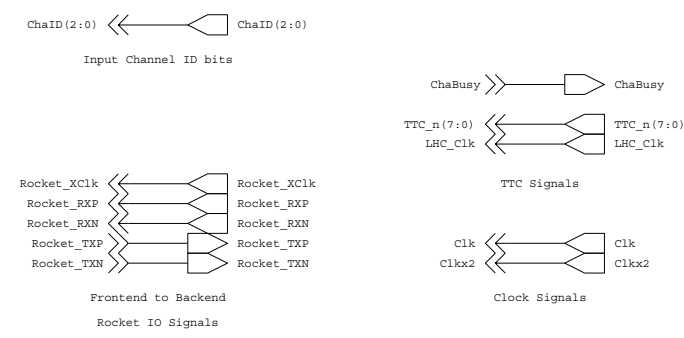
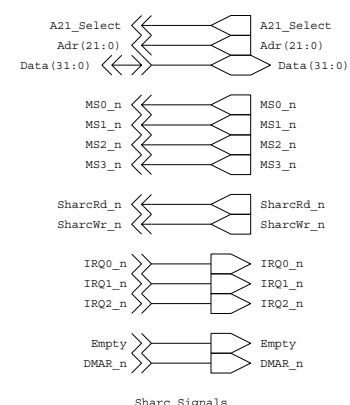
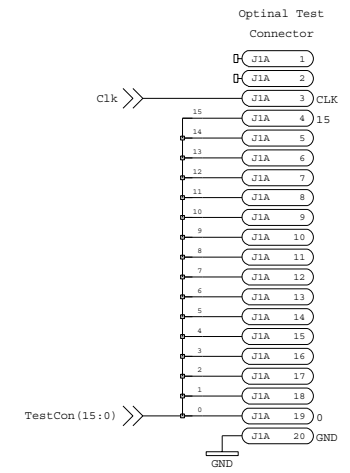
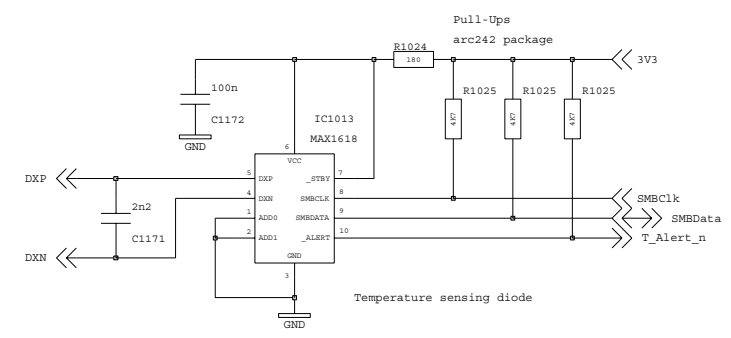
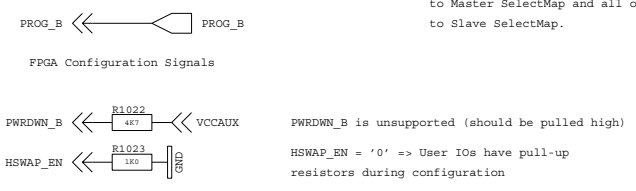
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
Size	A3	4 1 4 A		
Dim	420 x 297 mm			
Page	5 of 6			



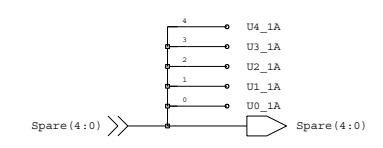
DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices. See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SelectMAP programming Mode -> BUSY. Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!



M2 M1 M0
 0 1 1 Master SelectMAP
 1 1 0 Slave SelectMAP (default)
 1 0 1 Boundary scan
 'On' = '1', 'Off' = '0'
 Default configuration mode will be Slave SelectMAP. It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562. In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.

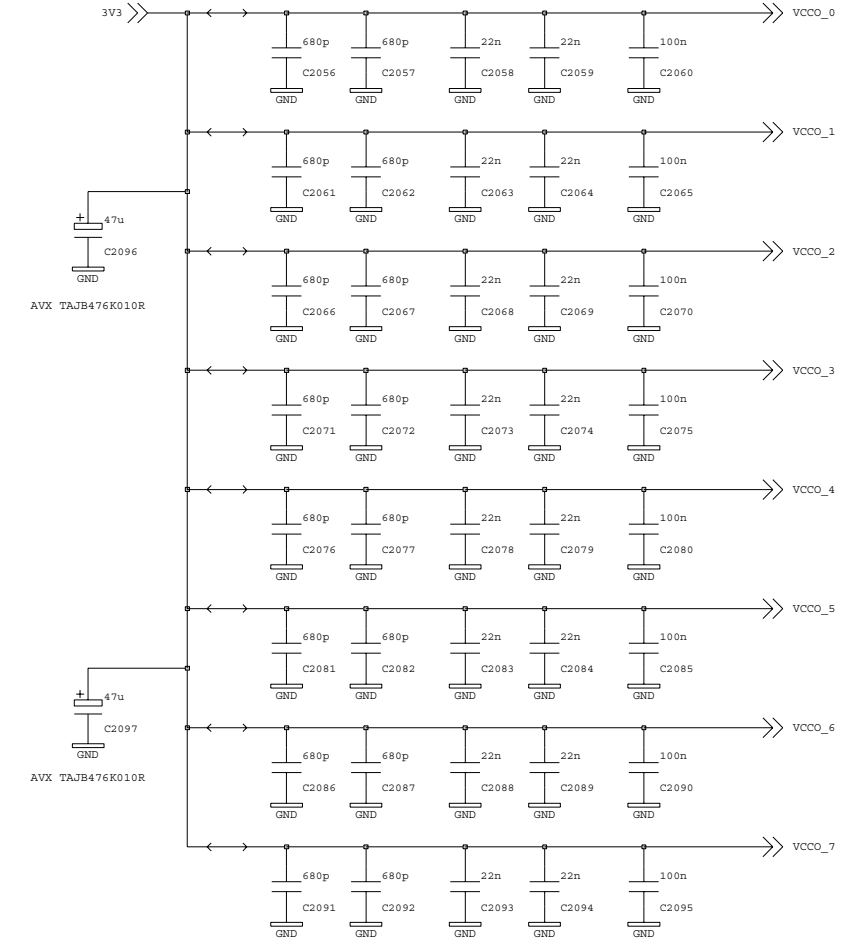
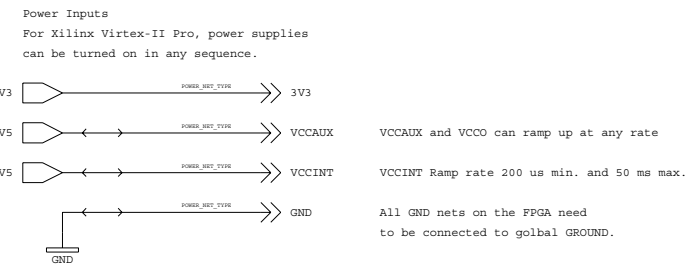
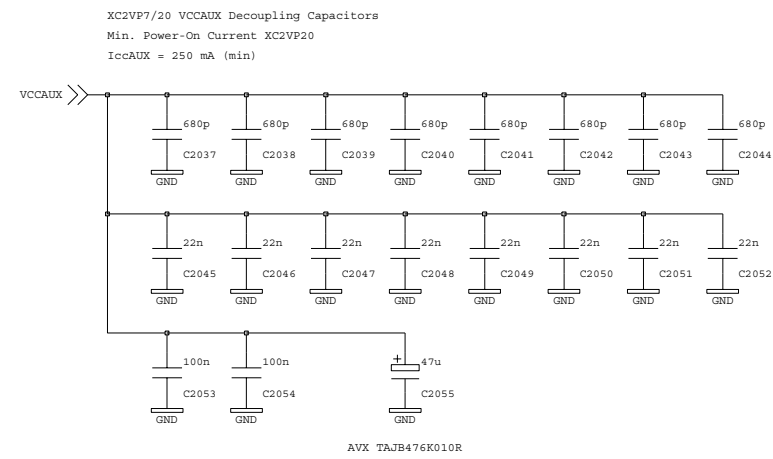
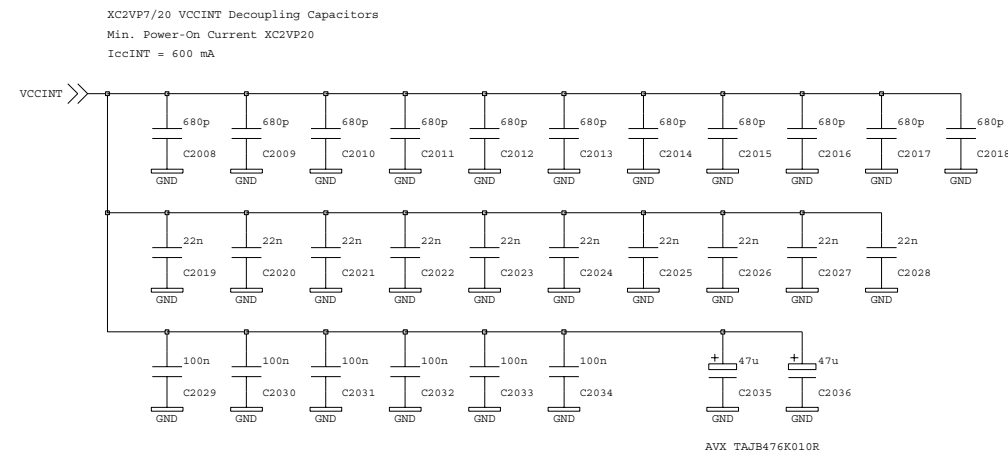


Testpoints force Spare lines to be accessible.



channel_in		Rev	V2	2						
		Date	7 Feb 2006							
Input FPGA Auxiliary Connections										
Proj:	MROD-X	Proj.No:	38405							
Peter Jansweijer		peterj@nikhef.nl								
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOOG ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND			Size	A3	4	1	4	A
					Dim	420 x 297 mm				
					Page	6 of 6				

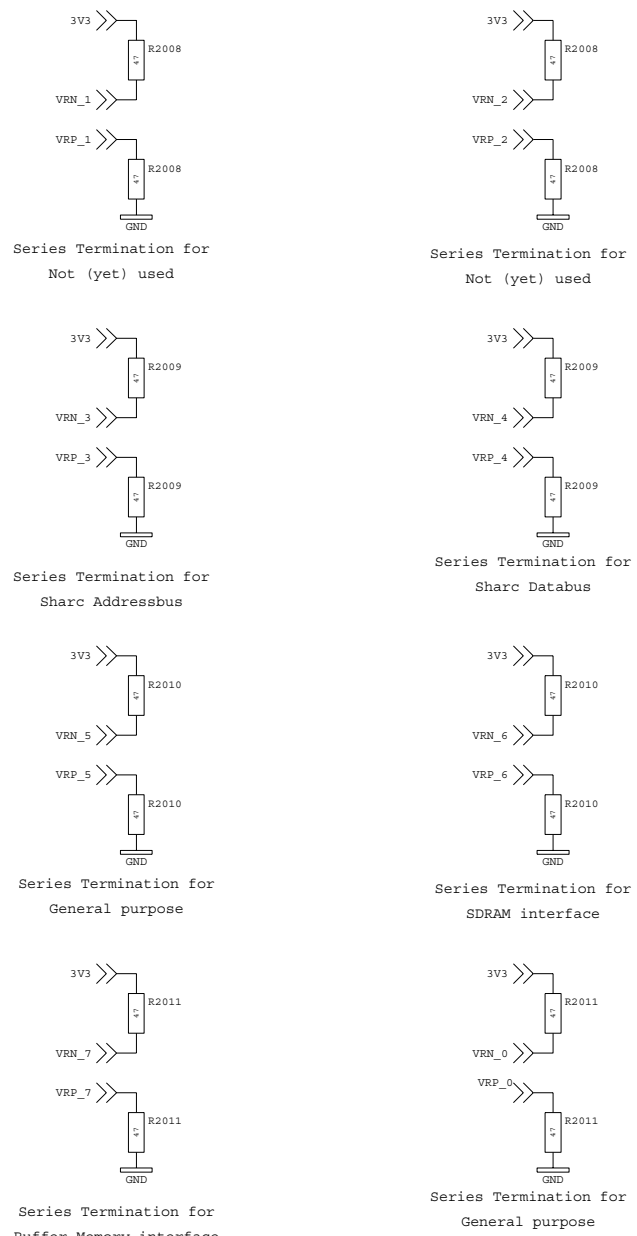
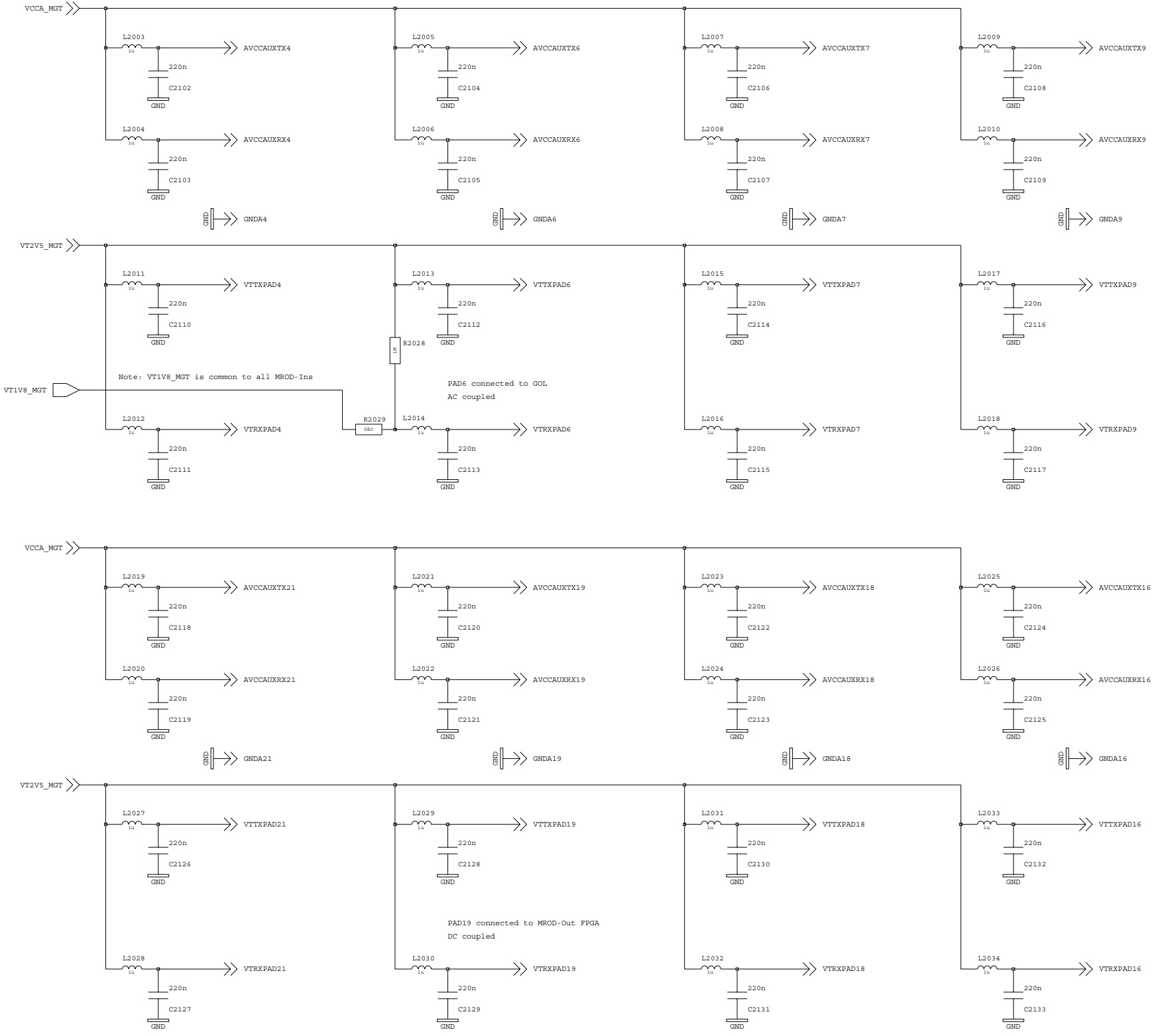
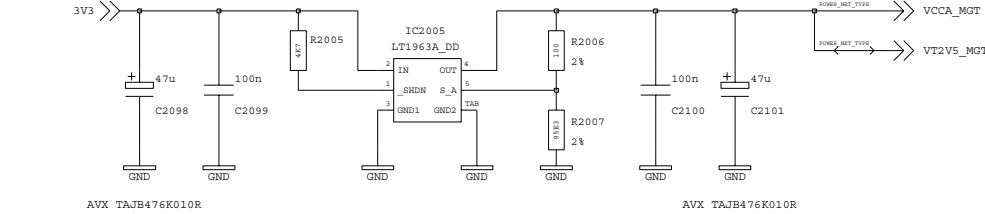
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B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30		
VCCAUX	GND	VRP_2	AVCCAUXK9	VTRXPAD9	AVCCAUXK9	VTRXPAD9									GOL_Xclk	AVCCAUXK6	VTRXPAD6	AVCCAUXK6	VTRXPAD6			LEDn(0)	AVCCAUXK4	VTRXPAD4	AVCCAUXK4	VTRXPAD4	VRN_7	GND	VCCAUX		
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17	C18	C19	C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30		
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		
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J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20	J21	J22	J23	J24	J25	J26	J27	J28	J29	J30		
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K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30		
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R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20	R21	R22	R23	R24	R25	R26	R27	R28	R29	R30		
VCCAUX	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		
S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30		
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MS0_n	MS0_n	MS1_n	MS2_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n	MS3_n		
Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15	Y16	Y17	Y18	Y19	Y20	Y21	Y22	Y23	Y24	Y25	Y26	Y27	Y28	Y29	Y30		
Adr(17)	Adr(18)	GND	Adr(19)	Adr(20)	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		
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Adr(11)	Adr(12)	Adr(13)	Adr(14)	Adr(15)	Adr(16)	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		
AB1	AB2	AB3	AB4	AB5	AB6	AB7	AB8	AB9	AB10	AB11	AB12	AB13	AB14	AB15	AB16	AB17	AB18	AB19	AB20	AB21	AB22	AB23	AB24	AB25	AB26	AB27	AB28	AB29	AB30		
Adr(7)	Adr(8)	Adr(9)	Adr(10)	VCCO_3	VCCO_4	VCCO_4	VCCO_4	VCCO_3	VCCO_3	Data(3)	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5			
AC1	AC2	AC3	AC4	AC5	AC6	AC7	AC8	AC9	AC10	AC11	AC12	AC13	AC14	AC15	AC16	AC17	AC18	AC19	AC20	AC21	AC22	AC23	AC24	AC25	AC26	AC27	AC28	AC29	AC30		
GND	Adr(4)	Adr(5)	Adr(6)	GND	CCLK	DONE	DO	Data(16)	Data(11)	Data(9)	Data(9)	Data(7)	Data(1)	Data(1)	Data(2)	IRQ_n	TestCon(6)	TestCon(9)	TestCon(10)	CD2	M2	M1	M1	AC25	AC26	AC27	AC28	AC29	AC30		
AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	AD13	AD14	AD15	AD16	AD17	AD18	AD19	AD20	AD21	AD22	AD23	AD24	AD25	AD26	AD27	AD28	AD29	AD30		
GND	GND	GND	GND	GND	Adr(2)	Adr(3)	PWRDN_B	D1	Data(15)	Data(10)	Data(8)	Data(4)	Data(4)	Data(1)	IRQ_n	TestCon(11)	TestCon(12)	TestCon(13)	D6	D6	M6	SDRAM_DQ(8)	SDRAM_DQ(8)	SDRAM_DQ(8)	SDRAM_DQ(8)	SDRAM_DQ(8)	SDRAM_DQ(8)	SDRAM_DQ(8)			
AE1	AE2	AE3	AE4	AE5	AE6	AE7	AE8	AE9	AE10	AE11	AE12	AE13	AE14	AE15	AE16	AE17	AE18	AE19	AE20	AE21	AE22	AE23	AE24	AE25	AE26	AE27	AE28	AE29	AE30		
GND	GND	GND	GND	GND	GND	Data(25)	Data(24)	Data(20)	Data(14)	Data(14)	Data(11)	Data(9)	Data(8)	Data(6)	Data(6)	Data(0)	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		
AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	AF16	AF17	AF18	AF19	AF20	AF21	AF22	AF23	AF24	AF25	AF26	AF27	AF28	AF29	AF30		
GND	GND	GND	GND	GND	GND	INIT_B	Data(23)	Data(19)	Data(13)	GND	GND	GND	Data(5)	SDRAM_CLKin	SDRAM_CLK	GND	GND	GND	GND	GND	GND	TTC_n(7)	TTC_n(6)	TTC_n(4)	EDWR_B	AF25	AF26	AF27	AF28	AF29	AF30
AG1	AG2	AG3	AG4	AG5	AG6	AG7	AG8	AG9	AG10	AG11	AG12	AG13	AG14	AG15	AG16	AG17	AG18	AG19	AG20	AG21	AG22	AG23	AG24	AG25	AG26	AG27	AG28	AG29	AG30		
Data(30)	Data(31)	Adr(0)	GND	Adr(1)	DOU7	D2	VRP_4	GND	Data(12)	GND	GND	Data(4)	Data(4)	ShareM_n	LHC_Clk	ChaBusy	GND	GND	GND	GND	GND	TTC_n(5)	GND	VRN_5	D5	CS_B	SDRAM_DQ(13)	GND	SDRAM_DQ(12)</		



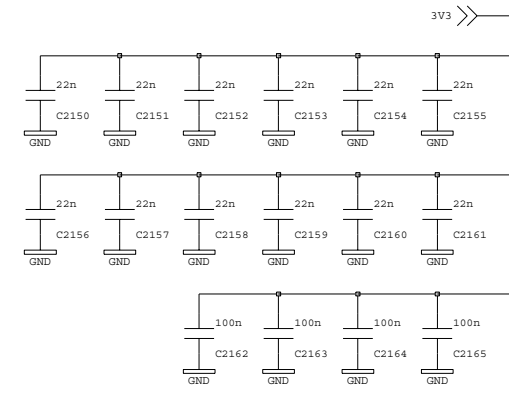
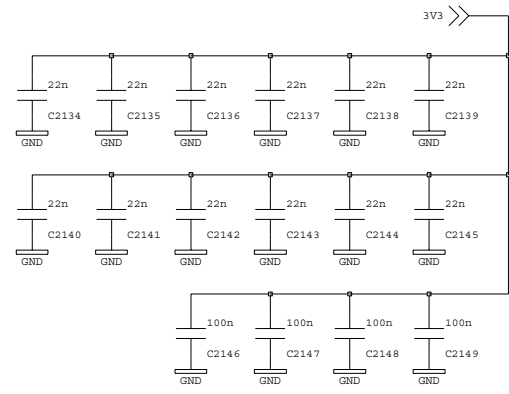
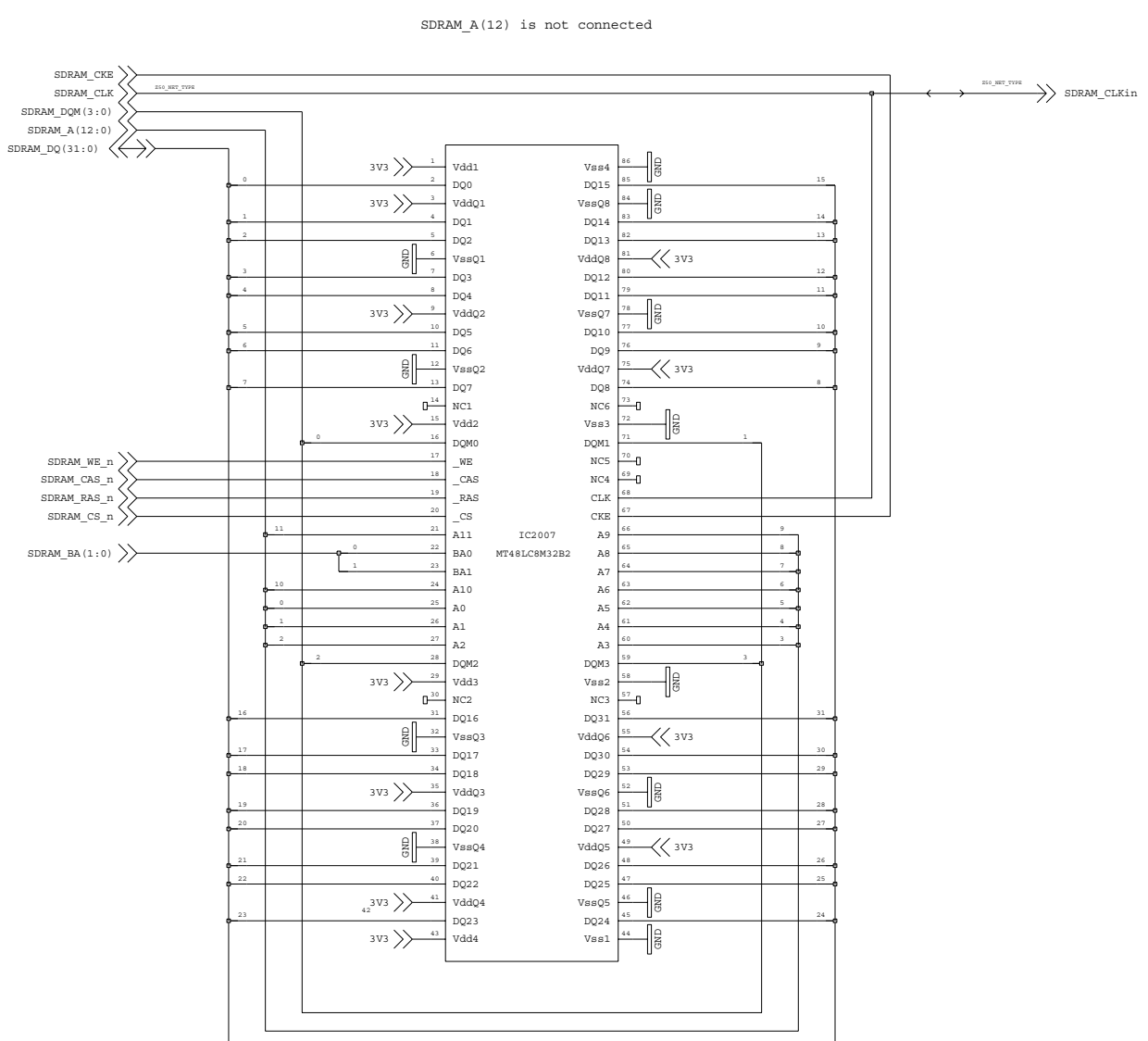
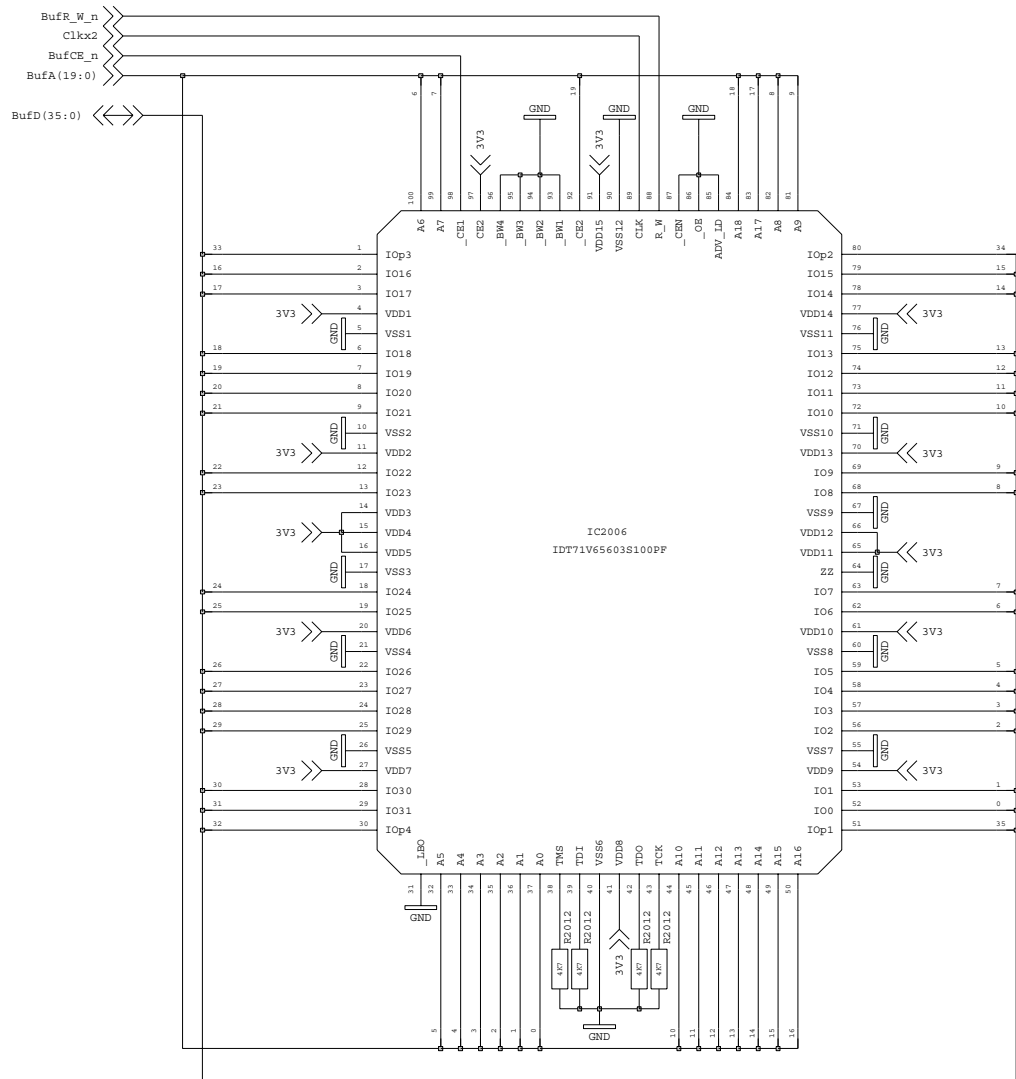
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		Date	7 Feb 2006				
Input FPGA Power Supply Decoupling		Time	1:51:34 pm				
Proj:	MROD-X	Proj.No:	38405				
Peter Jansweijer		peterj@nikhef.nl					
NIKHEF <small>© ET-Nikhef Amsterdam</small>		<small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>					
					Size	A3	4 1 4 A
					Dim	420 x 297 mm	
		Page	3	of 6			

2V5 @ 1,5A

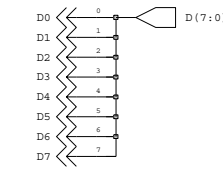
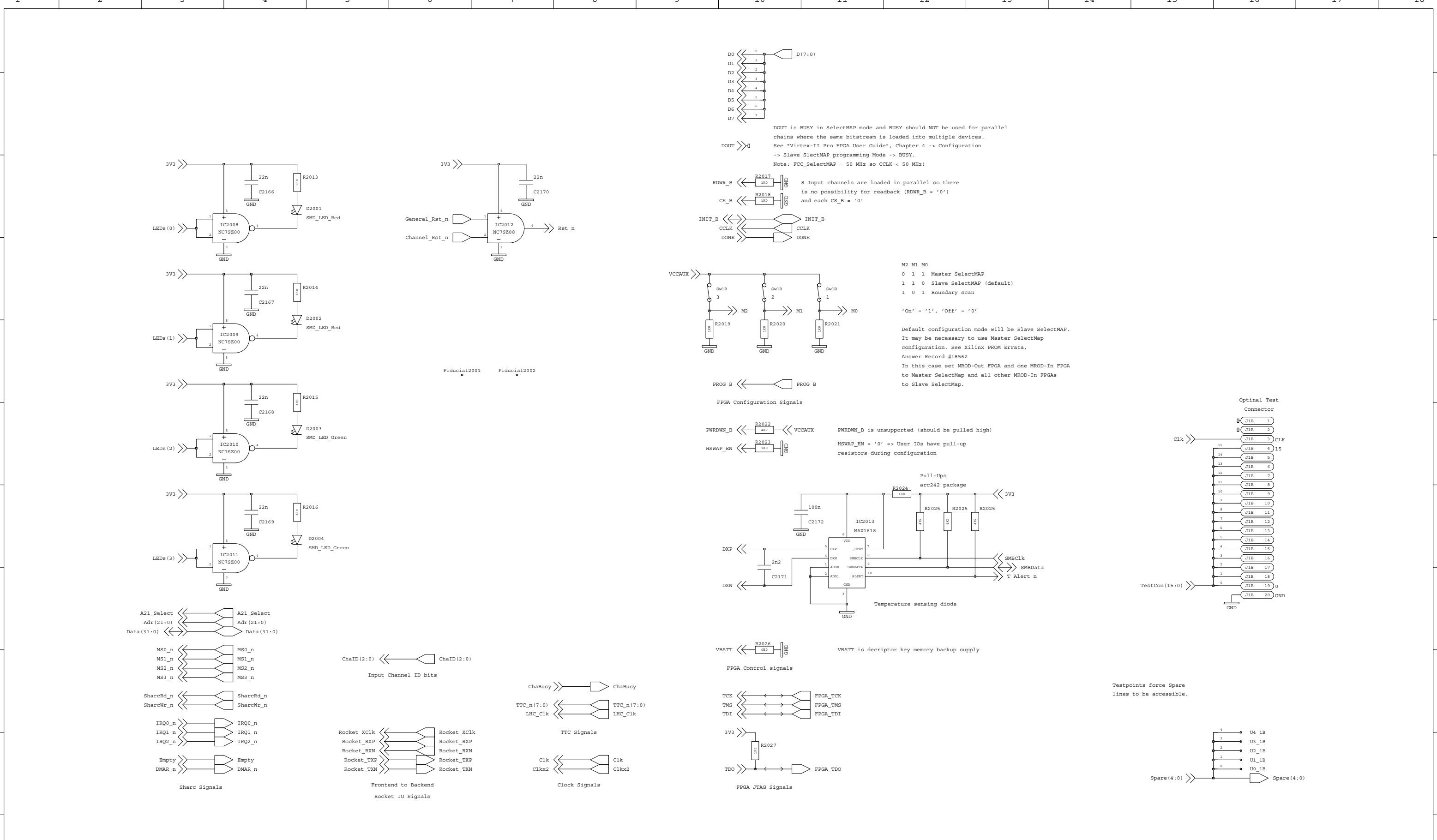
=> MGT Power (estimated 31 + 49 = 80 mA)
=> MGT TX (RX) Termination (estimated 11 mA)



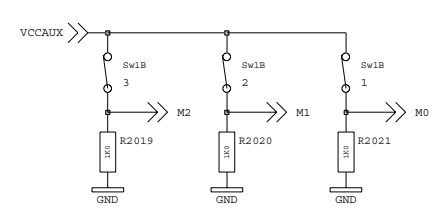
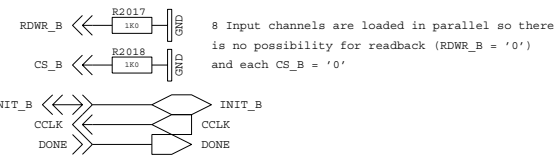
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination			Time	1:52:01 pm
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © NIKHEF Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	4	of 6



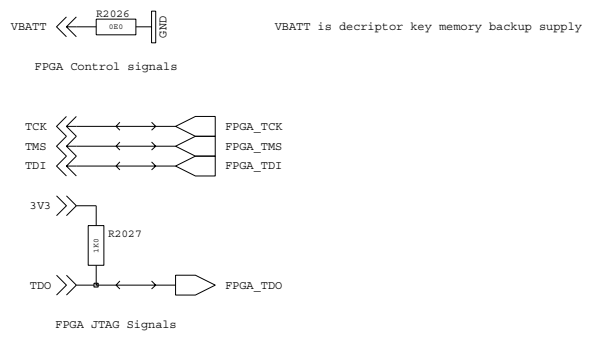
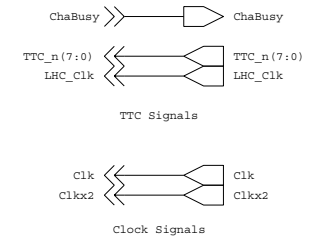
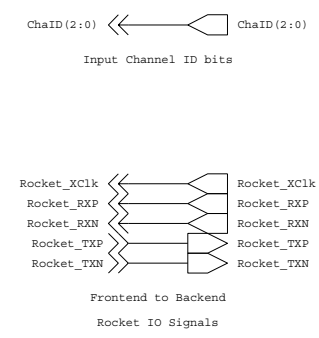
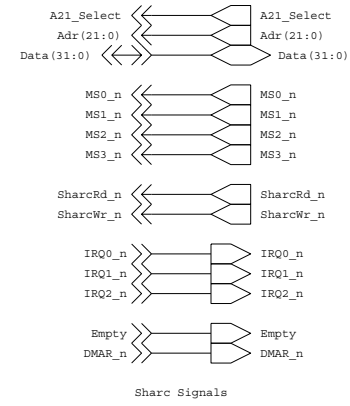
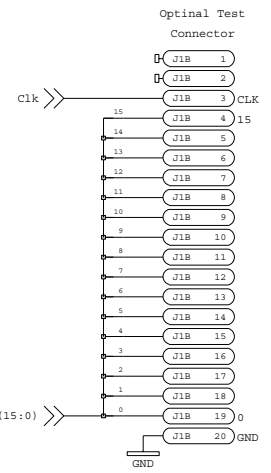
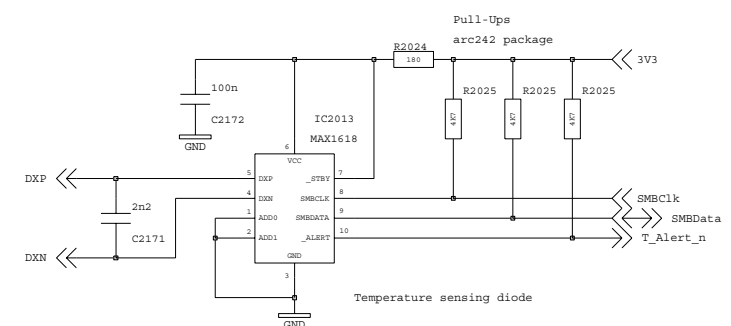
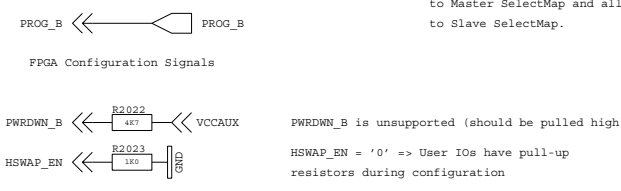
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
Size	A3	4 1 4 A		
Dim	420 x 297 mm			
Page	5 of 6			



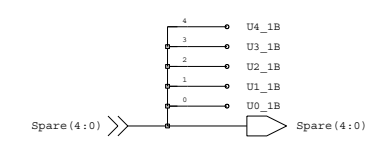
DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices. See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SelectMAP programming Mode -> BUSY. Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!



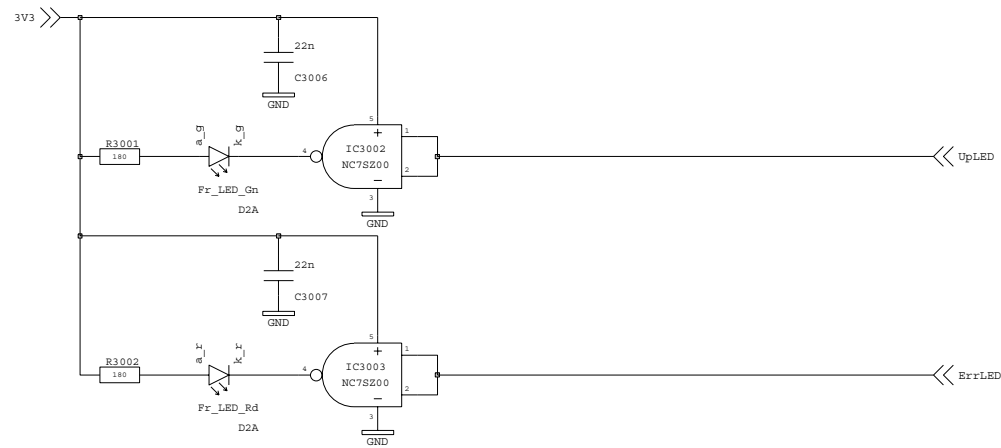
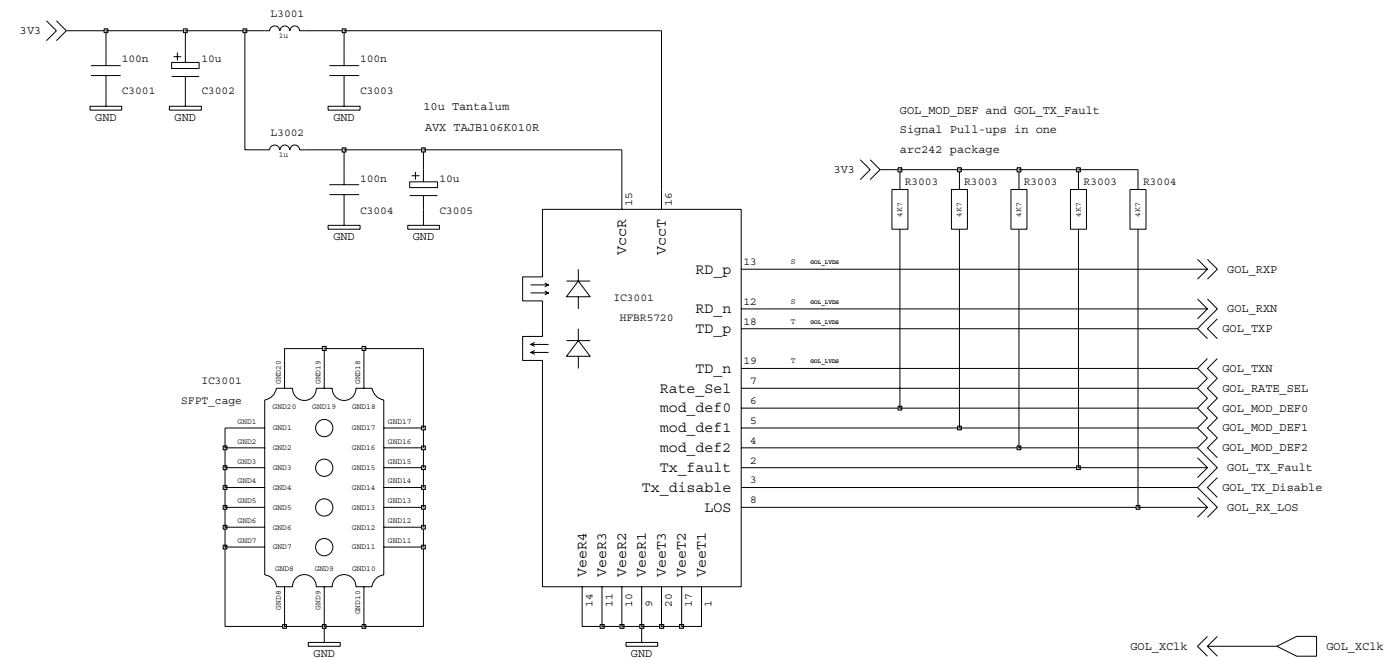
M2 M1 M0
 0 1 1 Master SelectMAP
 1 1 0 Slave SelectMAP (default)
 1 0 1 Boundary scan
 'On' = '1', 'Off' = '0'
 Default configuration mode will be Slave SelectMAP. It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562. In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.



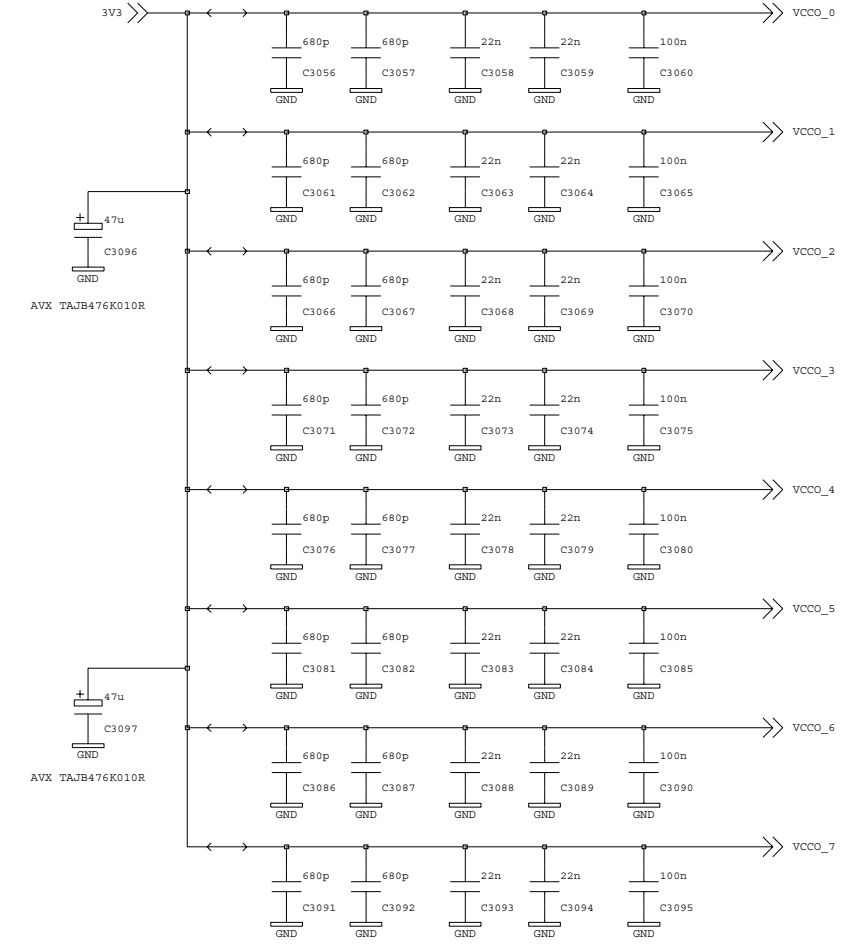
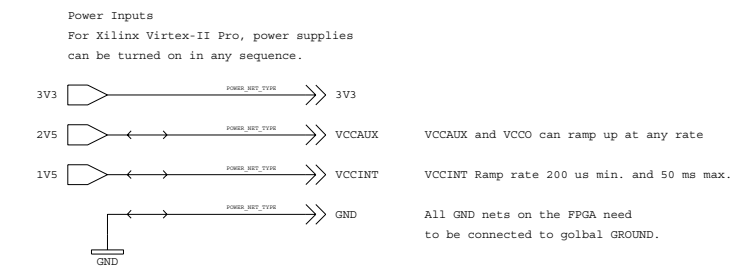
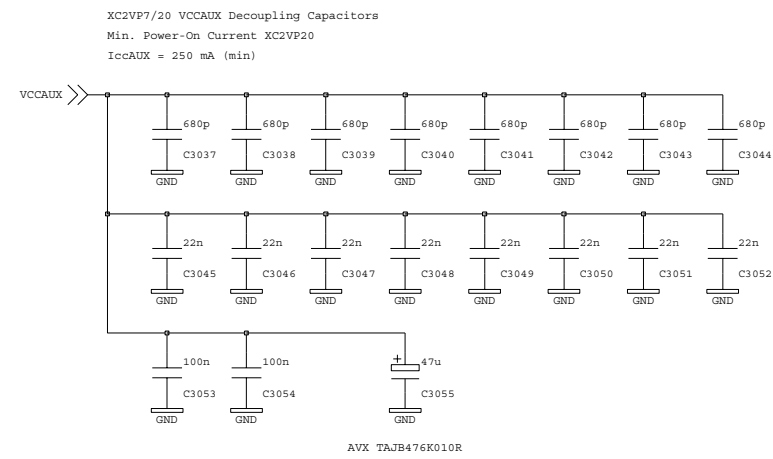
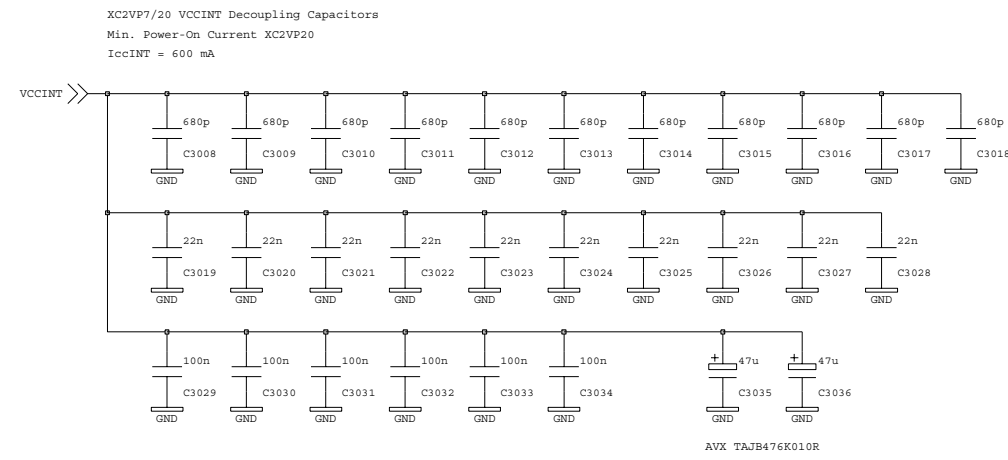
Testpoints force Spare lines to be accessible.



channel_in		Rev	V2	2						
		Date	7 Feb 2006							
Input FPGA Auxiliary Connections		Proj:	MROD-X	Proj.No:	38405					
Peter Jansweijer		peterj@nikhef.nl								
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND			Size	A3	4	1	4	A
		Dim	420 x 297 mm							
		Page	6 of 6							



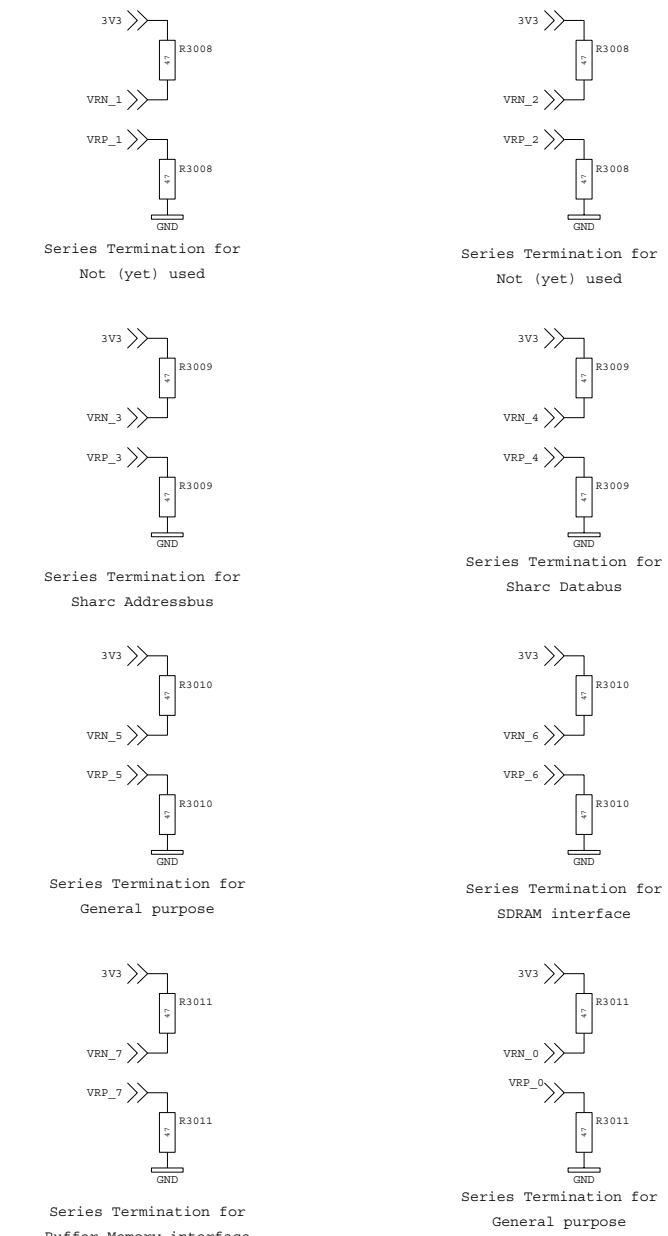
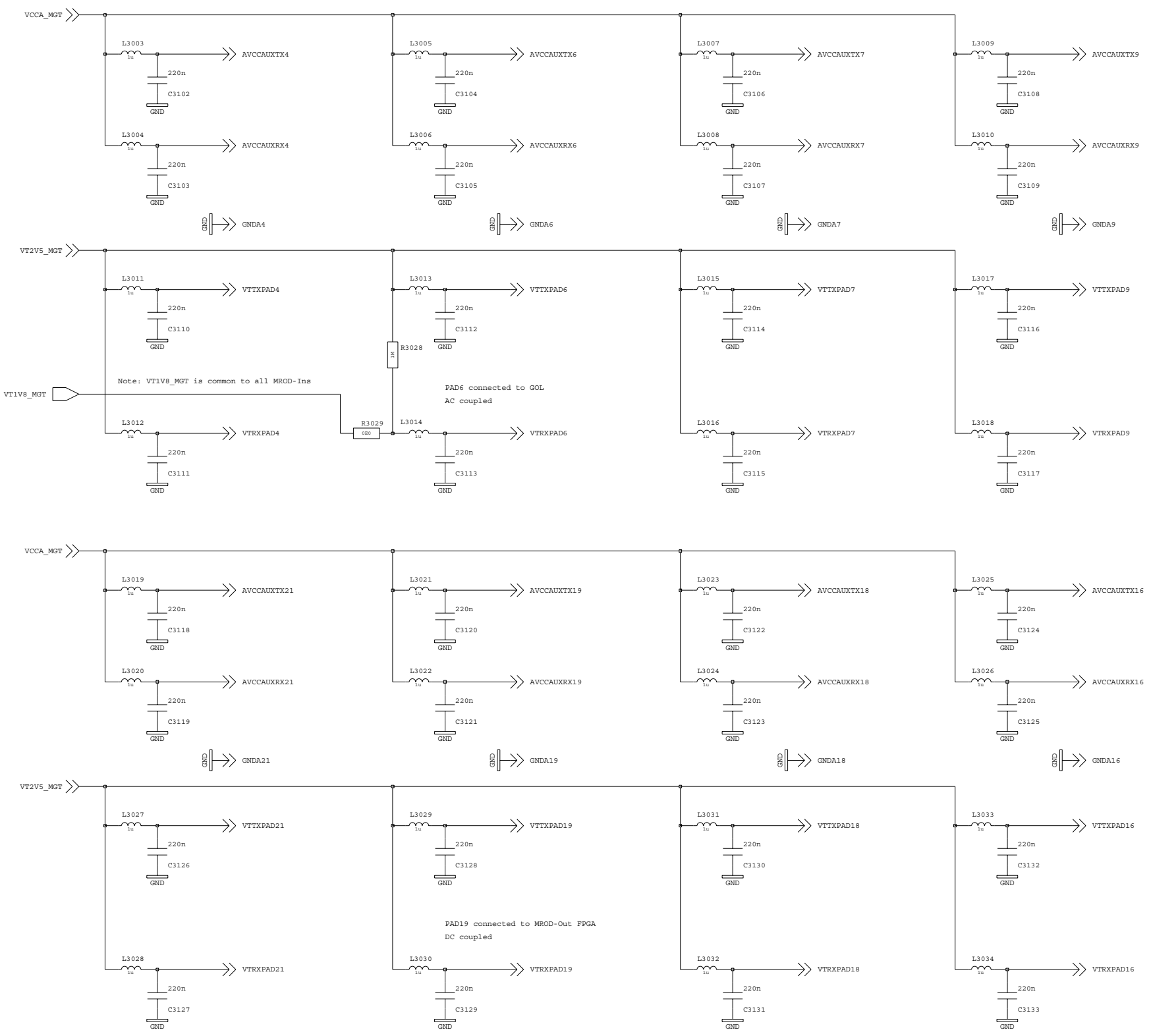
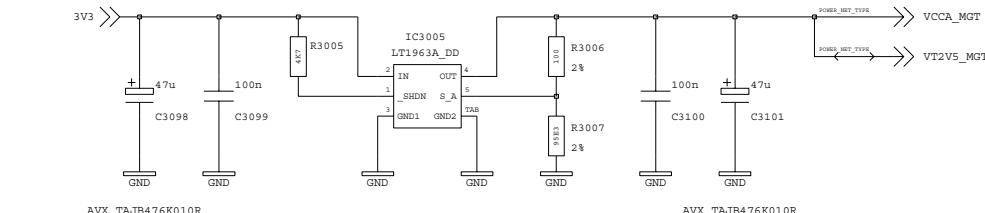
channel_in		Rev	V2	2
GOL Input		Date	7 Feb 2006	
Proj: MROD-X		Proj.No:	38405	
Peter Jansweijer		Name	tonvr	
NIKHEF		Size	A3	4 1 4 A
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Dim	420 x 297 mm	
© ET-Nikhef Amsterdam		Page	1 of 6	



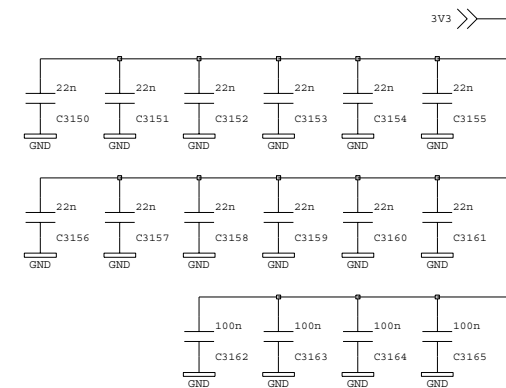
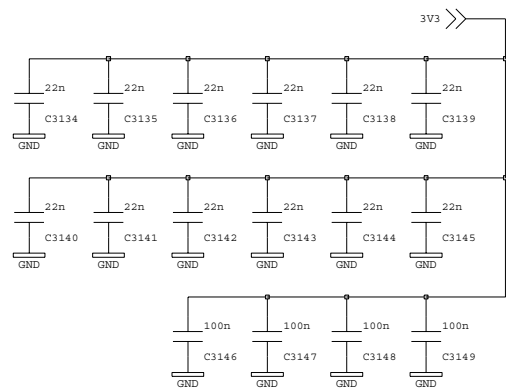
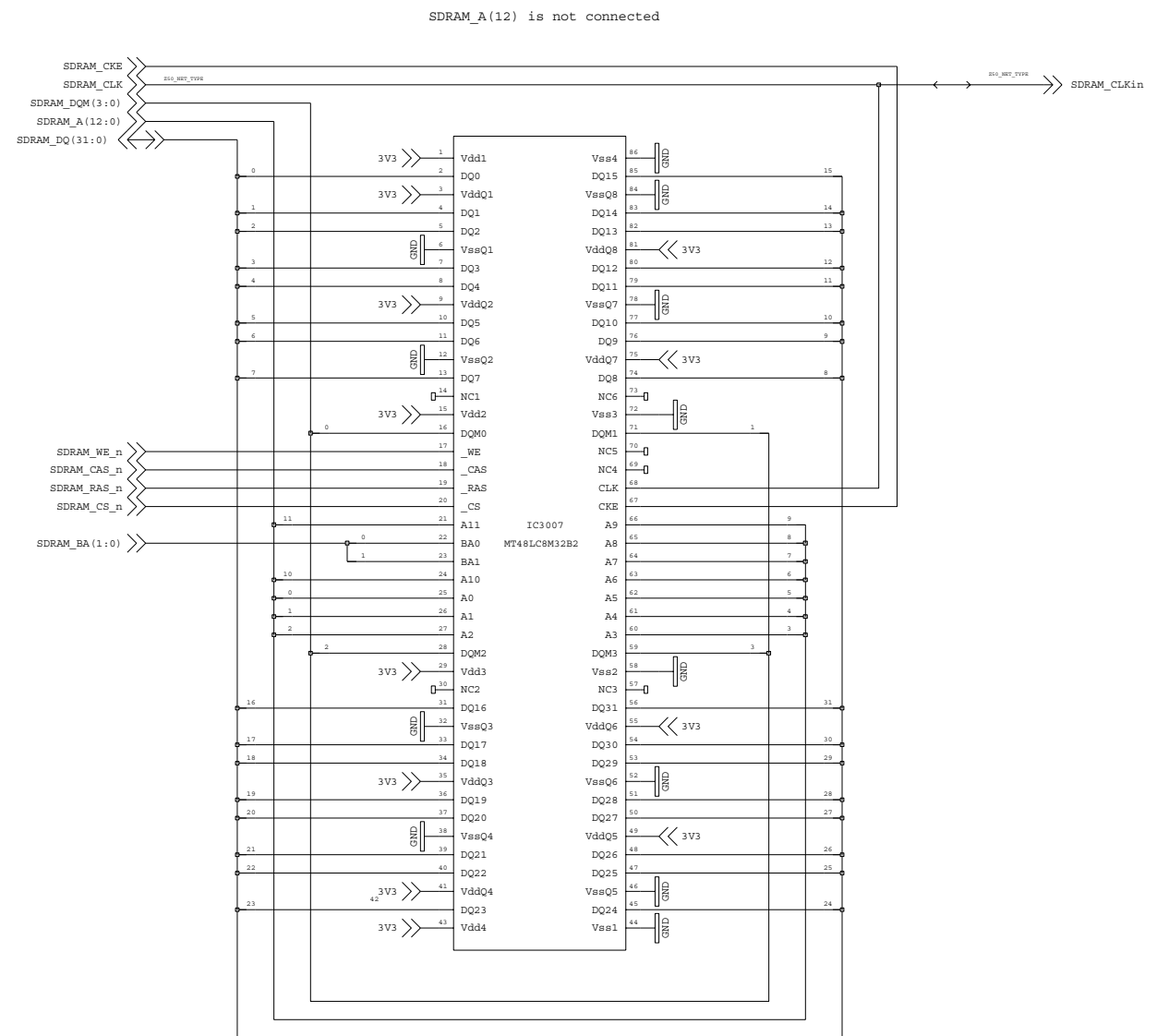
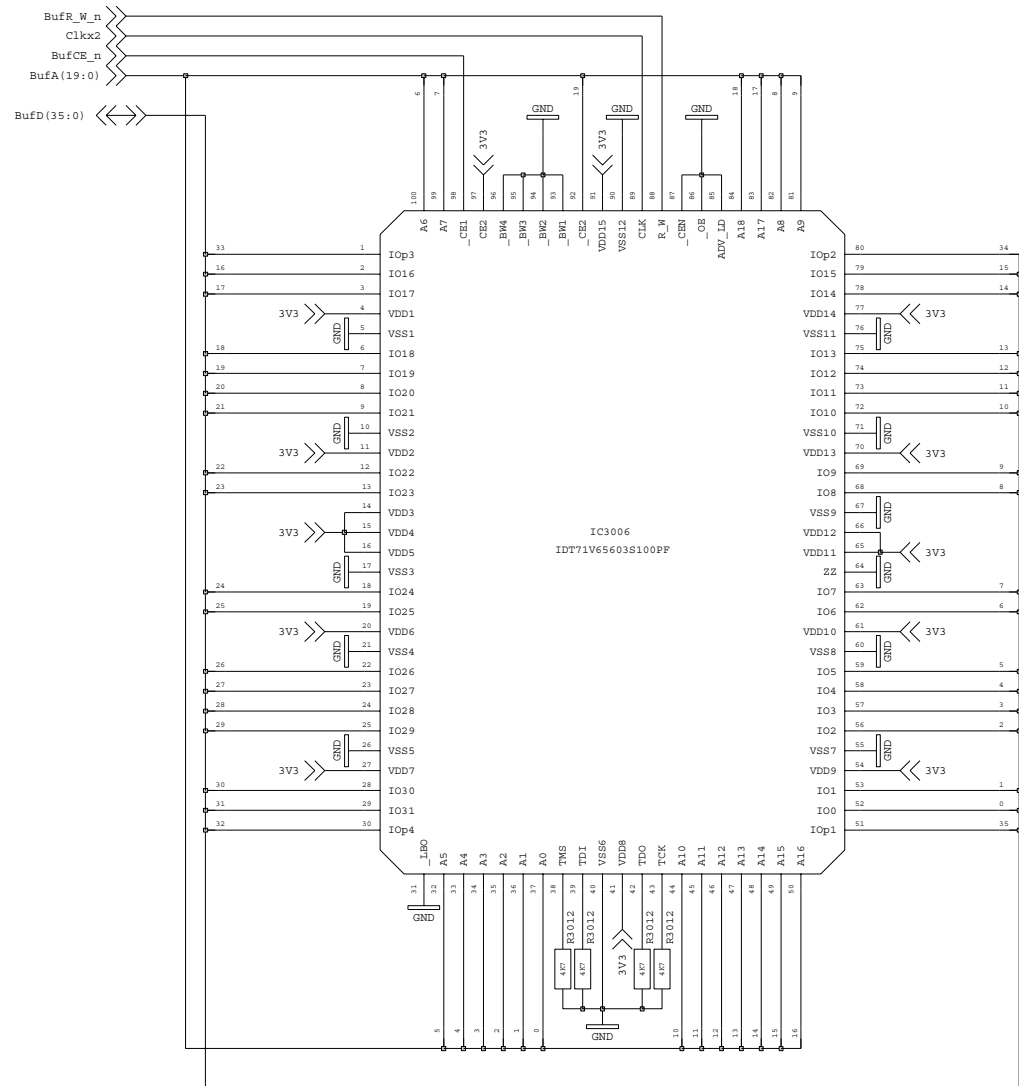
channel_in		Rev	V2	2			
		Date	7 Feb 2006				
Input FPGA Power Supply Decoupling		Time	1:51:34 pm				
Proj:	MROD-X	Proj.No:	38405				
Peter Jansweijer		peterj@nikhef.nl					
NIKHEF <small>© ET-Nikhef Amsterdam</small>		<small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>					
					Size	A3	4 1 4 A
					Dim	420 x 297 mm	
		Page	3	of 6			

2V5 @ 1,5A

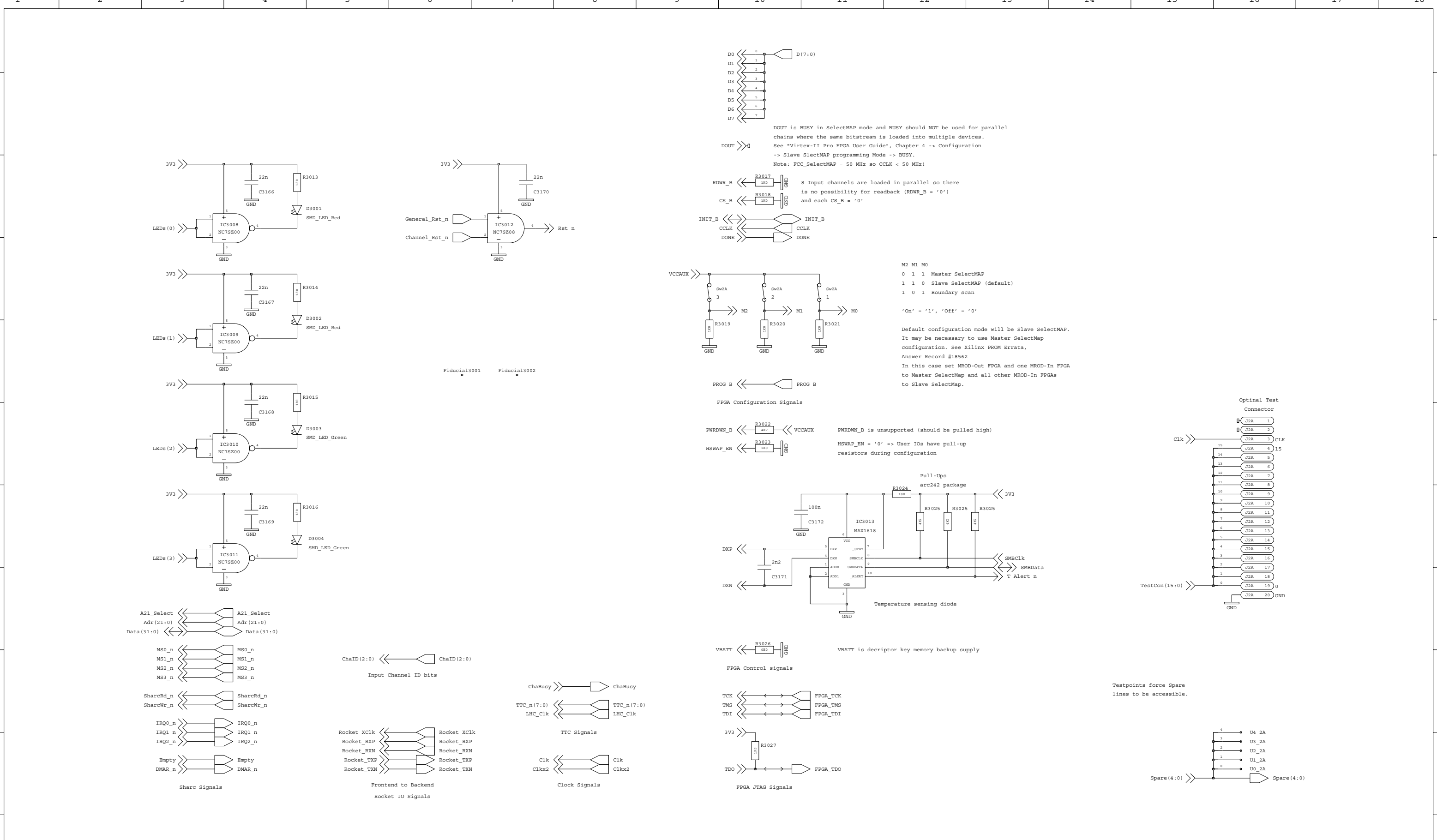
=> MGT Power (estimated 31 + 49 = 80 mA)
=> MGT TX (RX) Termination (estimated 11 mA)



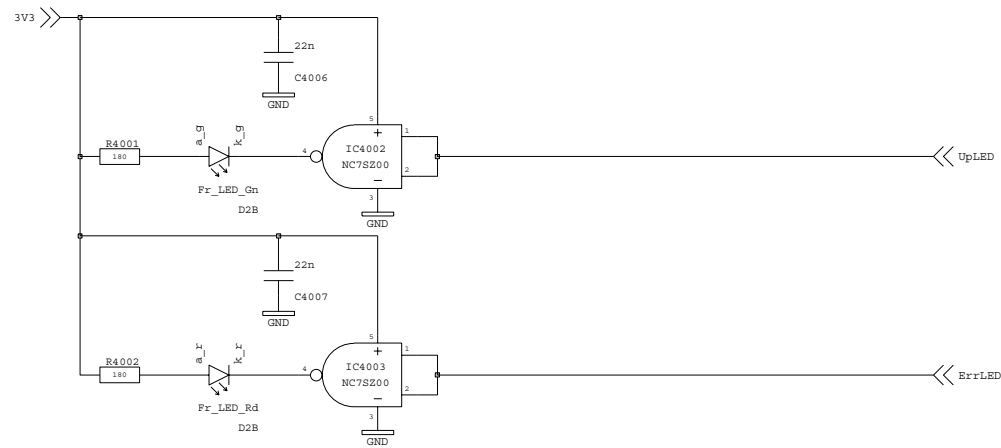
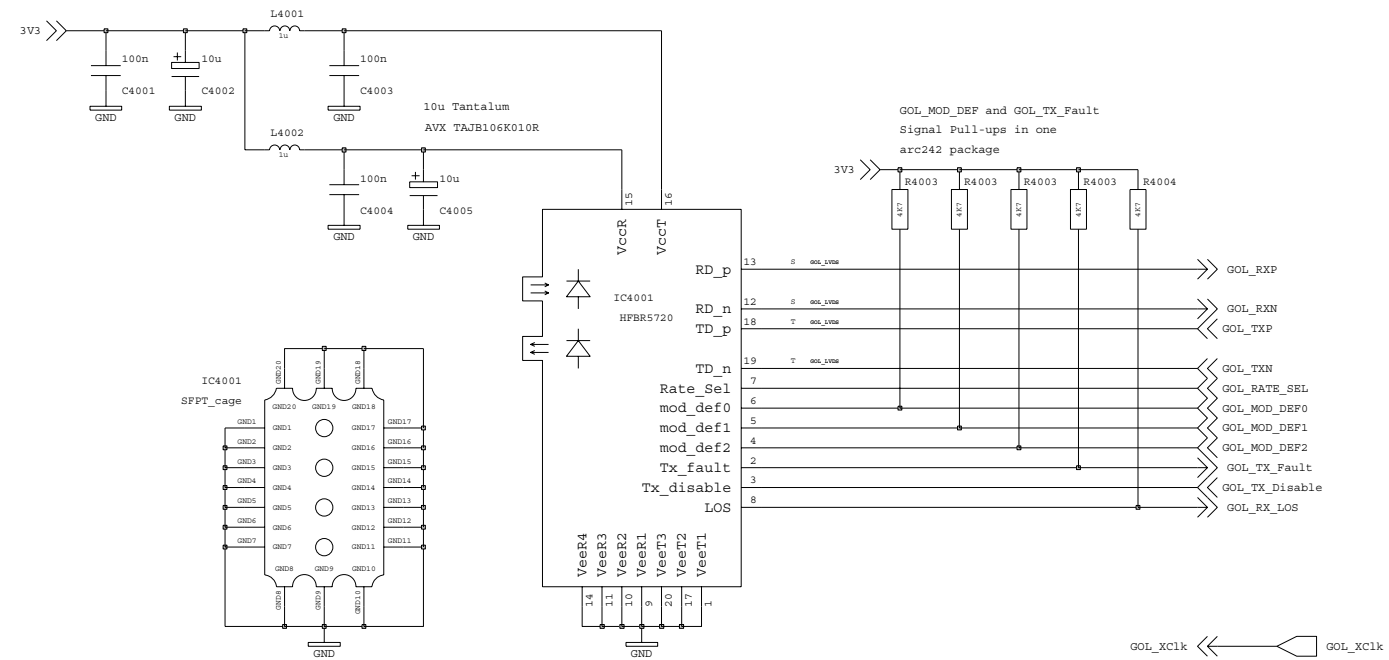
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time	1:52:01 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © NIKHEF Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	4 of 6	



channel_in		Rev	V2	2	
		Date	7 Feb 2006		
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm		
Proj:	MROD-X	Proj.No:	38405	Name	Ton van Reen
Peter Jansweijer		peterj@nikhef.nl			
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Size	A3	4 1 4 A	
		Dim	420 x 297 mm		
		Page	5	of 6	

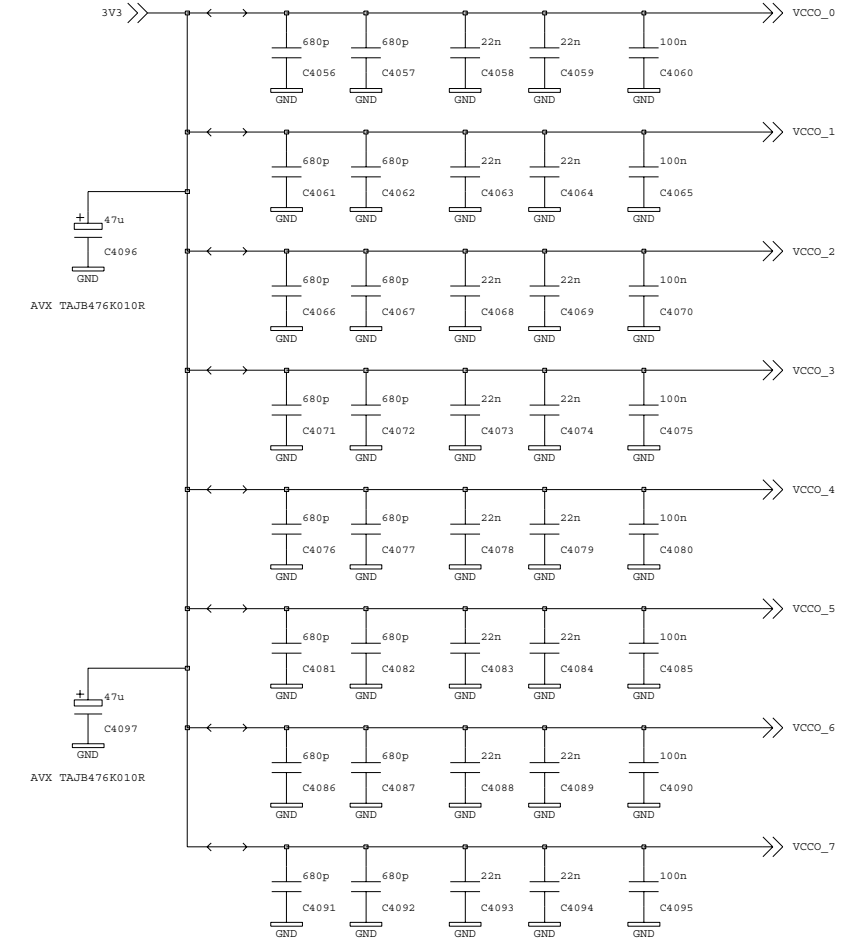
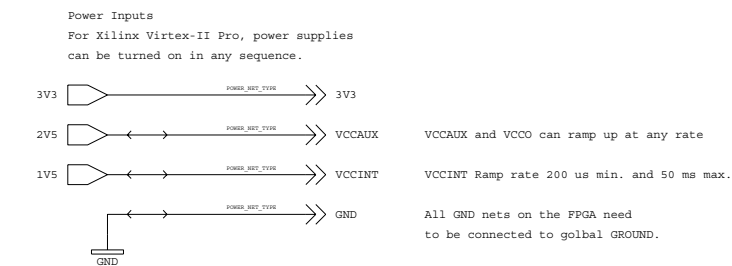
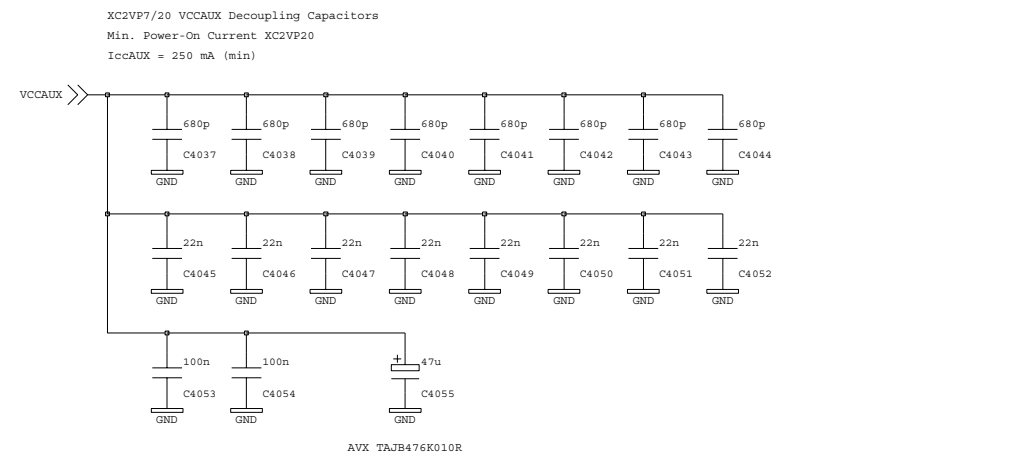
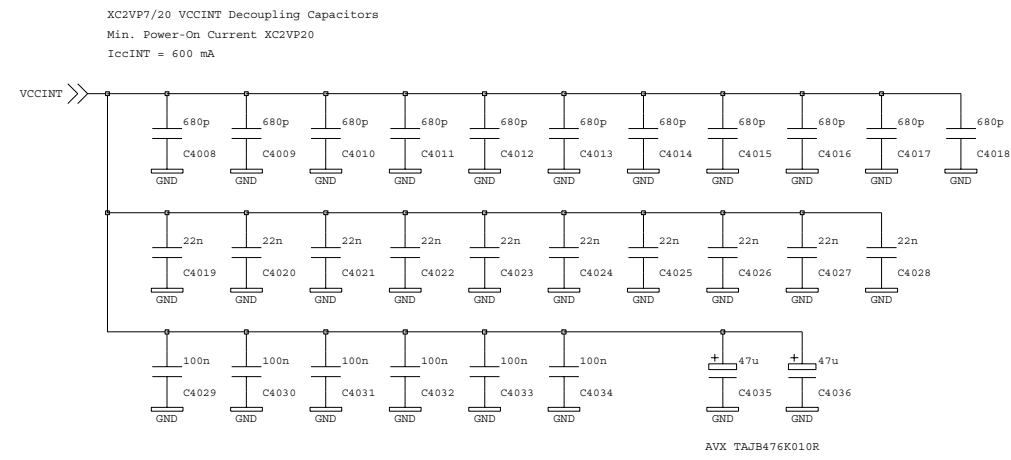


channel_in		Rev	V2 2
Input FPGA Auxiliary Connections		Date	7 Feb 2006
Proj: MROD-X	Proj.No: 38405	Time	1:53:04 pm
Peter Jansweijer peterj@nikhef.nl		Name	Ton van Reen
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOOG ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Size	A3 4 1 4 A
		Dim	420 x 297 mm
		Page	6 of 6

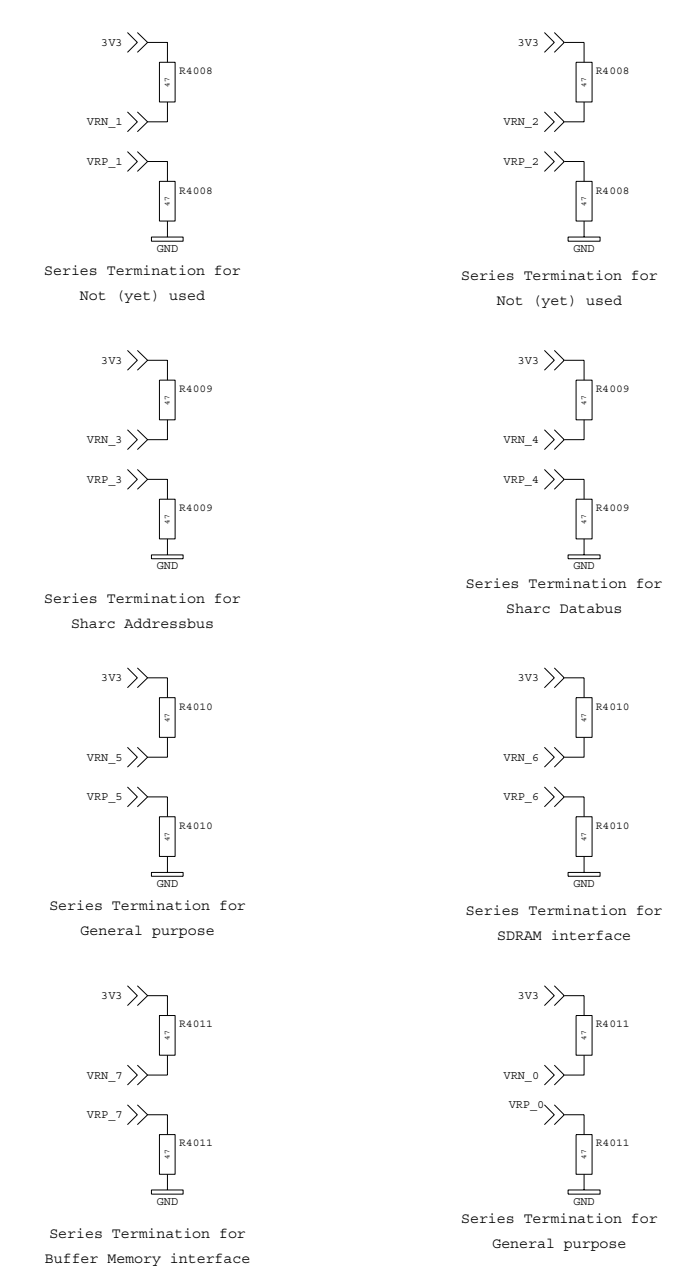
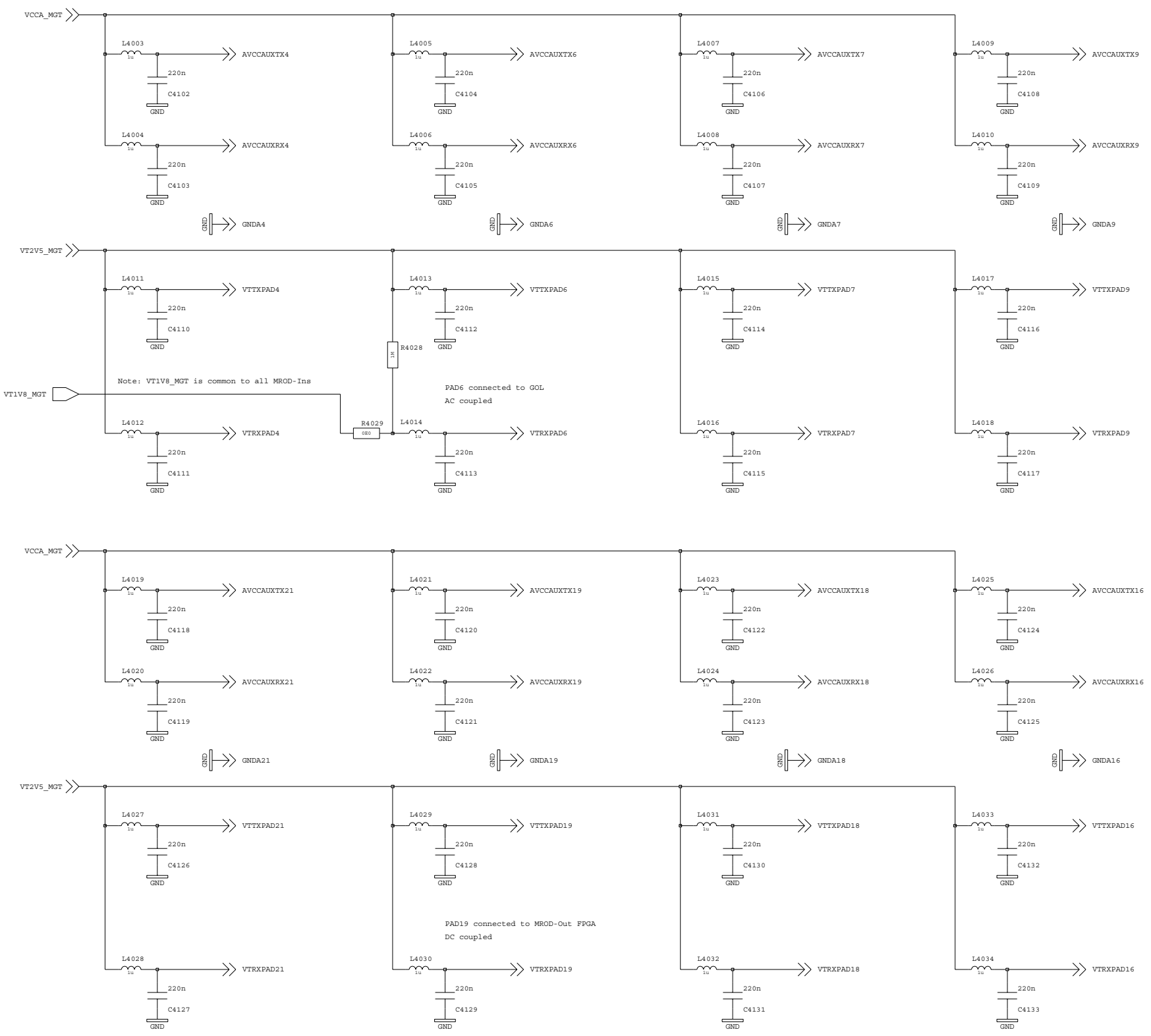
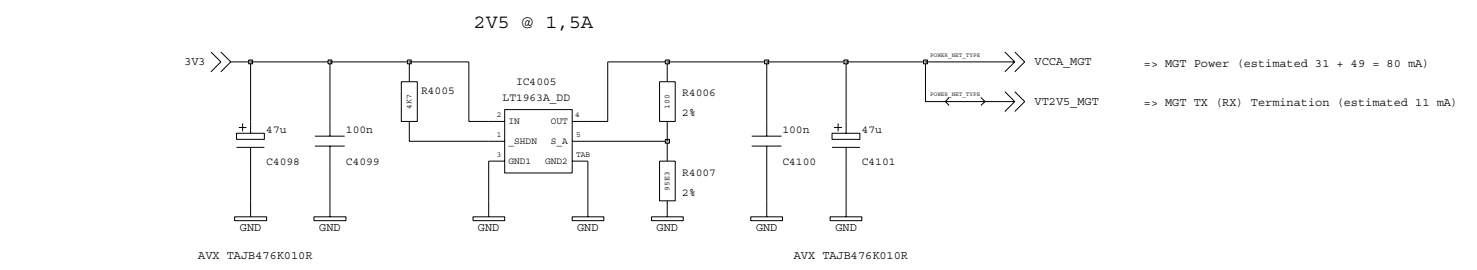


channel_in		Rev	V2	2	
		Date	7 Feb 2006		
GOL Input		Time	1:50:33 pm		
Proj:	MROD-X	Proj.No:	38405		
Peter Jansweijer		peterj@nikhef.nl			
NIKHEF © ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size	A3	4 1 4 A
			Dim	420 x 297 mm	
			Page	1 of 6	

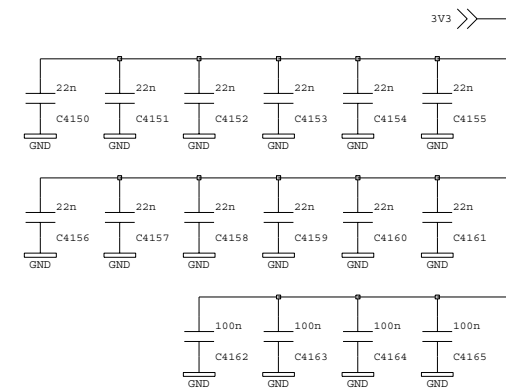
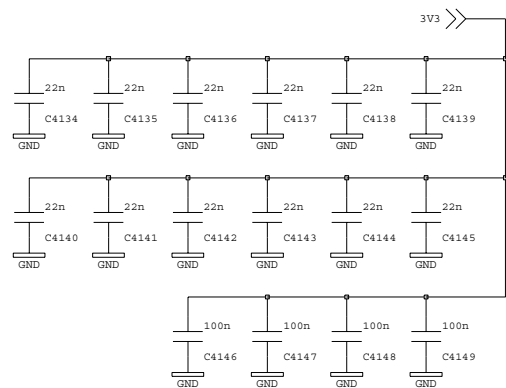
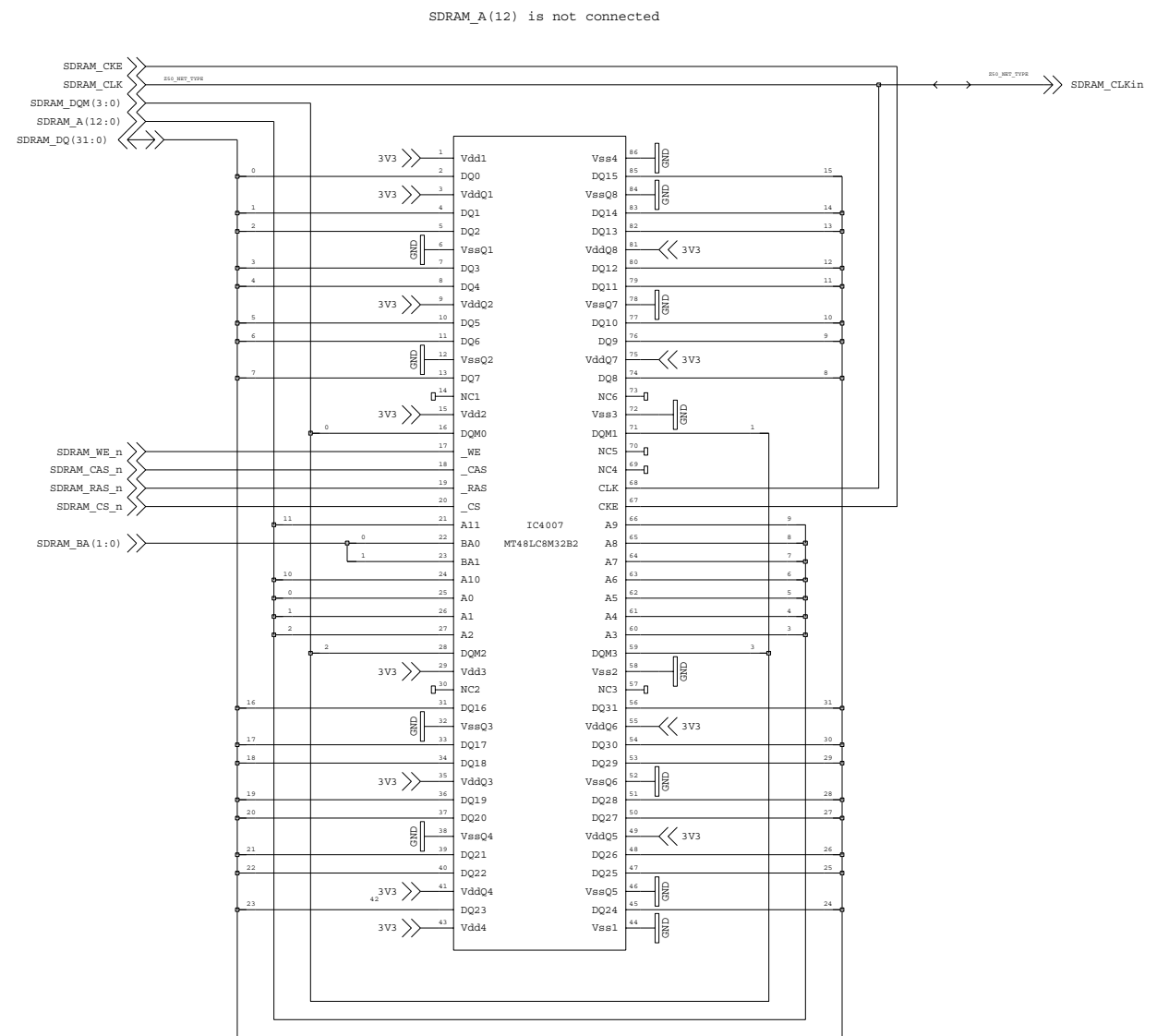
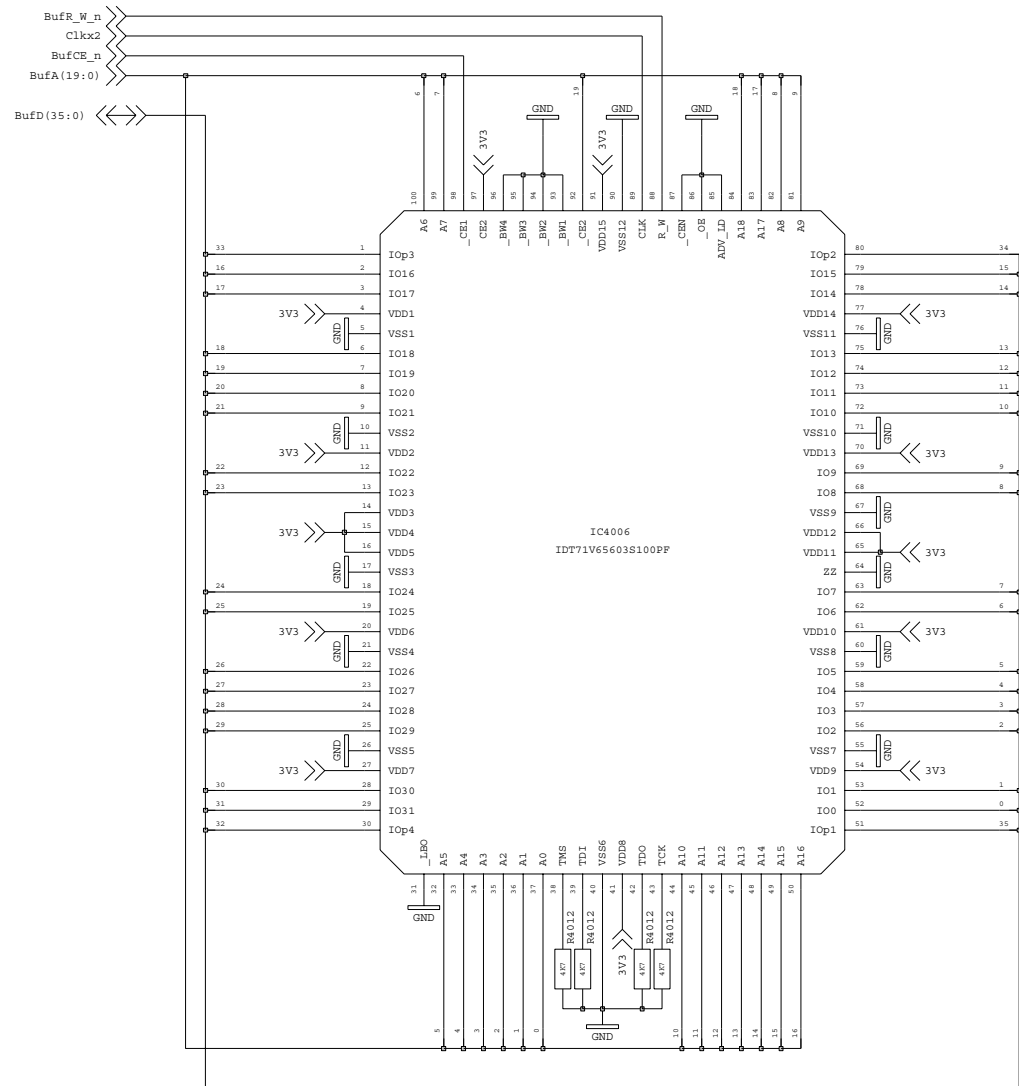
IC4004 XC2VP7FF896		A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																								
B1	VCCAUX	B2	VRP_2	B4	AVCCAUXK9	B6	VTRXPAD9	B8	GND	B10	AVCCAUXK7	B12	AVCCAUXK7	B14	VCCAUX	B16	GOL_RXN	B18	GOL_RKP	B19	GOL_TXP	B20	GOL_TXN	B21	GND	B22	LEDn(0)	B24	VRP_7	B28	VCCAUX	B30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
C1	GND	C2	VRN_2	C4	AVCCAUXK9	C6	VTRXPAD9	C8	GND	C10	AVCCAUXK7	C12	AVCCAUXK7	C14	GND	C16	GOL_Xclk	C18	VTRXPAD6	C19	AVCCAUXK6	C20	VTRXPAD6	C21	GND	C22	LEDn(1)	C24	VRN_7	C28	GND	C30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
D1	GND	D2	VRN_2	D4	AVCCAUXK9	D6	VTRXPAD9	D8	GND	D10	AVCCAUXK7	D12	AVCCAUXK7	D14	GND	D16	GOL_Xclk	D18	VTRXPAD6	D19	AVCCAUXK6	D20	VTRXPAD6	D21	GND	D22	LEDn(2)	D24	VRN_7	D28	GND	D30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
E1	GND	E2	VRN_1	E4	AVCCAUXK9	E6	VTRXPAD9	E8	GND	E10	AVCCAUXK7	E12	AVCCAUXK7	E14	GND	E16	GOL_Xclk	E18	VTRXPAD6	E19	AVCCAUXK6	E20	VTRXPAD6	E21	GND	E22	LEDn(3)	E24	VRN_7	E28	GND	E30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
F1	GND	F2	VRN_1	F4	AVCCAUXK9	F6	VTRXPAD9	F8	GND	F10	AVCCAUXK7	F12	AVCCAUXK7	F14	GND	F16	GOL_Xclk	F18	VTRXPAD6	F19	AVCCAUXK6	F20	VTRXPAD6	F21	GND	F22	LEDn(4)	F24	VRN_7	F28	GND	F30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
G1	GND	G2	VRN_1	G4	AVCCAUXK9	G6	VTRXPAD9	G8	GND	G10	AVCCAUXK7	G12	AVCCAUXK7	G14	GND	G16	GOL_Xclk	G18	VTRXPAD6	G19	AVCCAUXK6	G20	VTRXPAD6	G21	GND	G22	LEDn(5)	G24	VRN_7	G28	GND	G30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
H1	GND	H2	VRN_1	H4	AVCCAUXK9	H6	VTRXPAD9	H8	GND	H10	AVCCAUXK7	H12	AVCCAUXK7	H14	GND	H16	GOL_Xclk	H18	VTRXPAD6	H19	AVCCAUXK6	H20	VTRXPAD6	H21	GND	H22	LEDn(6)	H24	VRN_7	H28	GND	H30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
I1	GND	I2	VRN_1	I4	AVCCAUXK9	I6	VTRXPAD9	I8	GND	I10	AVCCAUXK7	I12	AVCCAUXK7	I14	GND	I16	GOL_Xclk	I18	VTRXPAD6	I19	AVCCAUXK6	I20	VTRXPAD6	I21	GND	I22	LEDn(7)	I24	VRN_7	I28	GND	I30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
J1	GND	J2	VRN_1	J4	AVCCAUXK9	J6	VTRXPAD9	J8	GND	J10	AVCCAUXK7	J12	AVCCAUXK7	J14	GND	J16	GOL_Xclk	J18	VTRXPAD6	J19	AVCCAUXK6	J20	VTRXPAD6	J21	GND	J22	LEDn(8)	J24	VRN_7	J28	GND	J30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
K1	GND	K2	VRN_1	K4	AVCCAUXK9	K6	VTRXPAD9	K8	GND	K10	AVCCAUXK7	K12	AVCCAUXK7	K14	GND	K16	GOL_Xclk	K18	VTRXPAD6	K19	AVCCAUXK6	K20	VTRXPAD6	K21	GND	K22	LEDn(9)	K24	VRN_7	K28	GND	K30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
L1	GND	L2	VRN_1	L4	AVCCAUXK9	L6	VTRXPAD9	L8	GND	L10	AVCCAUXK7	L12	AVCCAUXK7	L14	GND	L16	GOL_Xclk	L18	VTRXPAD6	L19	AVCCAUXK6	L20	VTRXPAD6	L21	GND	L22	LEDn(10)	L24	VRN_7	L28	GND	L30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
M1	GND	M2	VRN_1	M4	AVCCAUXK9	M6	VTRXPAD9	M8	GND	M10	AVCCAUXK7	M12	AVCCAUXK7	M14	GND	M16	GOL_Xclk	M18	VTRXPAD6	M19	AVCCAUXK6	M20	VTRXPAD6	M21	GND	M22	LEDn(11)	M24	VRN_7	M28	GND	M30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
N1	GND	N2	VRN_1	N4	AVCCAUXK9	N6	VTRXPAD9	N8	GND	N10	AVCCAUXK7	N12	AVCCAUXK7	N14	GND	N16	GOL_Xclk	N18	VTRXPAD6	N19	AVCCAUXK6	N20	VTRXPAD6	N21	GND	N22	LEDn(12)	N24	VRN_7	N28	GND	N30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
P1	GND	P2	VRN_1	P4	AVCCAUXK9	P6	VTRXPAD9	P8	GND	P10	AVCCAUXK7	P12	AVCCAUXK7	P14	GND	P16	GOL_Xclk	P18	VTRXPAD6	P19	AVCCAUXK6	P20	VTRXPAD6	P21	GND	P22	LEDn(13)	P24	VRN_7	P28	GND	P30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
Q1	GND	Q2	VRN_1	Q4	AVCCAUXK9	Q6	VTRXPAD9	Q8	GND	Q10	AVCCAUXK7	Q12	AVCCAUXK7	Q14	GND	Q16	GOL_Xclk	Q18	VTRXPAD6	Q19	AVCCAUXK6	Q20	VTRXPAD6	Q21	GND	Q22	LEDn(14)	Q24	VRN_7	Q28	GND	Q30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
R1	GND	R2	VRN_1	R4	AVCCAUXK9	R6	VTRXPAD9	R8	GND	R10	AVCCAUXK7	R12	AVCCAUXK7	R14	GND	R16	GOL_Xclk	R18	VTRXPAD6	R19	AVCCAUXK6	R20	VTRXPAD6	R21	GND	R22	LEDn(15)	R24	VRN_7	R28	GND	R30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
S1	GND	S2	VRN_1	S4	AVCCAUXK9	S6	VTRXPAD9	S8	GND	S10	AVCCAUXK7	S12	AVCCAUXK7	S14	GND	S16	GOL_Xclk	S18	VTRXPAD6	S19	AVCCAUXK6	S20	VTRXPAD6	S21	GND	S22	LEDn(16)	S24	VRN_7	S28	GND	S30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
T1	GND	T2	VRN_1	T4	AVCCAUXK9	T6	VTRXPAD9	T8	GND	T10	AVCCAUXK7	T12	AVCCAUXK7	T14	GND	T16	GOL_Xclk	T18	VTRXPAD6	T19	AVCCAUXK6	T20	VTRXPAD6	T21	GND	T22	LEDn(17)	T24	VRN_7	T28	GND	T30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
U1	GND	U2	VRN_1	U4	AVCCAUXK9	U6	VTRXPAD9	U8	GND	U10	AVCCAUXK7	U12	AVCCAUXK7	U14	GND	U16	GOL_Xclk	U18	VTRXPAD6	U19	AVCCAUXK6	U20	VTRXPAD6	U21	GND	U22	LEDn(18)	U24	VRN_7	U28	GND	U30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
V1	GND	V2	VRN_1	V4	AVCCAUXK9	V6	VTRXPAD9	V8	GND	V10	AVCCAUXK7	V12	AVCCAUXK7	V14	GND	V16	GOL_Xclk	V18	VTRXPAD6	V19	AVCCAUXK6	V20	VTRXPAD6	V21	GND	V22	LEDn(19)	V24	VRN_7	V28	GND	V30																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
W1	Adr(21)	W2	MS0_n	W3	MS1_n	W4	MS2_n	W5	MS3_n	W6	MS4_n	W7	MS5_n	W8	MS6_n	W9	MS7_n	W10	MS8_n	W11	MS9_n	W12	MS10_n	W13	MS11_n	W14	MS12_n	W15	MS13_n	W16	MS14_n	W17	MS15_n	W18	MS16_n	W19	MS17_n	W20	MS18_n	W21	MS19_n	W22	MS20_n	W23	MS21_n	W24	MS22_n	W25	MS23_n	W26	MS24_n	W27	MS25_n	W28	MS26_n	W29	MS27_n	W30	MS28_n	W31	MS29_n	W32	MS30_n	W33	MS31_n	W34	MS32_n	W35	MS33_n	W36	MS34_n	W37	MS35_n	W38	MS36_n	W39	MS37_n	W40	MS38_n	W41	MS39_n	W42	MS40_n	W43	MS41_n	W44	MS42_n	W45	MS43_n	W46	MS44_n	W47	MS45_n	W48	MS46_n	W49	MS47_n	W50	MS48_n	W51	MS49_n	W52	MS50_n	W53	MS51_n	W54	MS52_n	W55	MS53_n	W56	MS54_n	W57	MS55_n	W58	MS56_n	W59	MS57_n	W60	MS58_n	W61	MS59_n	W62	MS60_n	W63	MS61_n	W64	MS62_n	W65	MS63_n	W66	MS64_n	W67	MS65_n	W68	MS66_n	W69	MS67_n	W70	MS68_n	W71	MS69_n	W72	MS70_n	W73	MS71_n	W74	MS72_n	W75	MS73_n	W76	MS74_n	W77	MS75_n	W78	MS76_n	W79	MS77_n	W80	MS78_n	W81	MS79_n	W82	MS80_n	W83	MS81_n	W84	MS82_n	W85	MS83_n	W86	MS84_n	W87	MS85_n	W88	MS86_n	W89	MS87_n	W90	MS88_n	W91	MS89_n	W92	MS90_n	W93	MS91_n	W94	MS92_n	W95	MS93_n	W96	MS94_n	W97	MS95_n	W98	MS96_n	W99	MS97_n	W100	MS98_n	W101	MS99_n	W102	MS100_n	W103	MS101_n	W104	MS102_n	W105	MS103_n	W106	MS104_n	W107	MS105_n	W108	MS106_n	W109	MS107_n	W110	MS108_n	W111	MS109_n	W112	MS110_n	W113	MS111_n	W114	MS112_n	W115	MS113_n	W116	MS114_n	W117	MS115_n	W118	MS116_n	W119	MS117_n	W120	MS118_n	W121	MS119_n	W122	MS120_n	W123	MS121_n	W124	MS122_n	W125	MS123_n	W126	MS124_n	W127	MS125_n	W128	MS126_n	W129	MS127_n	W130	MS128_n	W131	MS129_n	W132	MS130_n	W133	MS131_n	W134	MS132_n	W135	MS133_n	W136	MS134_n	W137	MS135_n	W138	MS136_n	W139	MS137_n	W140	MS138_n	W141	MS139_n	W142	MS140_n	W143	MS141_n	W144	MS142_n	W145	MS143_n	W146	MS144_n	W147	MS145_n	W148	MS146_n	W149	MS147_n	W150	MS148_n	W151	MS149_n	W152	MS150_n	W153	MS151_n	W154	MS152_n	W155	MS153_n	W156	MS154_n	W157	MS155_n	W158	MS156_n	W159	MS157_n	W160	MS158_n	W161	MS159_n	W162	MS160_n	W163	MS161_n	W164	MS162_n	W165	MS163_n	W166	MS164_n	W167	MS165_n	W168	MS166_n	W169	MS167_n	W170	MS168_n	W171	MS169_n	W172	MS170_n	W173	MS171_n	W174	MS172_n	W175	MS173_n	W176	MS174_n	W177	MS175_n	W178	MS176_n	W179	MS177_n	W180	MS178_n	W181	MS179_n	W182	MS180_n	W183	MS181_n	W184	MS182_n	W185	MS183_n	W186	MS184_n	W187	MS185_n	W188	MS186_n	W189	MS187_n	W190	MS188_n	W191	MS189_n	W192	MS190_n	W193	MS191_n	W194	MS192_n	W195	MS193_n	W196	MS194_n	W197	MS195_n	W198	MS196_n	W199	MS197_n	W200	MS198_n	W201	MS199_n	W202	MS200_n	W203	MS201_n	W204	MS202_n	W205	MS203_n	W206	MS204_n	W207	MS205_n	W208	MS206_n	W209	MS207_n	W210	MS208_n	W211	MS209_n	W212	MS210_n	W213	MS211_n	W214	MS212_n	W215	MS213_n	W216	MS214_n	W217	MS215_n	W218	MS216_n	W219	MS217_n	W220	MS218_n	W221	MS219_n	W222	MS220_n	W223	MS221_n	W224	MS222_n	W225	MS223_n	W226	MS224_n	W227	MS225_n	W228	MS226_n	W229	MS227_n	W230	MS228_n	W231	MS229_n	W232	MS230_n	W233	MS231_n	W234	MS232_n	W235	MS233_n	W236	MS234_n	W237	MS235_n	W238	MS236_n	W239	MS237_n	W240	MS238_n	W241	MS239_n	W242	MS240_n	W243	MS241_n	W244	MS242_n	W245	MS243_n	W246	MS244_n	W247	MS245_n	W248	MS246_n	W249	MS247_n	W250	MS248_n	W251	MS249_n	W252	MS250_n	W253	MS251_n	W254	MS252_n	W255	MS253_n	W256	MS254_n	W257	MS255_n	W258	MS256_n	W259	MS257_n	W260	MS258_n	W261	MS259_n	W262	MS260_n	W263	MS261_n	W264	MS262_n	W265	MS263_n	W266	MS264_n	W267	MS265_n	W268	MS266_n	W269	MS267_n	W270	MS268_n	W271	MS269_n	W272	MS270_n	W273	MS271_n	W274	MS272_n	W275	MS273_n	W276	MS274_n	W277	MS275_n	W278	MS276_n	W279	MS277_n	W280	MS278_n	W281	MS279_n	W282	MS280_n	W283	MS281_n	W284	MS282_n	W285	MS283_n	W286	MS284_n	W287	MS285_n	W288	MS286_n	W289	MS287_n	W290	MS288_n	W291	MS289_n	W292	MS290_n	W293	MS291_n	W294	MS292_n	W295	MS293_n	W296	MS294_n	W297	MS295_n	W298	MS296_n	W299	MS297_n	W300	MS298_n	W301	MS299_n	W302	MS300_n	W303	MS301_n	W304	MS302_n	W305	MS303_n	W306	MS304_n	W307	MS305_n	W308	MS306_n	W309	MS307_n	W310	MS308_n	W311	MS309_n	W312	MS310_n	W313	MS311_n	W314	MS312_n	W315	MS313_n	W316	MS314_n	W317	MS315_n	W318	MS316_n	W319	MS317_n	W320	MS318_n	W321	MS319_n	W322	MS320_n	W323	MS321_n	W324	MS322_n	W325	MS323_n	W326	MS324_n	W327	MS325_n	W328	MS326_n	W329	MS327_n	W330	MS328_n	W331	MS329_n	W332	MS330_n	W333	MS331_n	W334	MS332_n	W335	MS333_n	W336	MS334_n	W337	MS335_n	W338	MS336_n	W339	MS337_n	W340	MS338_n	W341	MS339_n	W342	MS340_n	W343	MS341_n	W344	MS342_n	W345	MS343_n	W346	MS344_n	W347	MS345_n	W348	MS346_n	W349	MS347_n	W350	MS348_n	W351	MS349_n	W352	MS350_n	W353	MS351_n	W354	MS352_n	W355	MS353_n	W356	MS354_n	W357	MS355_n	W358	MS356_n	W359	MS357_n	W360	MS358_n	W361	MS359_n	W362	MS360_n	W363	MS361_n	W364	MS362_n	W365	MS363_n	W366	MS364_n	W367	MS365_n	W368	MS366_n	W369	MS367_n	W370	MS368_n	W371	MS369_n	W372	MS370_n	W373	MS371_n	W374	MS372_n	W375	MS373_n	W376	MS374_n	W377	MS375_n	W378	MS376_n	W379	MS377_n	W



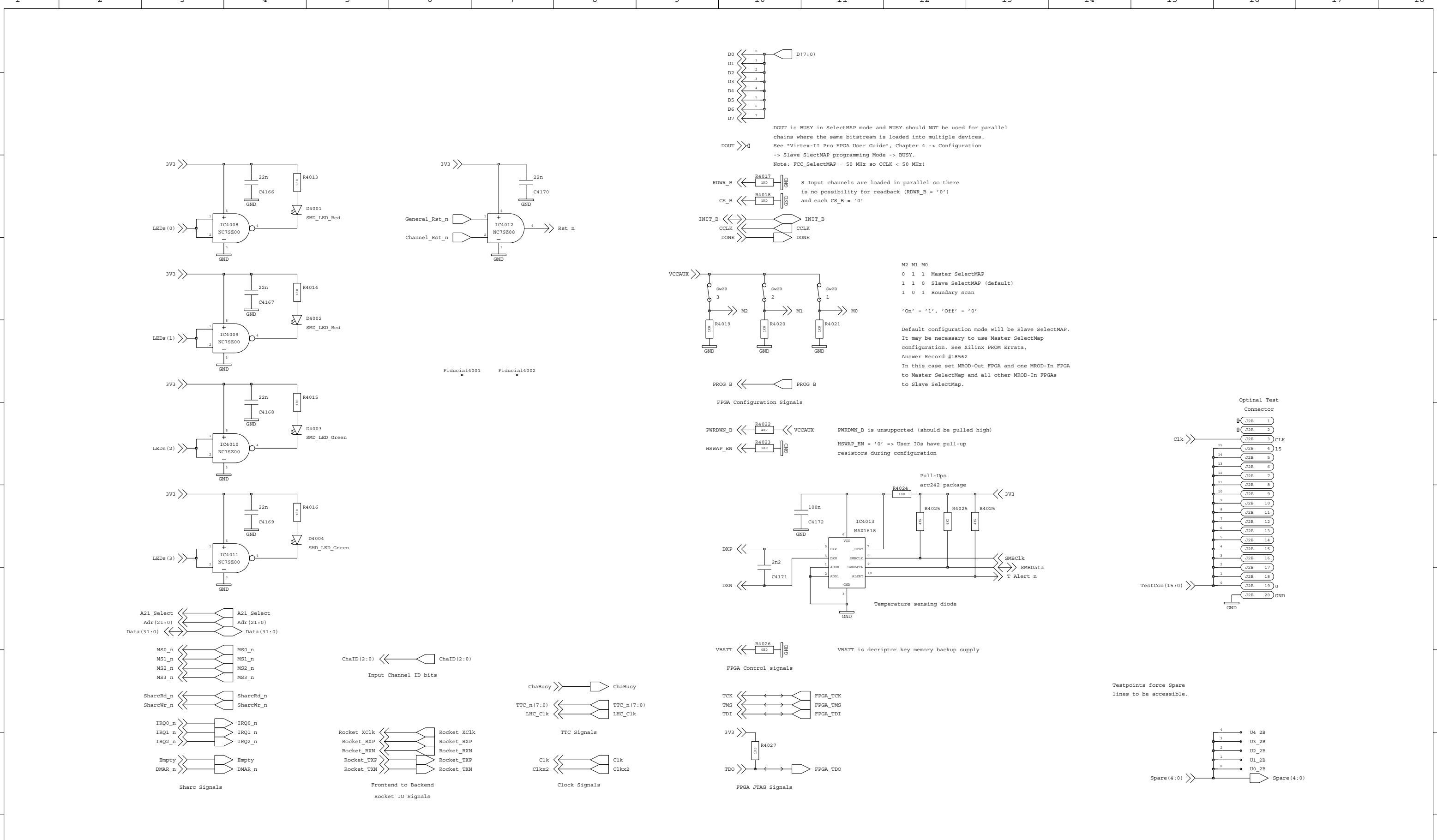
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		Date	7 Feb 2006	
Input FPGA Power Supply Decoupling		Time	1:51:34 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
Page		3	of	6



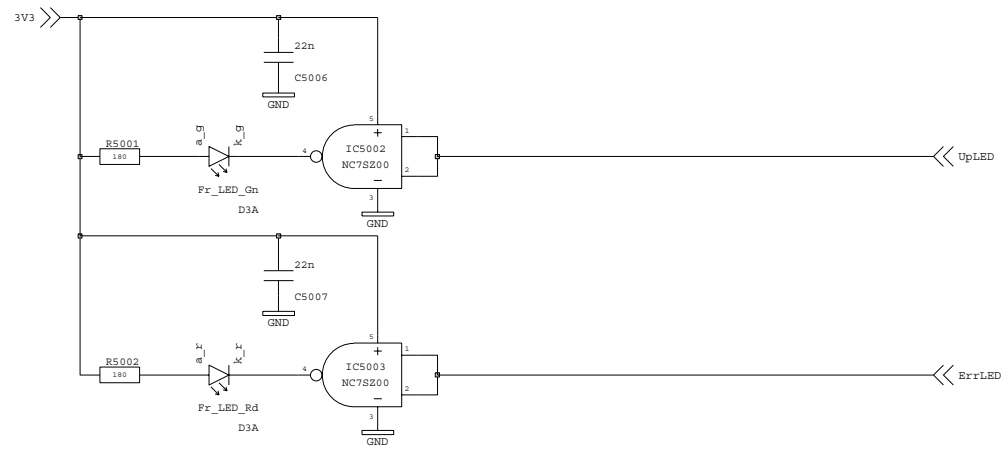
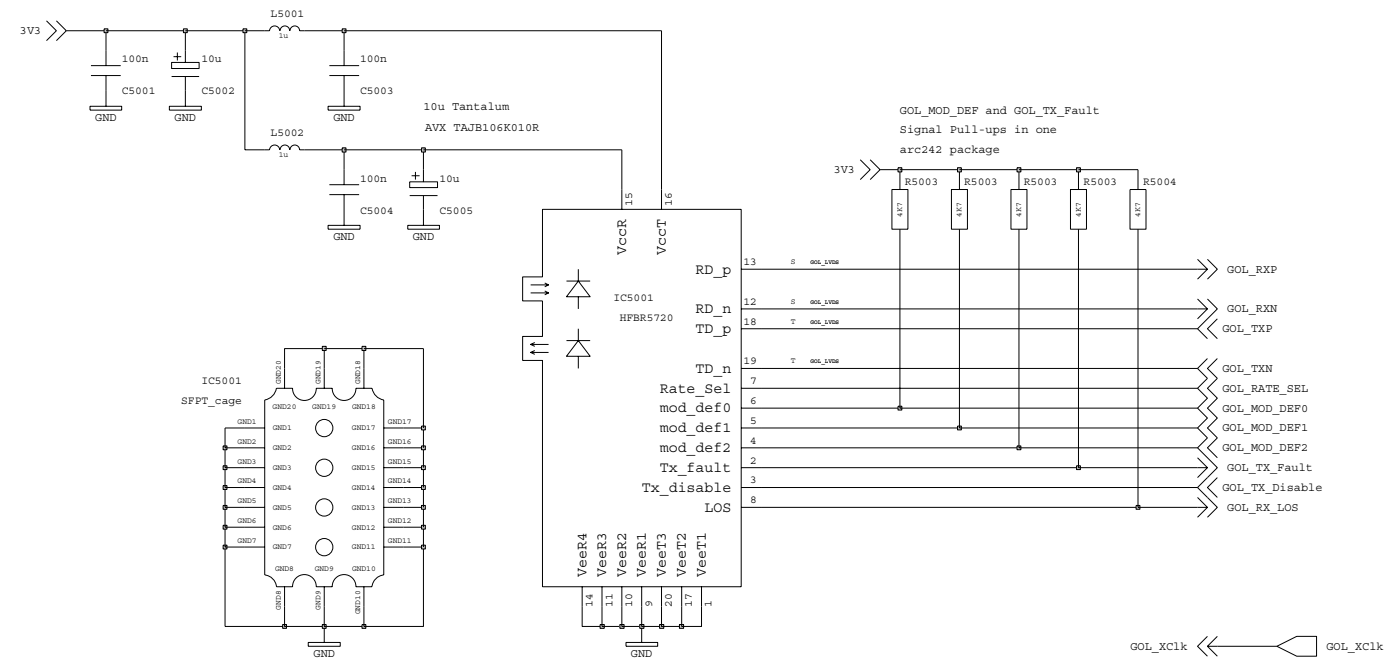
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		Date	7 Feb 2006							
Input FPGA MGT Pwr Decoupling, Termination			Time	1:52:01 pm						
Proj:	MROD-X	Proj.No:	38405							
Peter Jansweijer		peterj@nikhef.nl								
NIKHEF © NIKHEF Amsterdam		NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND			Size	A3	4	1	4	A
					Dim	420 x 297 mm				
					Page	4 of 6				



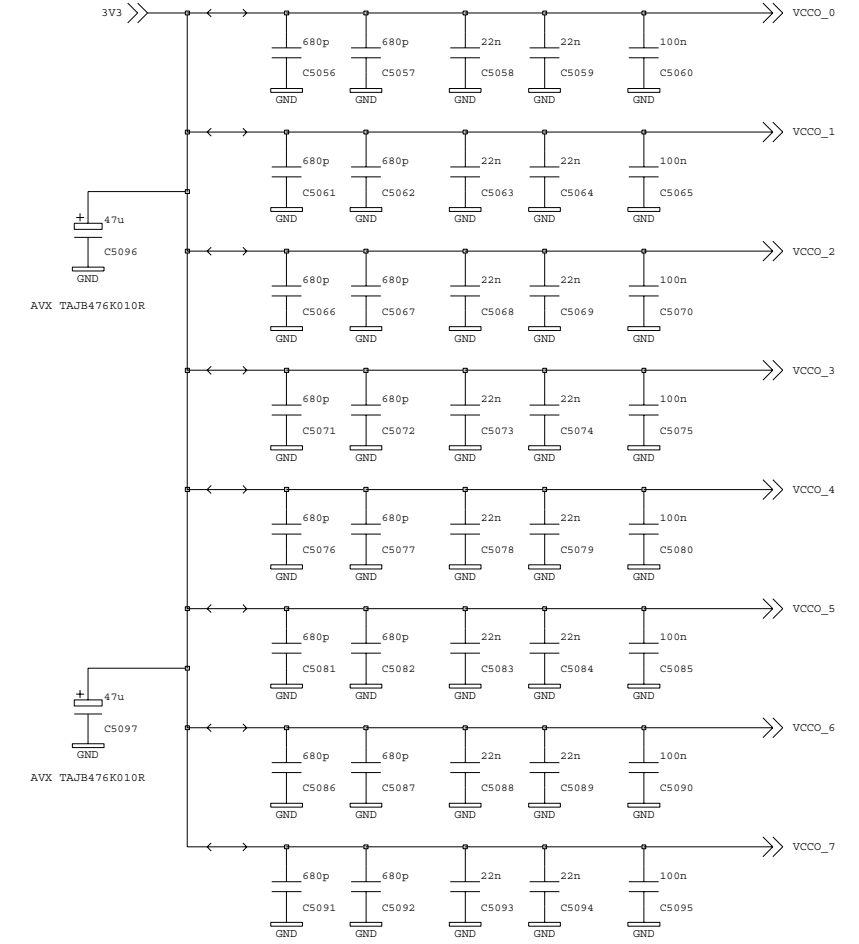
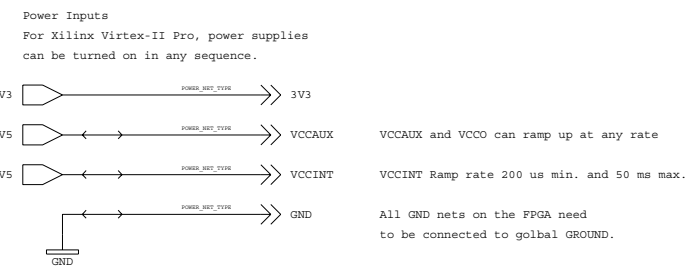
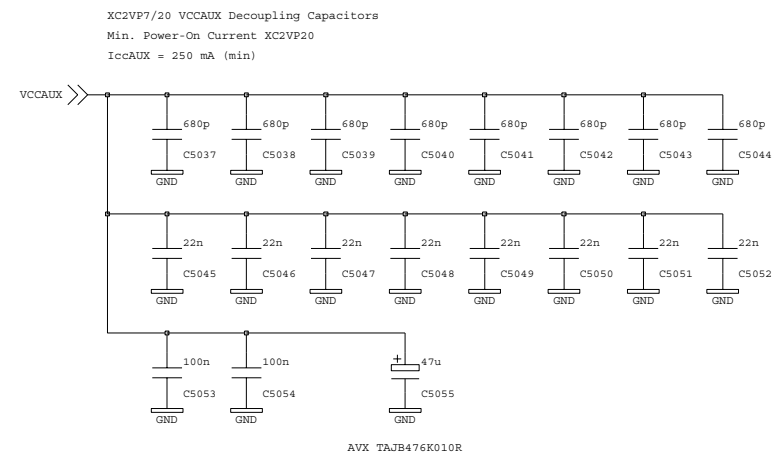
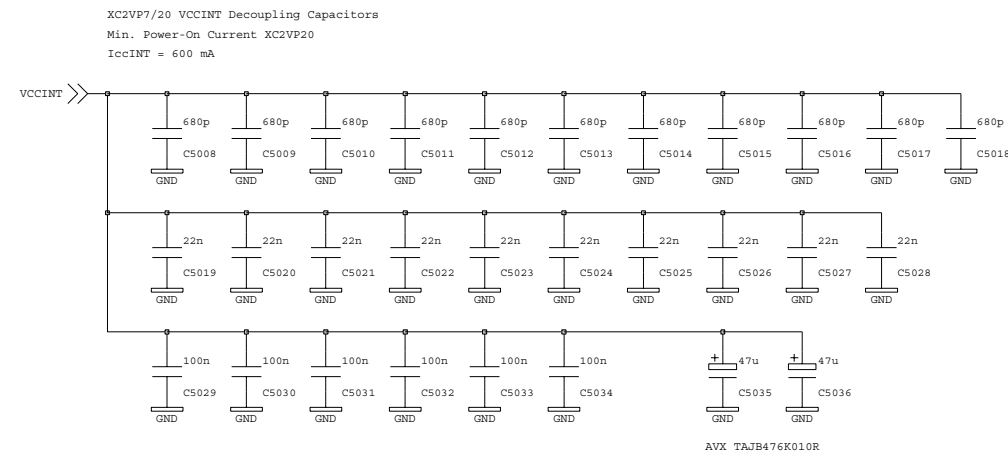
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © T-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	5	of 6



channel_in		Rev	V2	2
		Date	7 Feb 2006	
Input FPGA Auxiliary Connections		Time	1:53:04 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	6	of 6



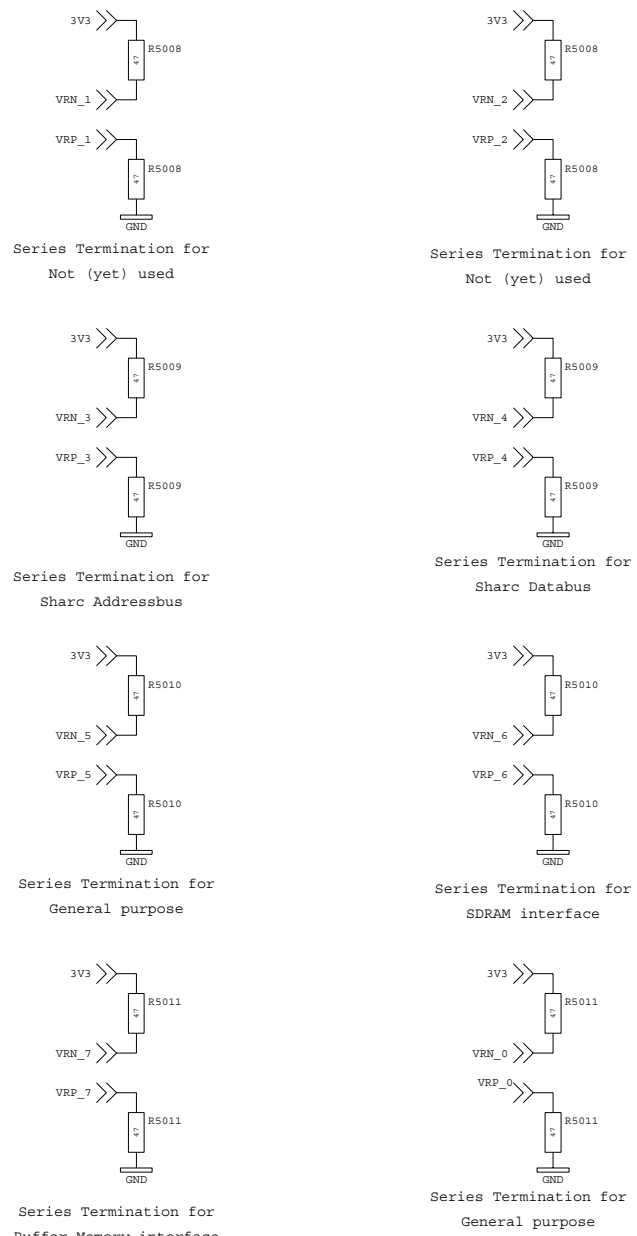
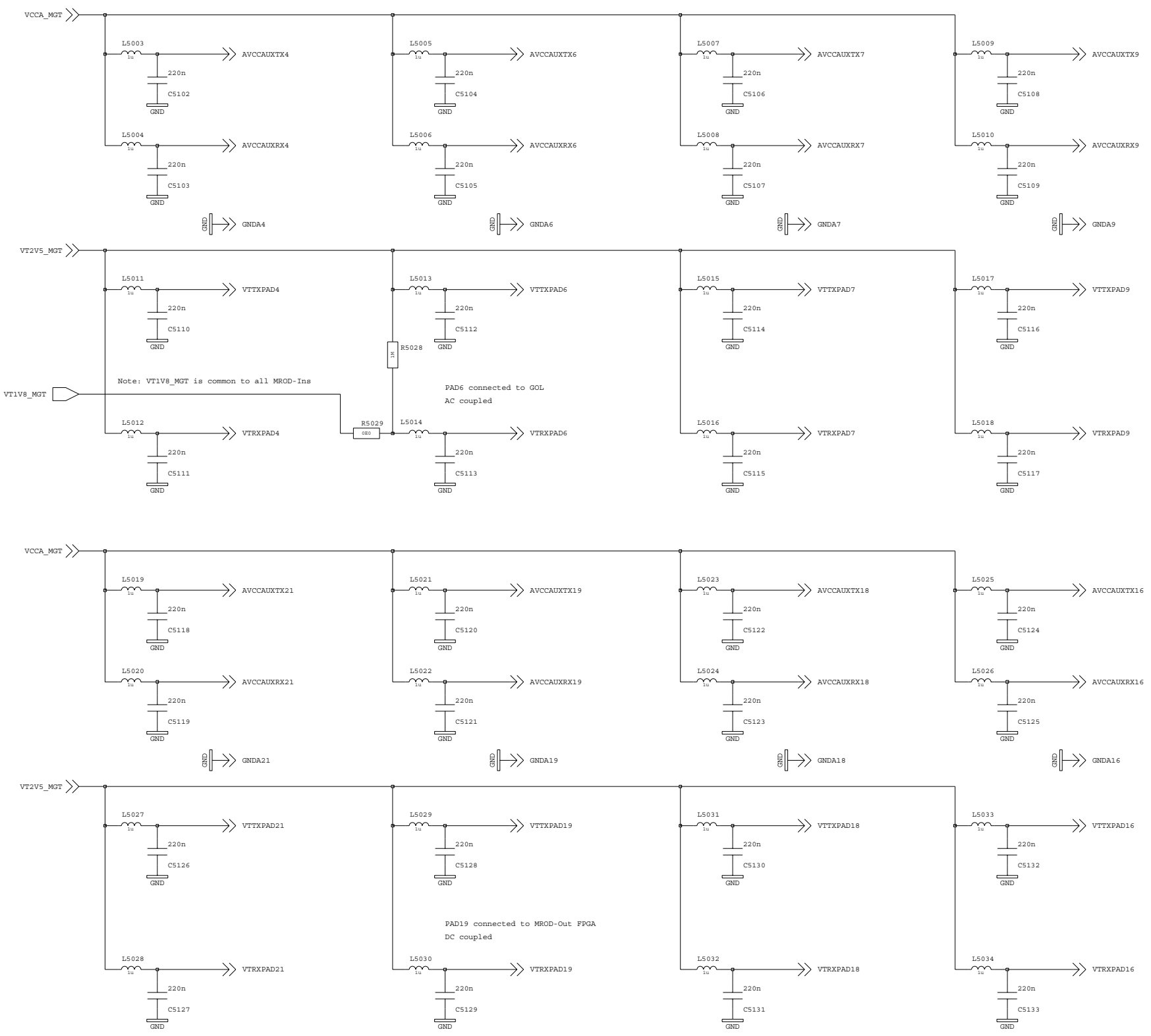
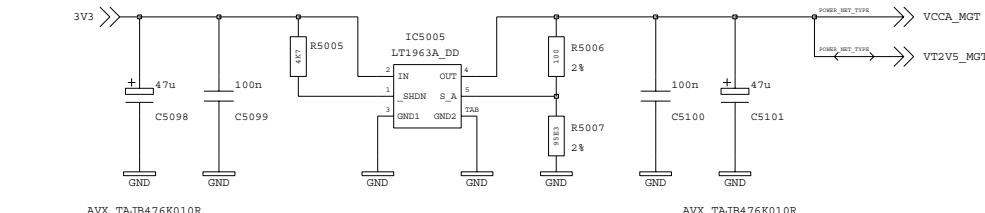
channel_in		Rev	V2	2
		Date	7 Feb 2006	
GOL Input		Time	1:50:33 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Dim	420 x 297 mm	
		Page	1 of 6	



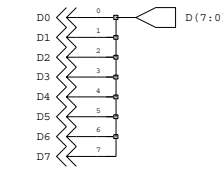
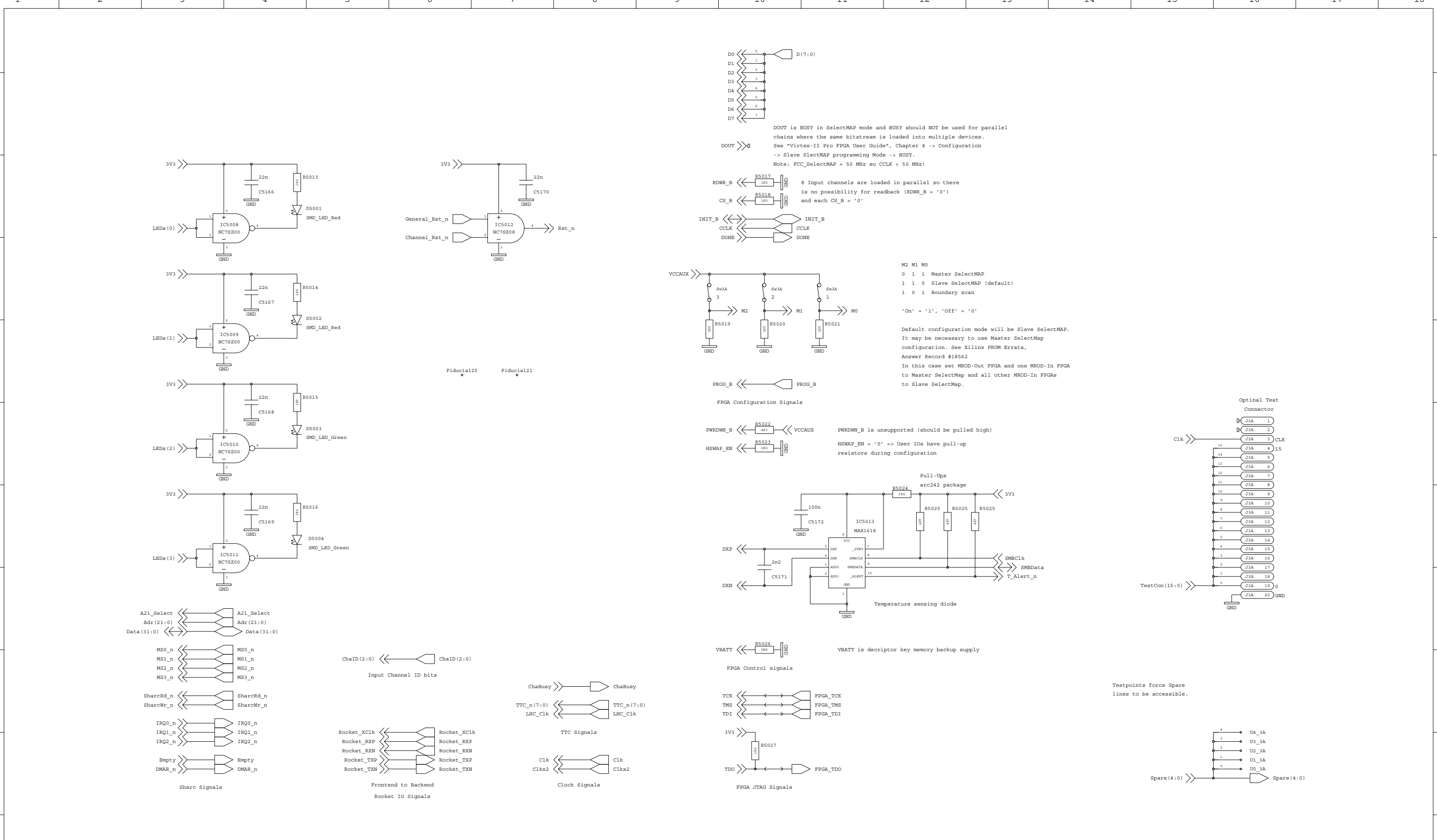
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Input FPGA Power Supply Decoupling		Time	1:51:34 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF <small>© ET-Nikhef Amsterdam</small>		<small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
Page		3	of	6

2V5 @ 1,5A

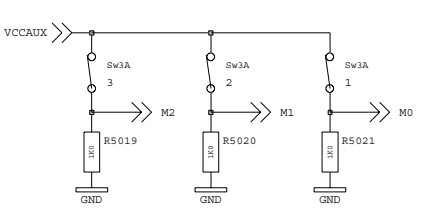
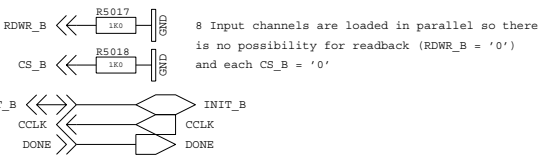
=> MGT Power (estimated 31 + 49 = 80 mA)
=> MGT TX (RX) Termination (estimated 11 mA)



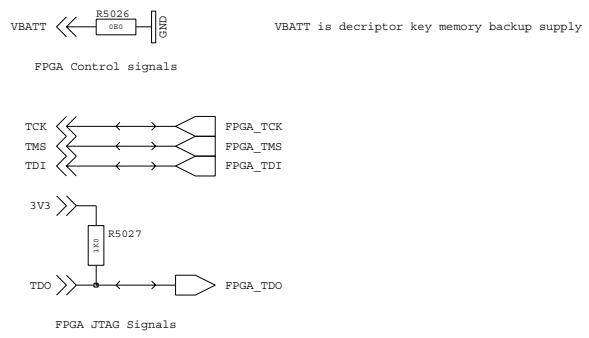
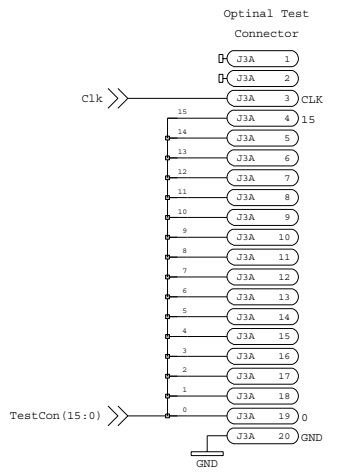
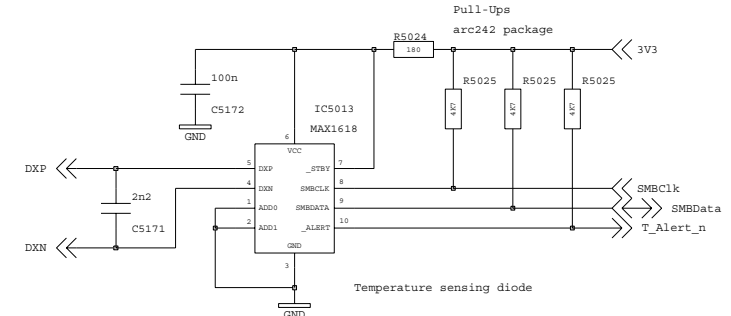
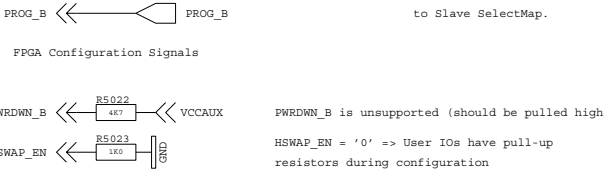
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time	1:52:01 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © NIKHEF Amsterdam		NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	4	of 6



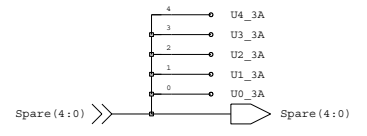
DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices. See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SelectMAP programming Mode -> BUSY. Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!



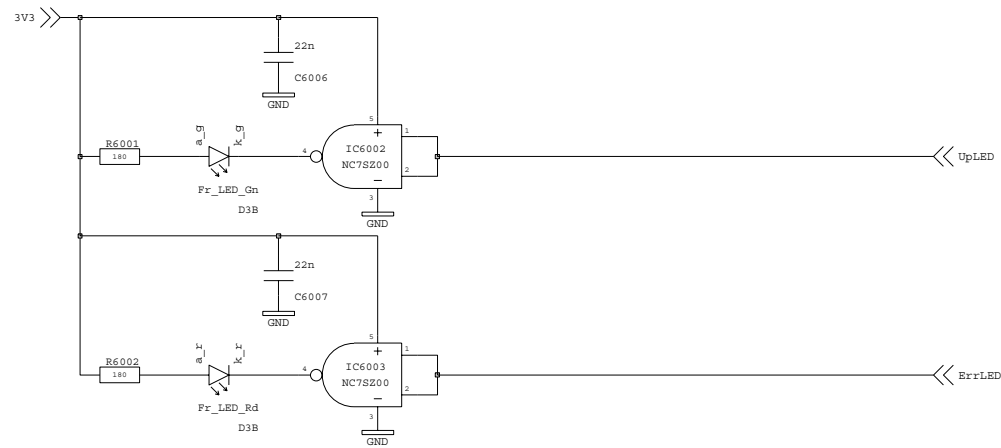
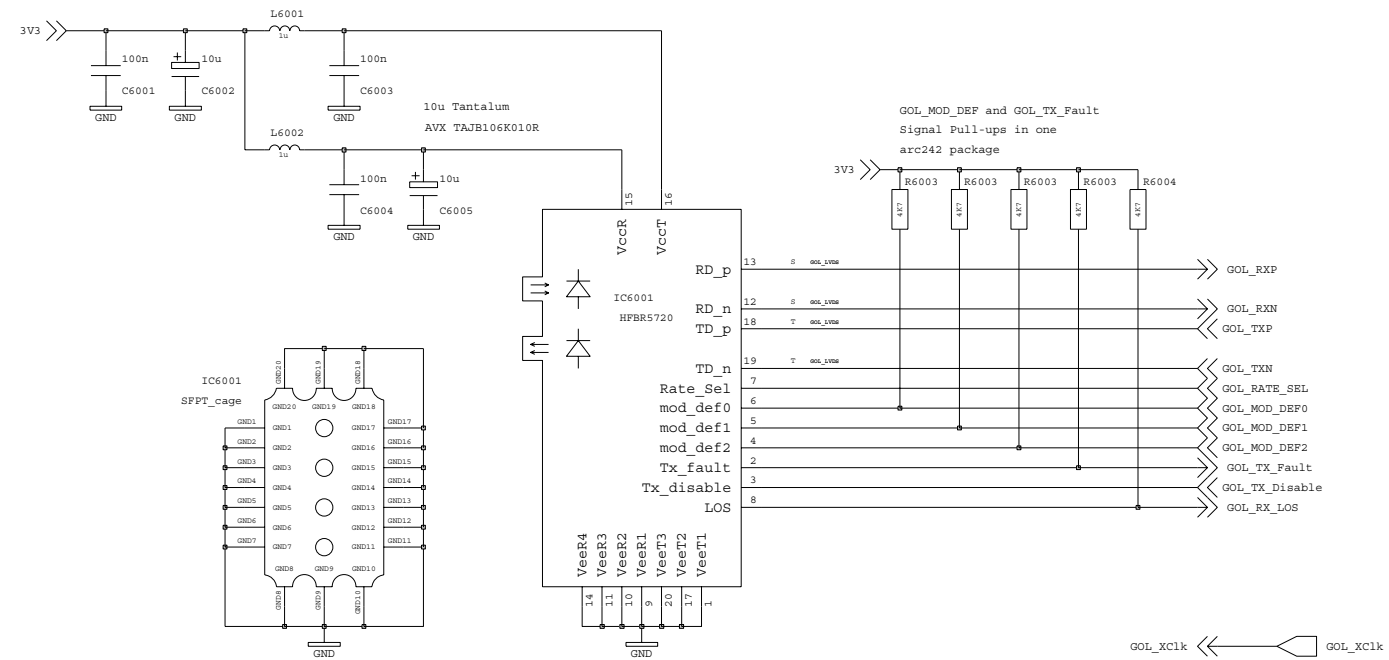
M2 M1 M0
 0 1 1 Master SelectMAP
 1 1 0 Slave SelectMAP (default)
 1 0 1 Boundary scan
 'On' = '1', 'Off' = '0'
 Default configuration mode will be Slave SelectMAP. It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562. In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.



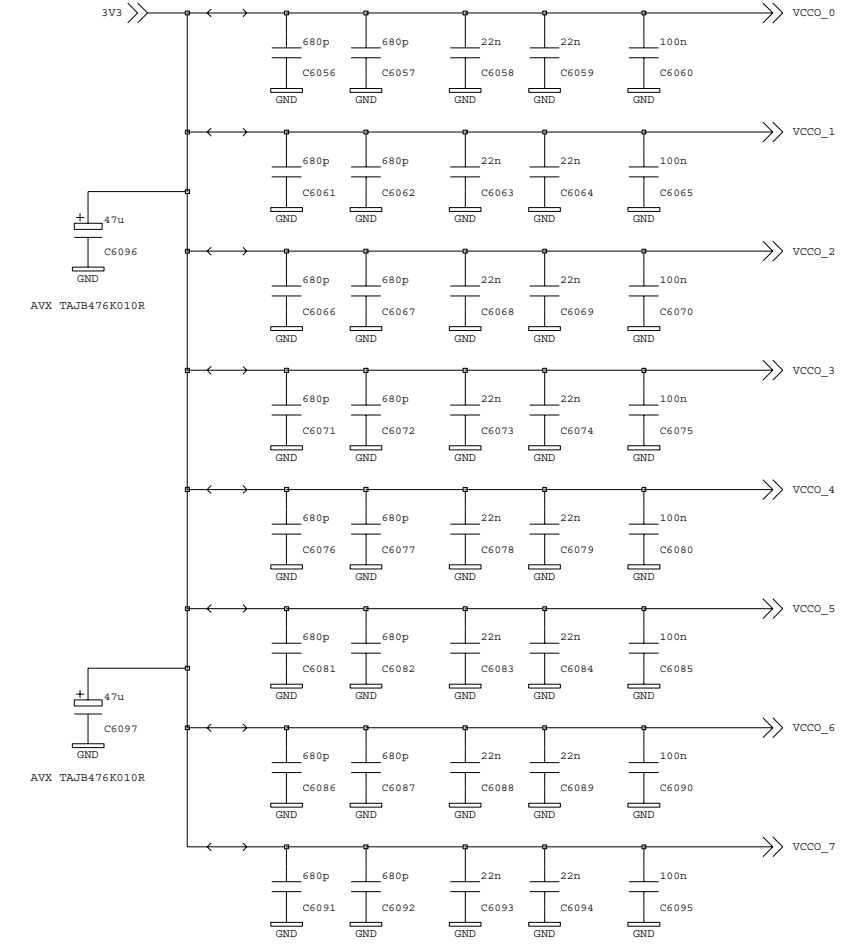
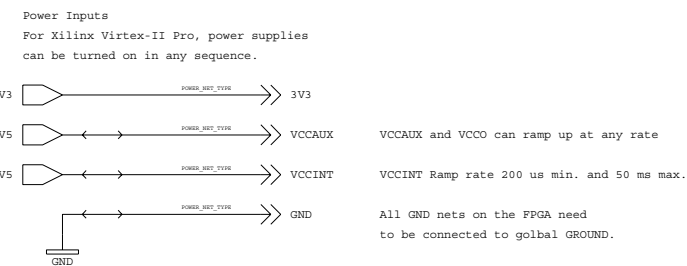
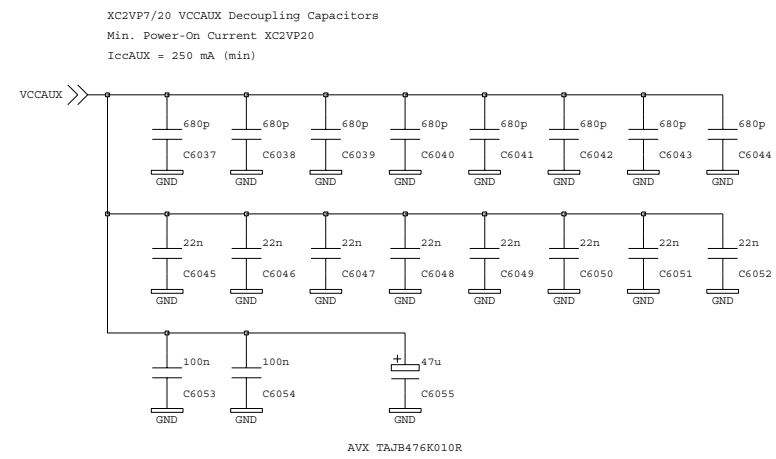
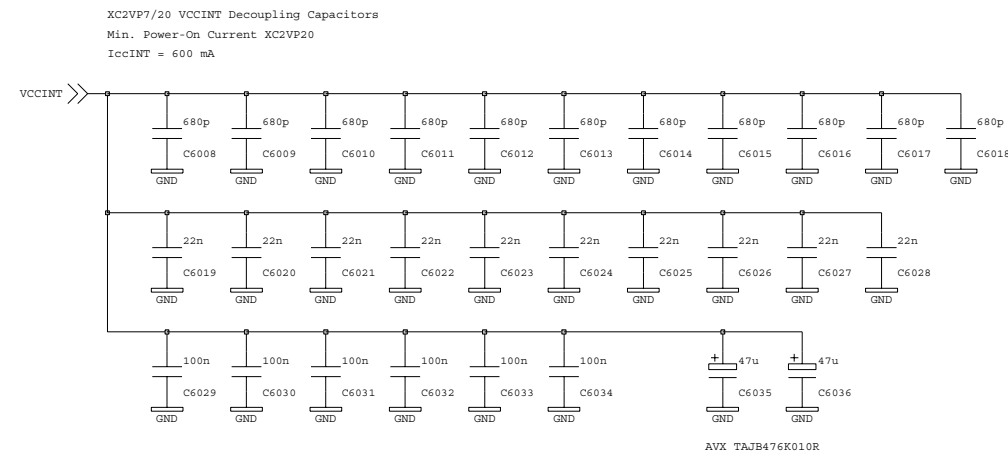
Testpoints force Spare lines to be accessible.



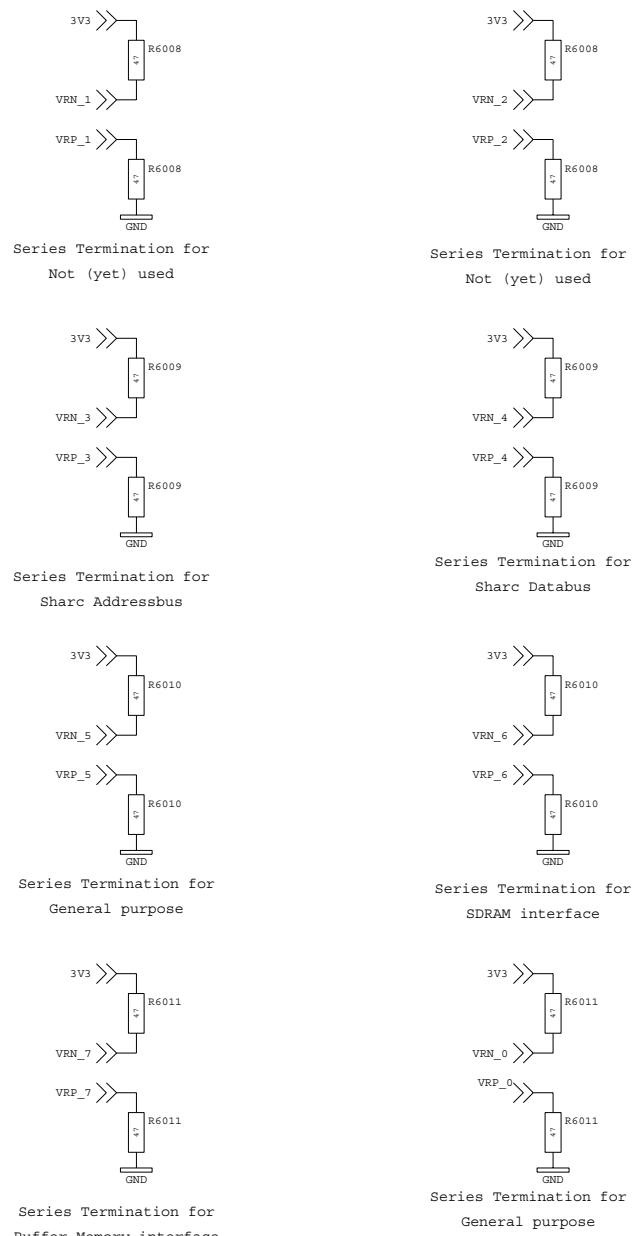
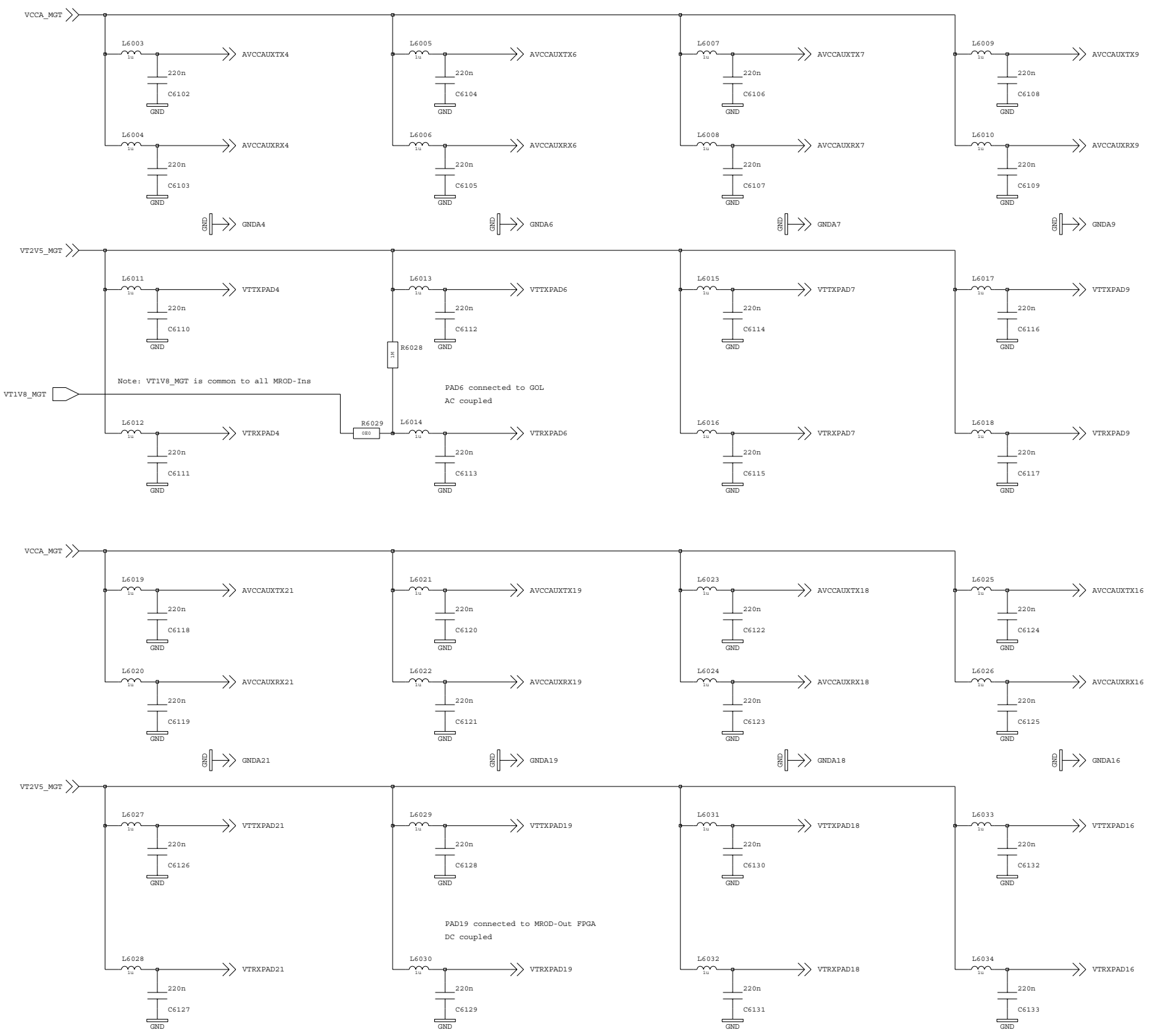
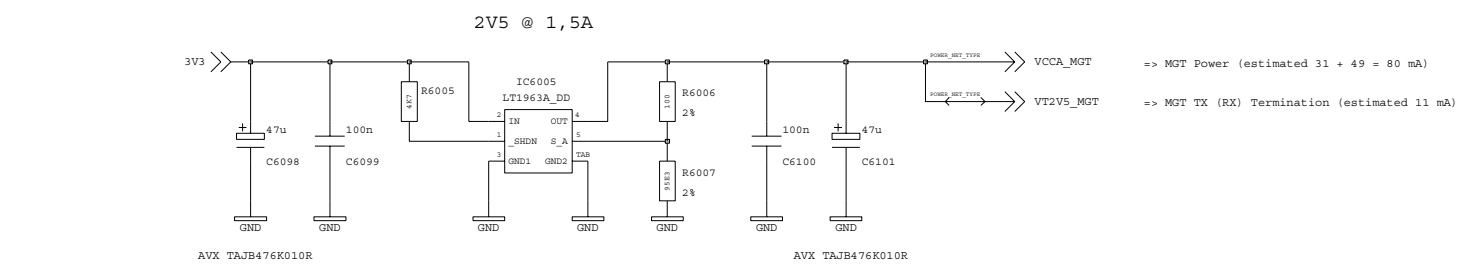
channel_in		Rev V2 2
		Date 7 Feb 2006
Input FPGA Auxiliary Connections		Time 1:53:04 pm
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size A3 4 1 4 A
		Dim 420 x 297 mm
		Page 6 of 6



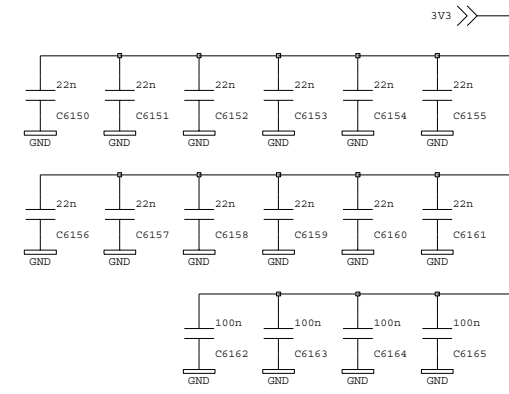
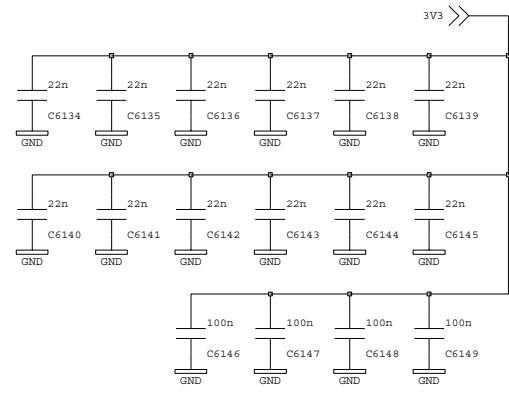
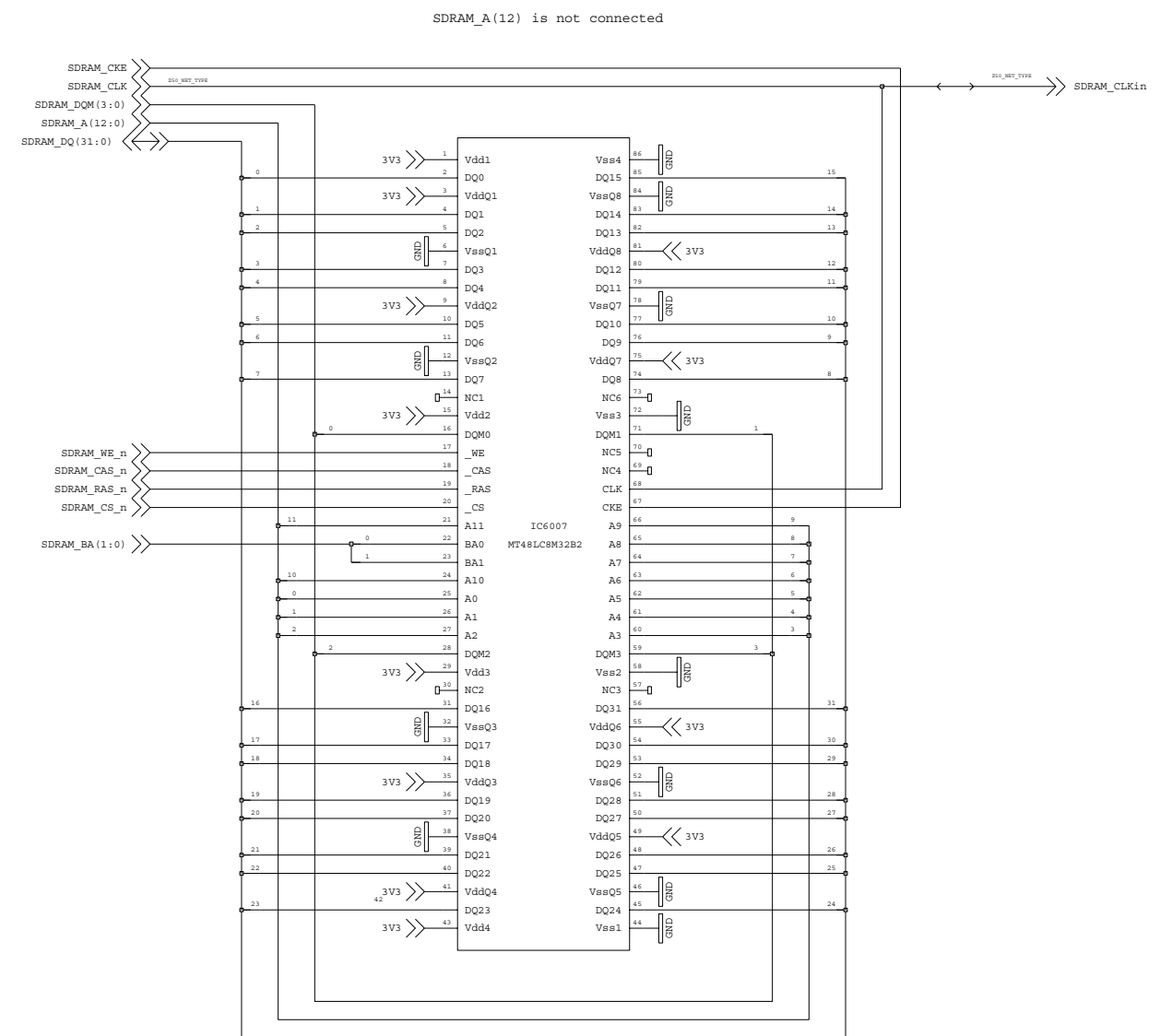
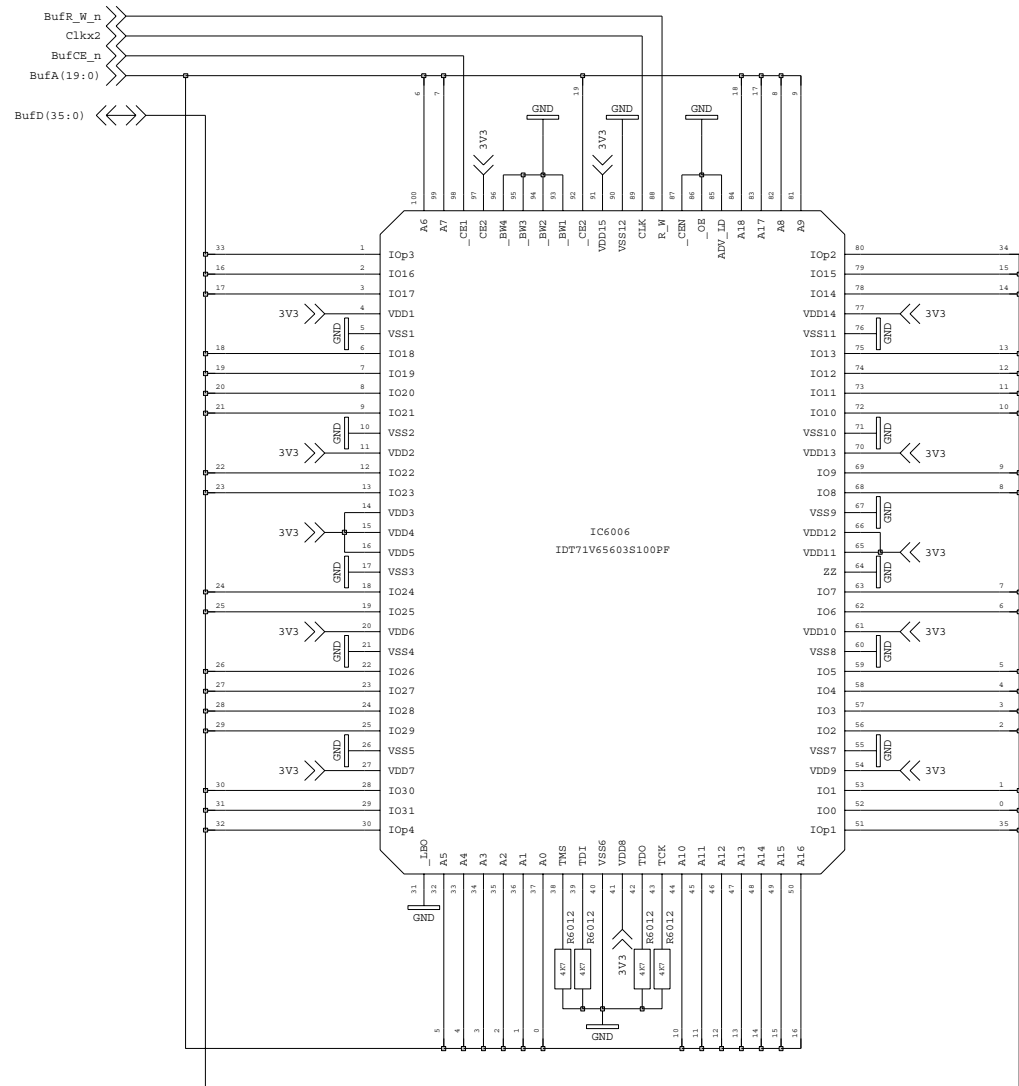
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		Date	7 Feb 2006					
GOL Input		Time	1:50:33 pm					
Proj:	MROD-X	Proj.No:	38405					
Peter Jansweijer		peterj@nikhef.nl						
NIKHEF © ET-Nikhef Amsterdam	NATIONAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size	A3	4	1	4	A
			Dim	420 x 297 mm				
			Page	1 of 6				



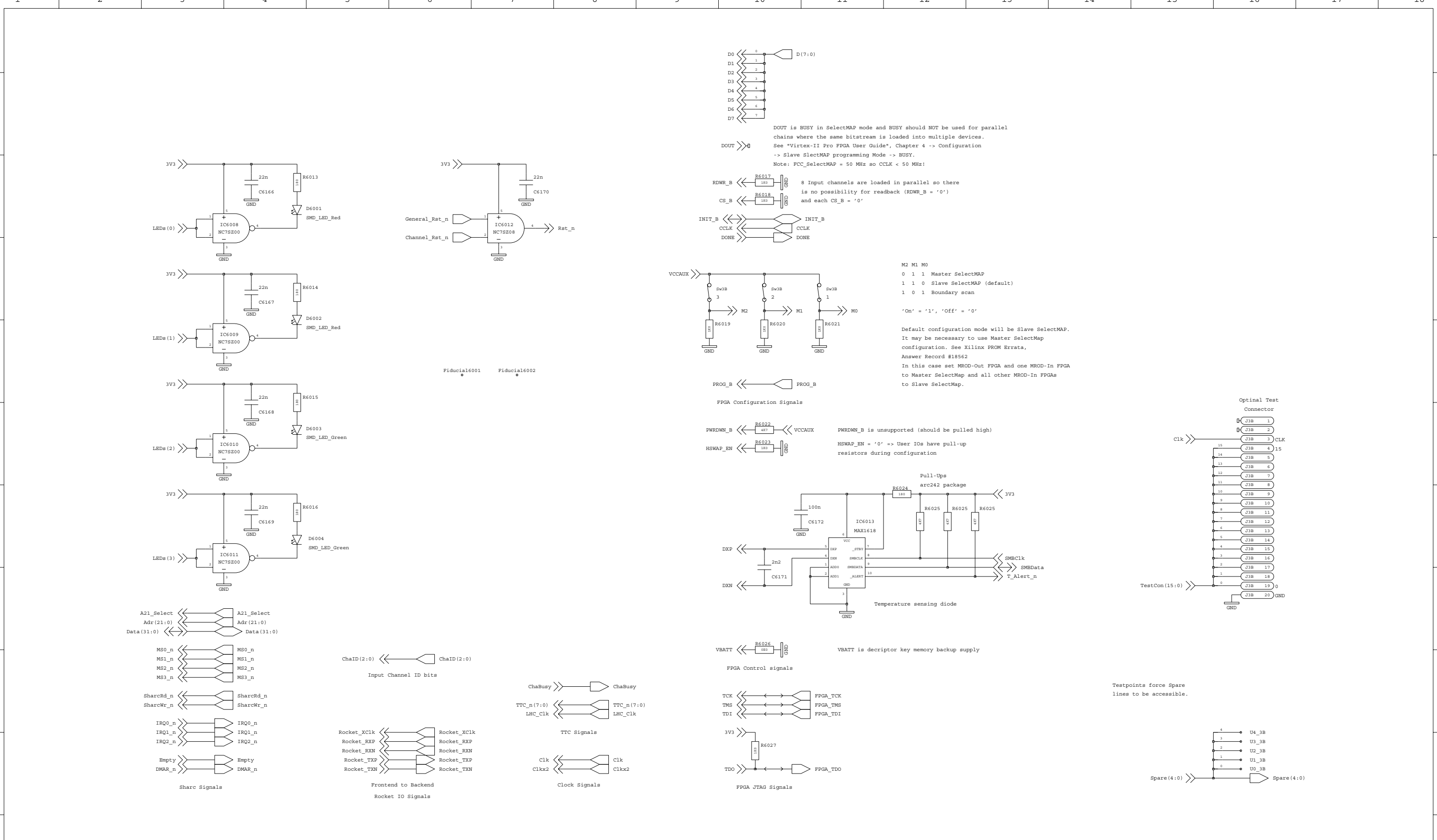
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		Date	7 Feb 2006	
Input FPGA Power Supply Decoupling		Time	1:51:34 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	3 of 6	



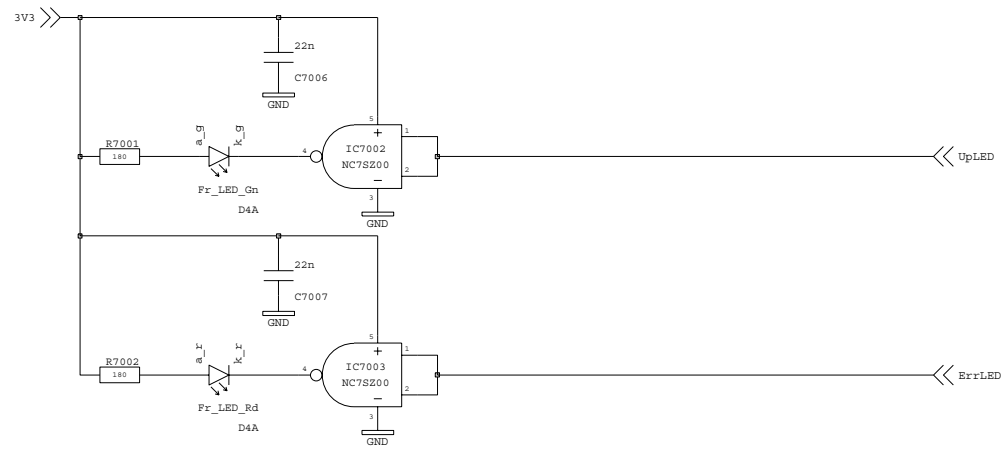
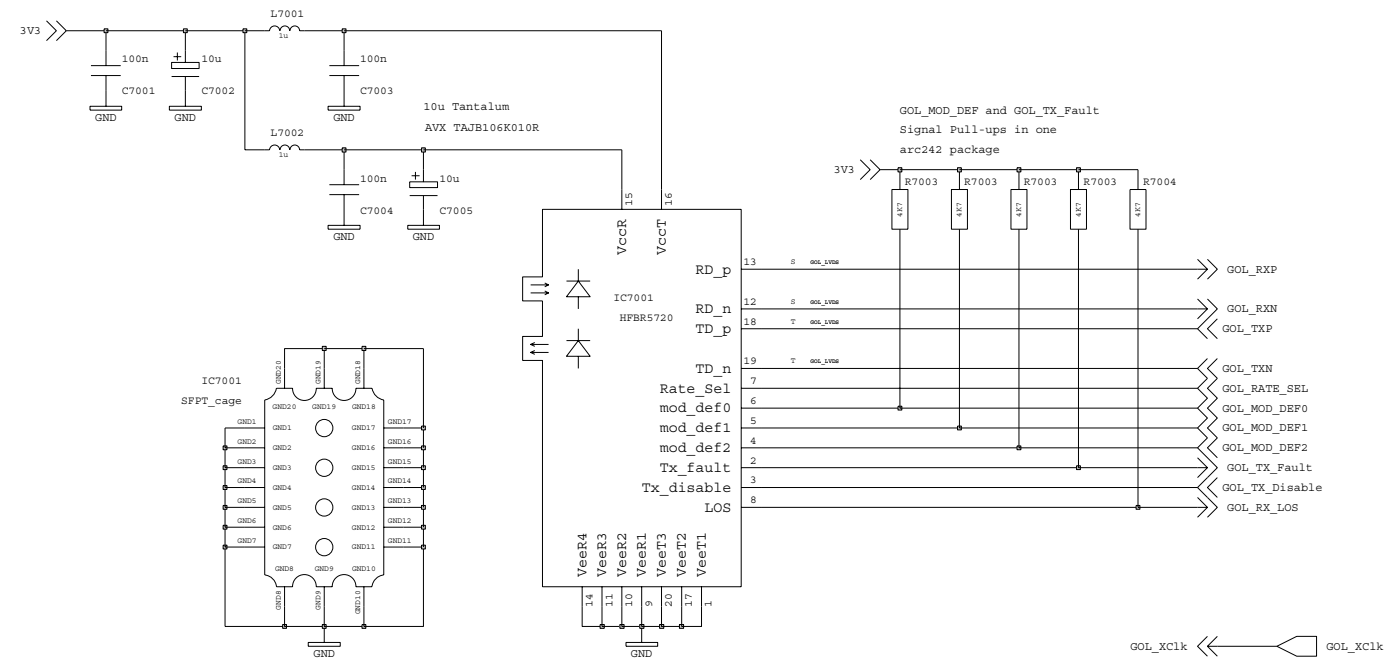
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time	1:52:01 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © NIKHEF Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	4	of 6



channel_in		Rev	V2	2
		Date	7 Feb 2006	
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm	
Proj: MROD-X	Proj.No: 38405	Name	Ton van Reen	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Dim	420 x 297 mm	
		Page	5	of 6



channel_in		Rev	V2	2
		Date	7 Feb 2006	
Input FPGA Auxiliary Connections		Time	1:53:04 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOOG ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	6	of 6



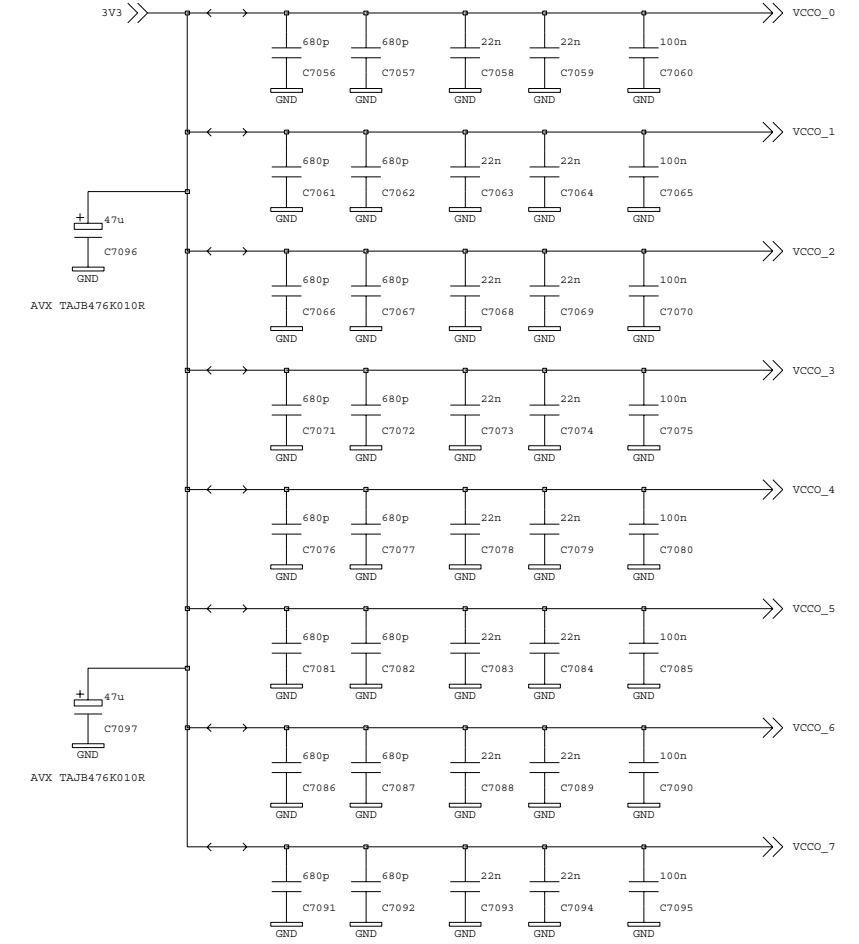
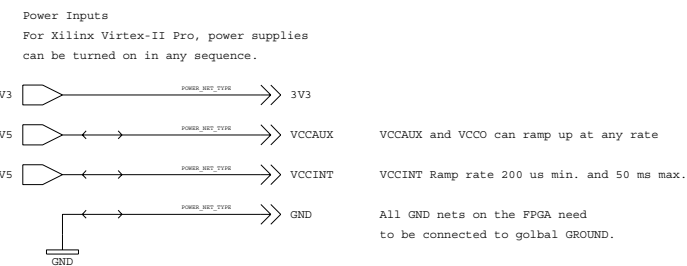
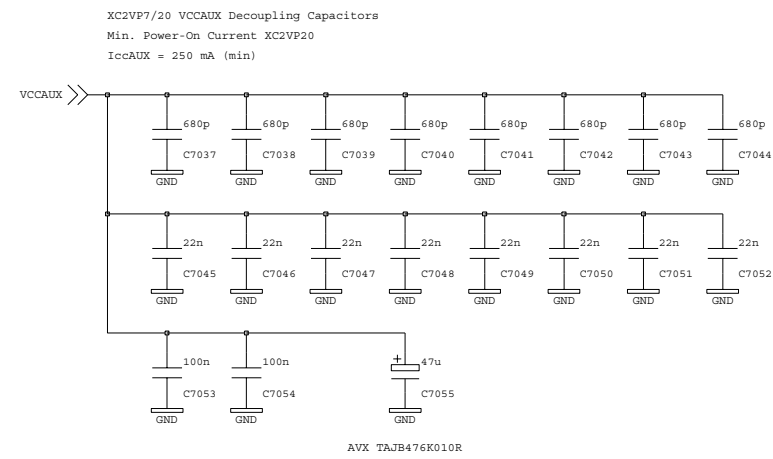
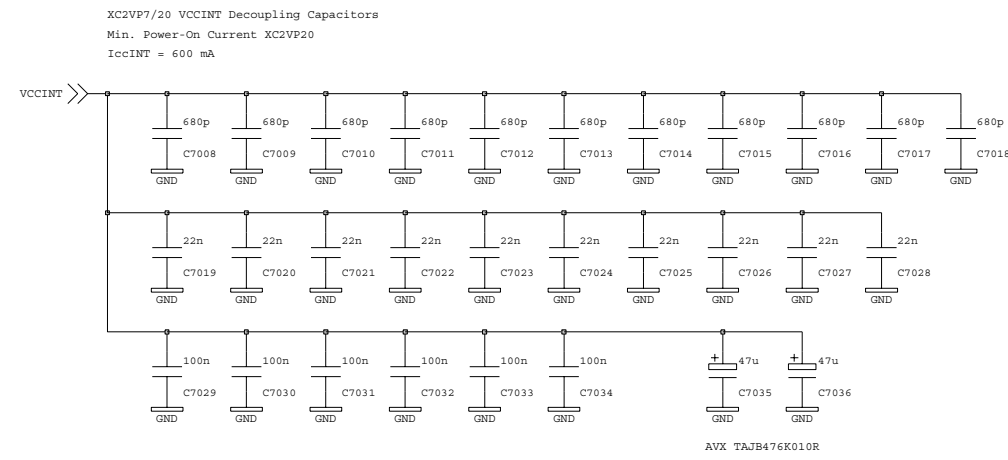
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		Date	7 Feb 2006	
GOL Input		Time	1:50:33 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Dim	420 x 297 mm	
		Page	1 of 6	

IC7004
XC2VP7FF896

	A2 VCCAUX	A3 VRP_2	A4 AVCCAUXK9	A5 VTRXPAD9	A6 AVCCAUXK9	A7 VTRXPAD9	A8 GND	A9 GND	A10 GND	A11 AVCCAUXK7	A12 VTRXPAD7	A13 AVCCAUXK7	A14 VTRXPAD7	A15 VCCAUX	A16 VCCAUX	A17 GOL_RXN	A18 GOL_RKP	A19 GOL_TXP	A20 GOL_TXN	A21 GND	A22 GND	A23 LEDn(0)	A24 LEDn(1)	A25 LEDn(2)	A26 LEDn(3)	A27 GND	A28 VRP_7	A29 VCCAUX	A30 GND	A31 VCCAUX	A32 GND	A33 LEDn(4)	A34 LEDn(5)	A35 GND	A36 LEDn(6)	A37 LEDn(7)	A38 GND	A39 BufCE_n	A40 BufA(19)	A41 C30	A42 C29	A43 C28	A44 C27	A45 BufA(7)	A46 BufA(6)	A47 GND	A48 GND	A49 GND	A50 GND	A51 GND	A52 GND	A53 GND	A54 GND	A55 GND	A56 GND	A57 GND	A58 GND	A59 GND	A60 GND	A61 GND	A62 GND	A63 GND	A64 GND	A65 GND	A66 GND	A67 GND	A68 GND	A69 GND	A70 GND	A71 GND	A72 GND	A73 GND	A74 GND	A75 GND	A76 GND	A77 GND	A78 GND	A79 GND	A80 GND	A81 GND	A82 GND	A83 GND	A84 GND	A85 GND	A86 GND	A87 GND	A88 GND	A89 GND	A90 GND	A91 GND	A92 GND	A93 GND	A94 GND	A95 GND	A96 GND	A97 GND	A98 GND	A99 GND	A100 GND	A101 GND	A102 GND	A103 GND	A104 GND	A105 GND	A106 GND	A107 GND	A108 GND	A109 GND	A110 GND	A111 GND	A112 GND	A113 GND	A114 GND	A115 GND	A116 GND	A117 GND	A118 GND	A119 GND	A120 GND	A121 GND	A122 GND	A123 GND	A124 GND	A125 GND	A126 GND	A127 GND	A128 GND	A129 GND	A130 GND	A131 GND	A132 GND	A133 GND	A134 GND	A135 GND	A136 GND	A137 GND	A138 GND	A139 GND	A140 GND	A141 GND	A142 GND	A143 GND	A144 GND	A145 GND	A146 GND	A147 GND	A148 GND	A149 GND	A150 GND	A151 GND	A152 GND	A153 GND	A154 GND	A155 GND	A156 GND	A157 GND	A158 GND	A159 GND	A160 GND	A161 GND	A162 GND	A163 GND	A164 GND	A165 GND	A166 GND	A167 GND	A168 GND	A169 GND	A170 GND	A171 GND	A172 GND	A173 GND	A174 GND	A175 GND	A176 GND	A177 GND	A178 GND	A179 GND	A180 GND	A181 GND	A182 GND	A183 GND	A184 GND	A185 GND	A186 GND	A187 GND	A188 GND	A189 GND	A190 GND	A191 GND	A192 GND	A193 GND	A194 GND	A195 GND	A196 GND	A197 GND	A198 GND	A199 GND	A200 GND	A201 GND	A202 GND	A203 GND	A204 GND	A205 GND	A206 GND	A207 GND	A208 GND	A209 GND	A210 GND	A211 GND	A212 GND	A213 GND	A214 GND	A215 GND	A216 GND	A217 GND	A218 GND	A219 GND	A220 GND	A221 GND	A222 GND	A223 GND	A224 GND	A225 GND	A226 GND	A227 GND	A228 GND	A229 GND	A230 GND	A231 GND	A232 GND	A233 GND	A234 GND	A235 GND	A236 GND	A237 GND	A238 GND	A239 GND	A240 GND	A241 GND	A242 GND	A243 GND	A244 GND	A245 GND	A246 GND	A247 GND	A248 GND	A249 GND	A250 GND	A251 GND	A252 GND	A253 GND	A254 GND	A255 GND	A256 GND	A257 GND	A258 GND	A259 GND	A260 GND	A261 GND	A262 GND	A263 GND	A264 GND	A265 GND	A266 GND	A267 GND	A268 GND	A269 GND	A270 GND	A271 GND	A272 GND	A273 GND	A274 GND	A275 GND	A276 GND	A277 GND	A278 GND	A279 GND	A280 GND	A281 GND	A282 GND	A283 GND	A284 GND	A285 GND	A286 GND	A287 GND	A288 GND	A289 GND	A290 GND	A291 GND	A292 GND	A293 GND	A294 GND	A295 GND	A296 GND	A297 GND	A298 GND	A299 GND	A300 GND	A301 GND	A302 GND	A303 GND	A304 GND	A305 GND	A306 GND	A307 GND	A308 GND	A309 GND	A310 GND	A311 GND	A312 GND	A313 GND	A314 GND	A315 GND	A316 GND	A317 GND	A318 GND	A319 GND	A320 GND	A321 GND	A322 GND	A323 GND	A324 GND	A325 GND	A326 GND	A327 GND	A328 GND	A329 GND	A330 GND	A331 GND	A332 GND	A333 GND	A334 GND	A335 GND	A336 GND	A337 GND	A338 GND	A339 GND	A340 GND	A341 GND	A342 GND	A343 GND	A344 GND	A345 GND	A346 GND	A347 GND	A348 GND	A349 GND	A350 GND	A351 GND	A352 GND	A353 GND	A354 GND	A355 GND	A356 GND	A357 GND	A358 GND	A359 GND	A360 GND	A361 GND	A362 GND	A363 GND	A364 GND	A365 GND	A366 GND	A367 GND	A368 GND	A369 GND	A370 GND	A371 GND	A372 GND	A373 GND	A374 GND	A375 GND	A376 GND	A377 GND	A378 GND	A379 GND	A380 GND	A381 GND	A382 GND	A383 GND	A384 GND	A385 GND	A386 GND	A387 GND	A388 GND	A389 GND	A390 GND	A391 GND	A392 GND	A393 GND	A394 GND	A395 GND	A396 GND	A397 GND	A398 GND	A399 GND	A400 GND	A401 GND	A402 GND	A403 GND	A404 GND	A405 GND	A406 GND	A407 GND	A408 GND	A409 GND	A410 GND	A411 GND	A412 GND	A413 GND	A414 GND	A415 GND	A416 GND	A417 GND	A418 GND	A419 GND	A420 GND	A421 GND	A422 GND	A423 GND	A424 GND	A425 GND	A426 GND	A427 GND	A428 GND	A429 GND	A430 GND	A431 GND	A432 GND	A433 GND	A434 GND	A435 GND	A436 GND	A437 GND	A438 GND	A439 GND	A440 GND	A441 GND	A442 GND	A443 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GND	A555 GND	A556 GND	A557 GND	A558 GND	A559 GND	A560 GND	A561 GND	A562 GND	A563 GND	A564 GND	A565 GND	A566 GND	A567 GND	A568 GND	A569 GND	A570 GND	A571 GND	A572 GND	A573 GND	A574 GND	A575 GND	A576 GND	A577 GND	A578 GND	A579 GND	A580 GND	A581 GND	A582 GND	A583 GND	A584 GND	A585 GND	A586 GND	A587 GND	A588 GND	A589 GND	A590 GND	A591 GND	A592 GND	A593 GND	A594 GND	A595 GND	A596 GND	A597 GND	A598 GND	A599 GND	A600 GND	A601 GND	A602 GND	A603 GND	A604 GND	A605 GND	A606 GND	A607 GND	A608 GND	A609 GND	A610 GND	A611 GND	A612 GND	A613 GND	A614 GND	A615 GND	A616 GND	A617 GND	A618 GND	A619 GND	A620 GND	A621 GND	A622 GND	A623 GND	A624 GND	A625 GND	A626 GND	A627 GND	A628 GND	A629 GND	A630 GND	A631 GND	A632 GND	A633 GND	A634 GND	A635 GND	A636 GND	A637 GND	A638 GND	A639 GND	A640 GND	A641 GND	A642 GND	A643 GND	A644 GND	A645 GND	A646 GND	A647 GND	A648 GND	A649 GND	A650 GND	A651 GND	A652 GND	A653 GND	A654 GND	A655 GND	A656 GND	A657 GND	A658 GND	A659 GND	A660 GND	A661 GND	A662 GND	A663 GND	A664 GND	A665 GND	A666 GND	A667 GND	A668 GND	A669 GND	A670 GND	A671 GND	A672 GND	A673 GND	A674 GND	A675 GND	A676 GND	A677 GND	A678 GND	A679 GND	A680 GND	A681 GND	A682 GND	A683 GND	A684 GND	A685 GND	A686 GND	A687 GND	A688 GND	A689 GND	A690 GND	A691 GND	A692 GND	A693 GND	A694 GND	A695 GND	A696 GND	A697 GND	A698 GND	A699 GND	A700 GND	A701 GND	A702 GND	A703 GND	A704 GND	A705 GND	A706 GND	A707 GND	A708 GND	A709 GND	A710 GND	A711 GND	A712 GND	A713 GND	A714 GND	A715 GND	A716 GND	A717 GND	A718 GND	A719 GND	A720 GND	A721 GND	A722 GND	A723 GND	A724 GND	A725 GND	A726 GND	A727 GND	A728 GND	A729 GND	A730 GND	A731 GND	A732 GND	A733 GND	A734 GND	A735 GND	A736 GND	A737 GND	A738 GND	A739 GND	A740 GND	A741 GND	A742 GND	A743 GND	A744 GND	A745 GND	A746 GND	A747 GND	A748 GND	A749 GND	A750 GND	A751 GND	A752 GND	A753 GND	A754 GND	A755 GND	A756 GND	A757 GND	A758 GND	A759 GND	A760 GND	A761 GND	A762 GND	A763 GND	A764 GND	A765 GND	A766 GND	A767 GND	A768 GND	A769 GND	A770 GND	A771 GND	A772 GND	A773 GND	A774 GND	A775 GND	A776 GND	A777 GND	A778 GND	A779 GND	A780 GND	A781 GND	A782 GND	A783 GND	A784 GND	A785 GND	A786 GND	A787 GND	A788 GND	A789 GND	A790 GND	A791 GND	A792 GND	A793 GND	A794 GND	A795 GND	A796 GND	A797 GND	A798 GND	A799 GND	A800 GND	A801 GND	A802 GND	A803 GND	A804 GND	A805 GND	A806 GND	A807 GND	A808 GND	A809 GND	A810 GND	A811 GND	A812 GND	A813 GND	A814 GND	A815 GND	A816 GND	A817 GND	A818 GND	A819 GND	A820 GND	A821 GND	A822 GND	A823 GND	A824 GND	A825 GND	A826 GND	A827 GND	A828 GND	A829 GND	A830 GND	A831 GND	A832 GND	A833 GND	A834 GND	A835 GND	A836 GND	A837 GND	A838 GND	A839 GND	A840 GND	A841 GND	A842 GND	A843 GND	A844 GND	A845 GND	A846 GND	A847 GND	A848 GND	A849 GND	A850 GND	A851 GND	A852 GND	A853 GND	A854 GND	A855 GND	A856 GND	A857 GND	A858 GND	A859 GND	A860 GND	A861 GND	A862 GND	A863 GND	A864 GND	A865 GND	A866 GND	A867 GND	A868 GND	A869 GND	A870 GND	A871 GND	A872 GND	A873 GND	A874 GND	A875 GND	A876 GND	A877 GND	A878 GND	A879 GND	A880 GND	A881 GND	A882 GND	A883 GND	A884 GND	A885 GND	A886 GND	A887 GND	A888 GND	A889 GND	A890 GND	A891 GND	A892 GND	A893 GND	A894 GND	A895 GND	A896 GND	A897 GND	A898 GND	A899 GND	A900 GND	A901 GND	A902 GND	A903 GND	A904 GND	A905 GND	A906 GND	A907 GND	A908 GND	A909 GND	A910 GND	A911 GND	A912 GND	A913 GND	A914 GND	A915 GND	A916 GND	A917 GND	A918 GND	A919 GND	A920 GND	A921 GND	A922 GND	A923 GND	A924 GND	A925 GND	A926 GND	A927 GND	A928 GND	A929 GND	A930 GND	A931 GND	A932 GND	A933 GND	A934 GND	A935 GND	A936 GND	A937 GND	A938 GND	A939 GND	A940 GND	A941 GND	A942 GND	A943 GND	A944 GND	A945 GND	A946 GND	A947 GND	A948 GND	A949 GND	A950 GND	A951 GND	A952 GND	A953 GND	A954 GND	A955 GND	A956 GND	A957 GND	A958 GND	A959 GND	A960 GND	A961 GND	A962 GND	A963 GND	A964 GND	A965 GND	A966 GND	A967 GND	A968 GND	A969 GND	A970 GND	A971 GND	A972 GND	A973 GND	A974 GND	A975 GND	A976 GND	A977 GND	A978 GND	A979 GND	A980 GND	A981 GND	A982 GND	A983 GND	A984 GND	A985 GND	A986 GND	A987 GND	A988 GND	A989 GND	A990 GND	A991 GND	A992 GND	A993 GND	A994 GND	A995 GND	A996 GND	A997 GND	A998 GND	A999 GND	A1000 GND
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Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

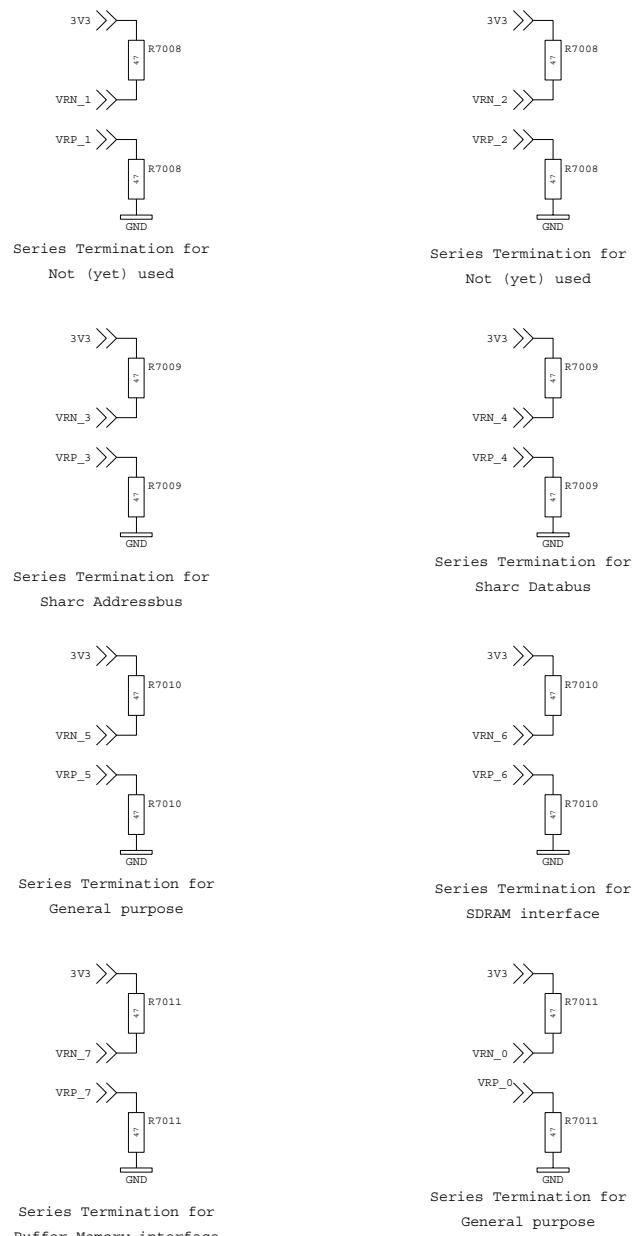
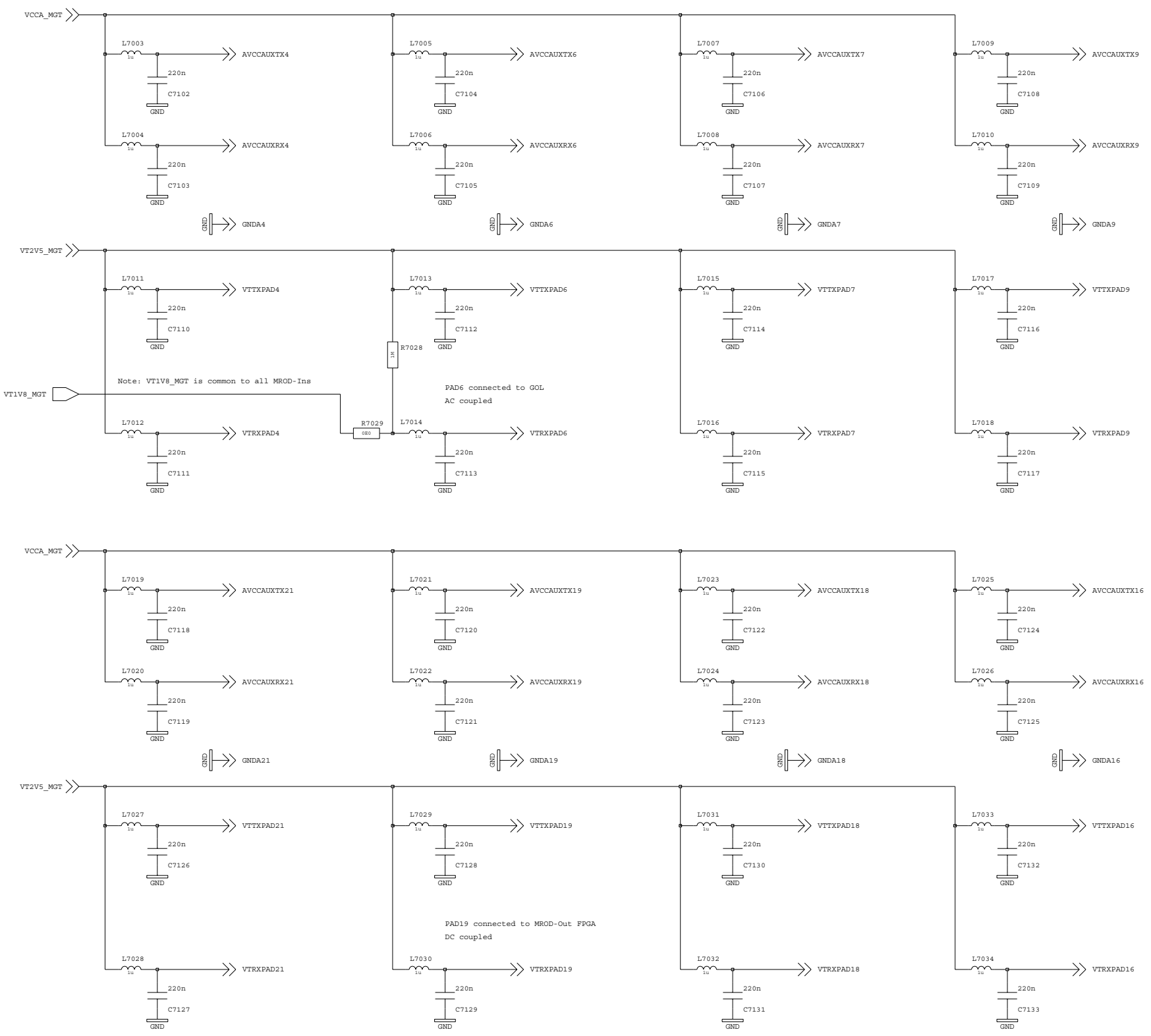
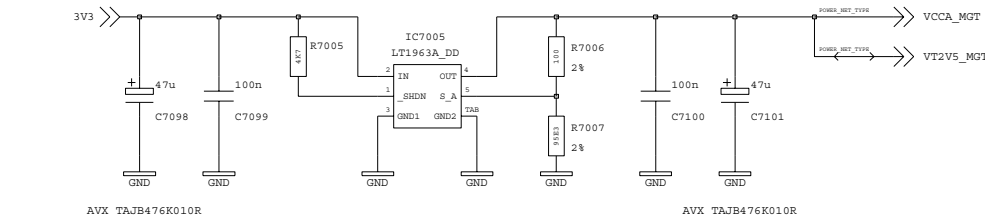
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Input FPGA		Time 1:50:53 pm		
Proj: MROD-X		Name tonvr		
Peter Jansweijer		peterj@nikhef.nl		
NIKHE				



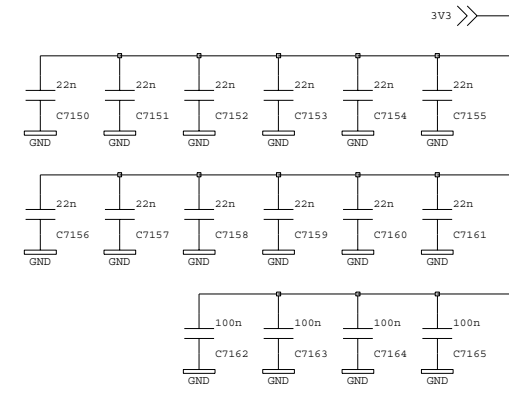
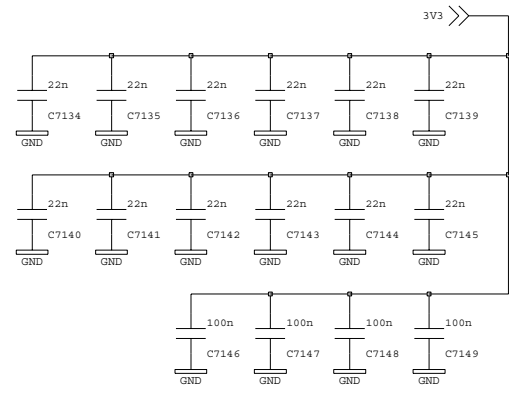
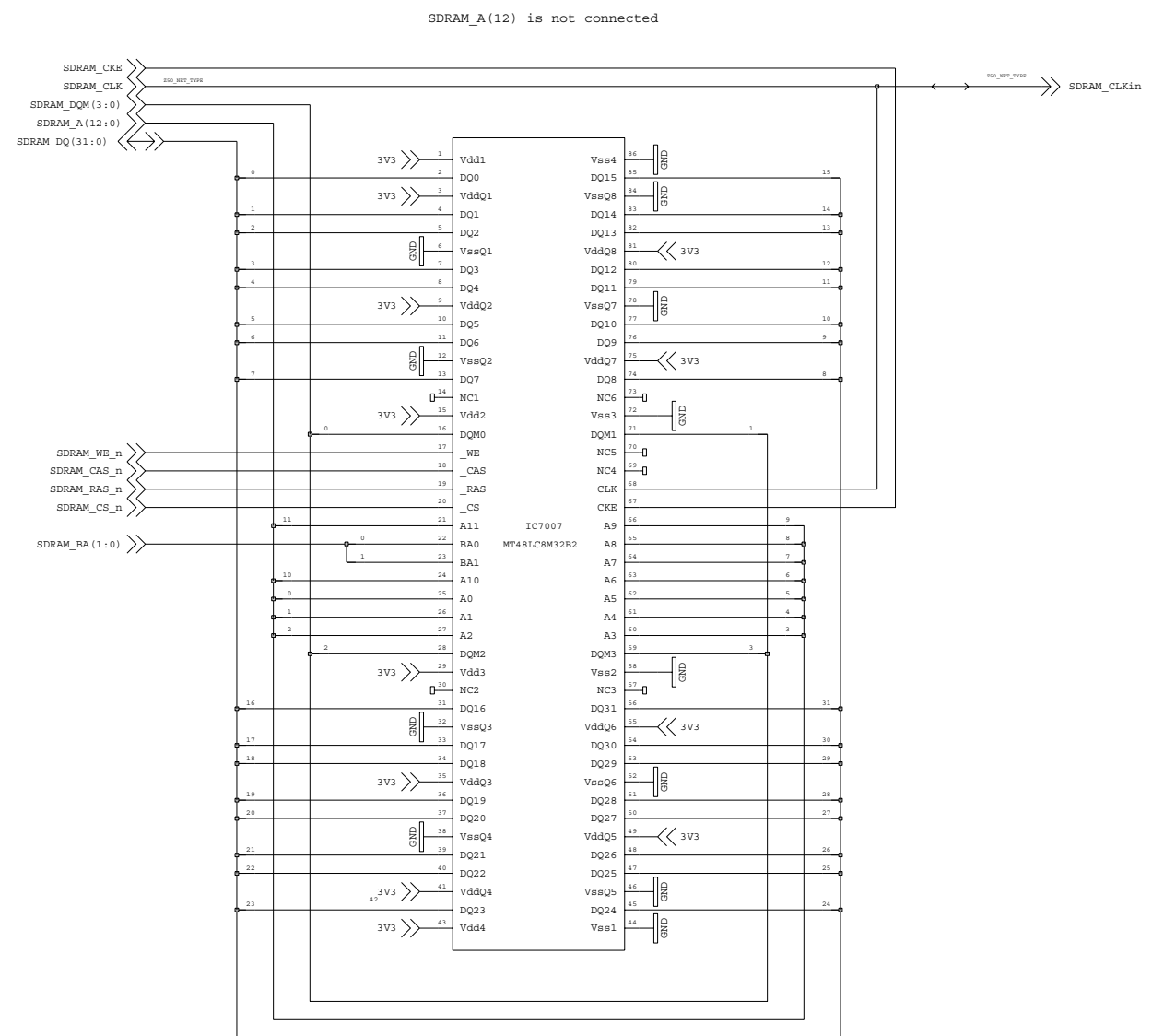
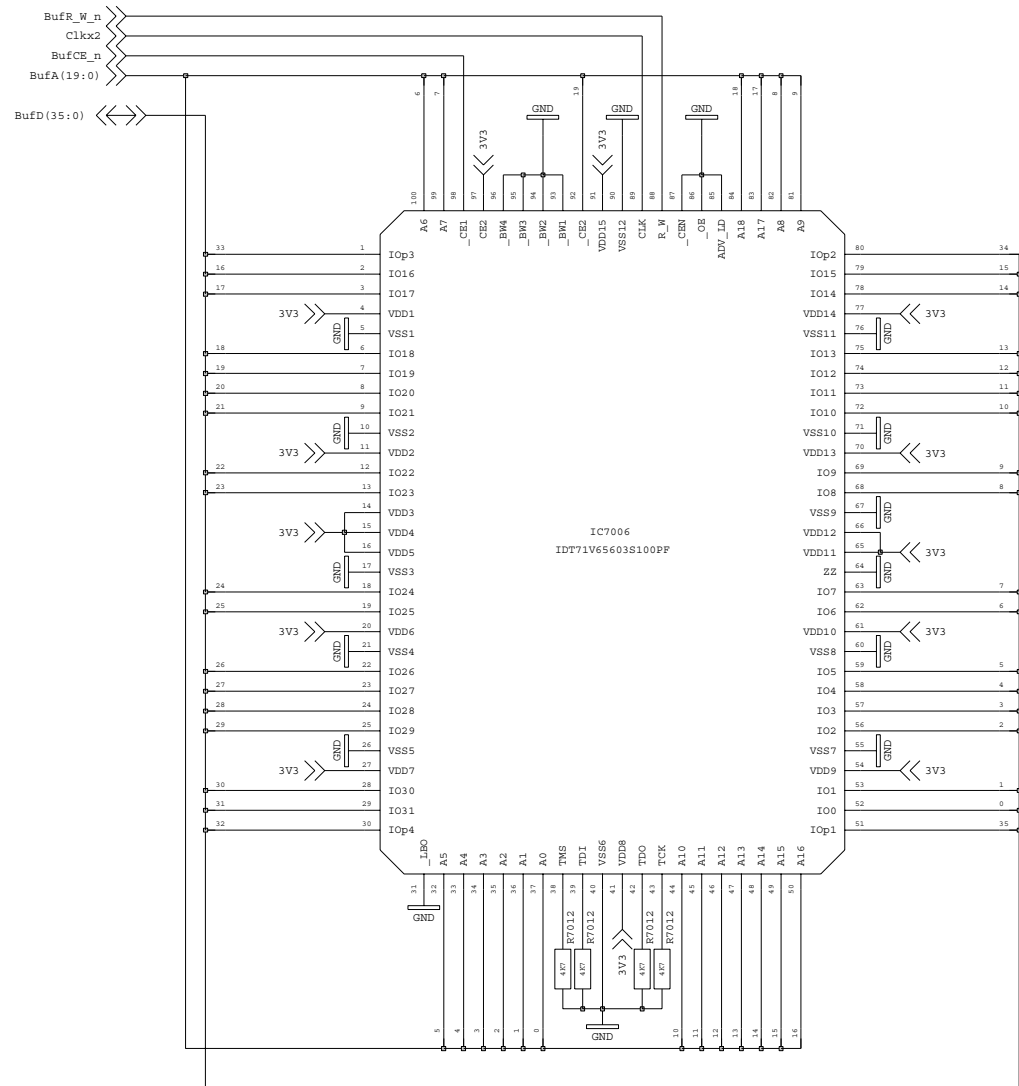
channel_in		Rev	V2	2
Input FPGA Power Supply Decoupling		Date	7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time	1:51:34 pm	
Peter Jansweijer	peterj@nikhef.nl	Name	Ton van Reen	
NIKHEF <small>© ET-Nikhef Amsterdam</small>		<small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	3	of 6

2V5 @ 1,5A

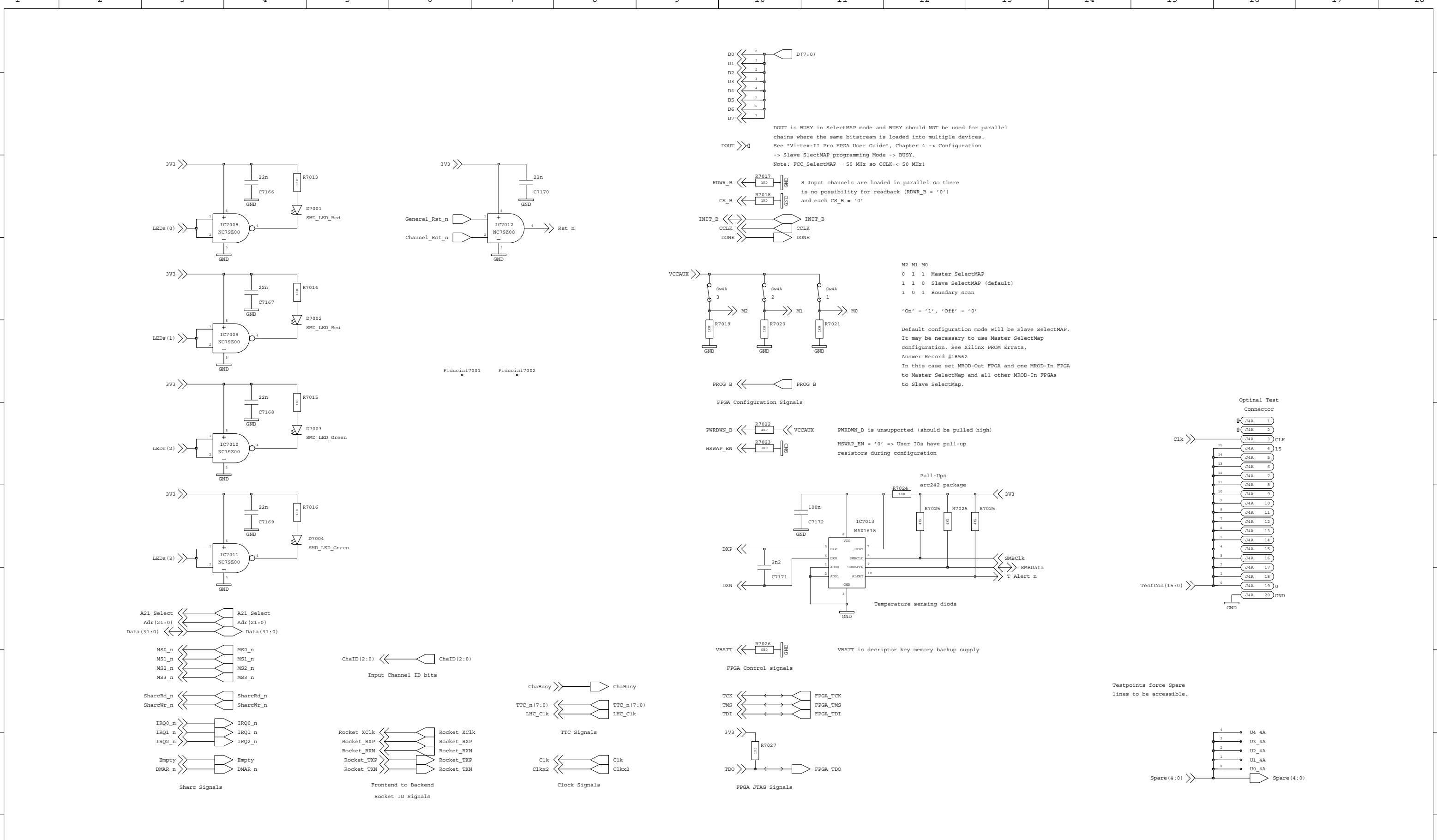
=> MGT Power (estimated 31 + 49 = 80 mA)
=> MGT TX (RX) Termination (estimated 11 mA)



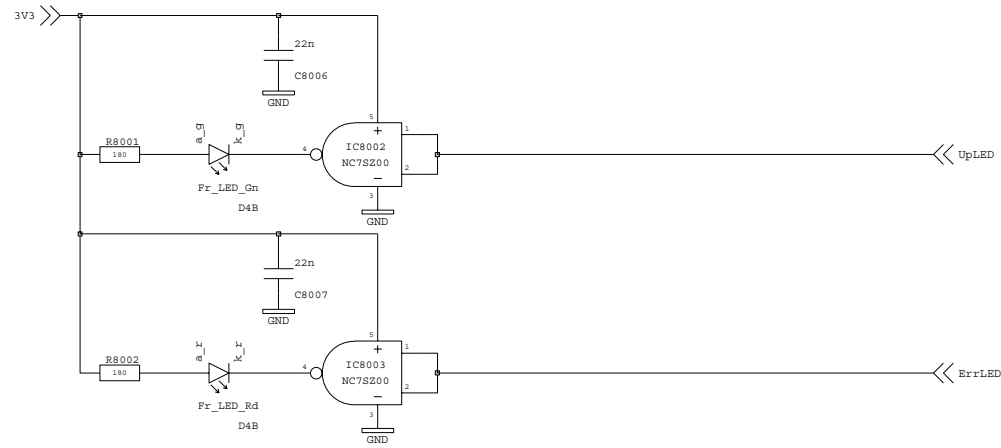
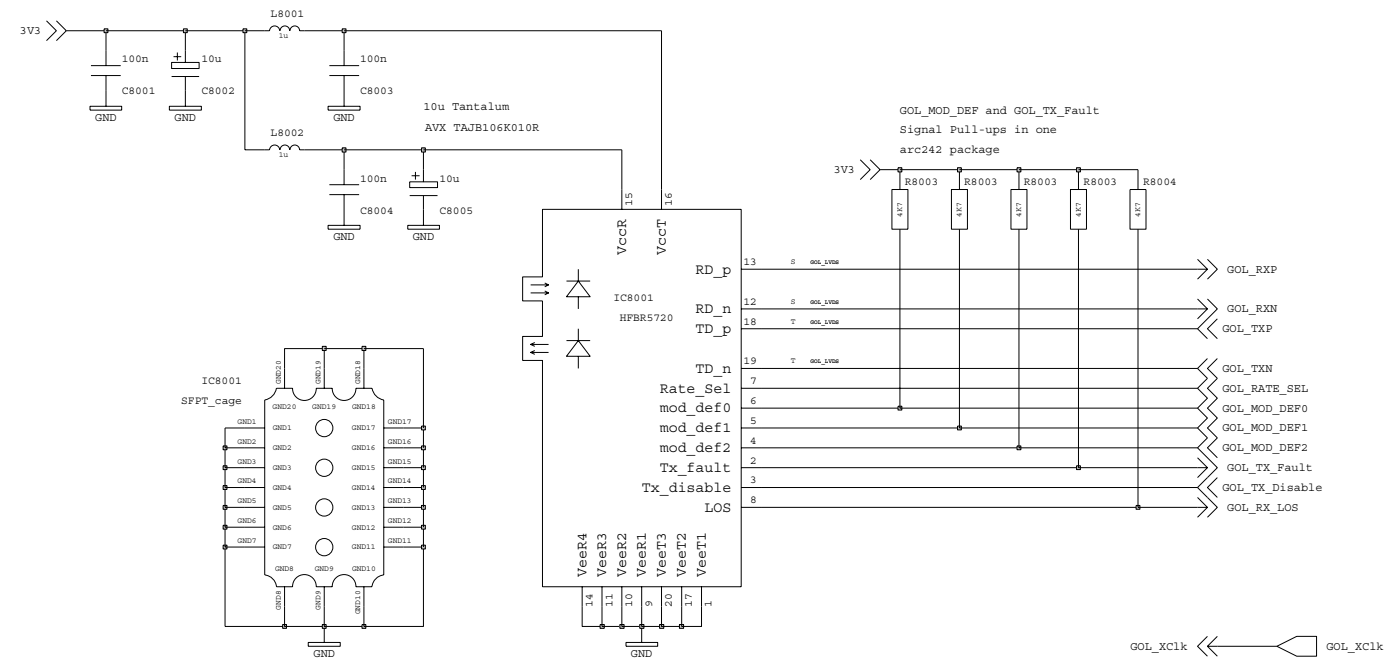
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time	1:52:01 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	4	of 6



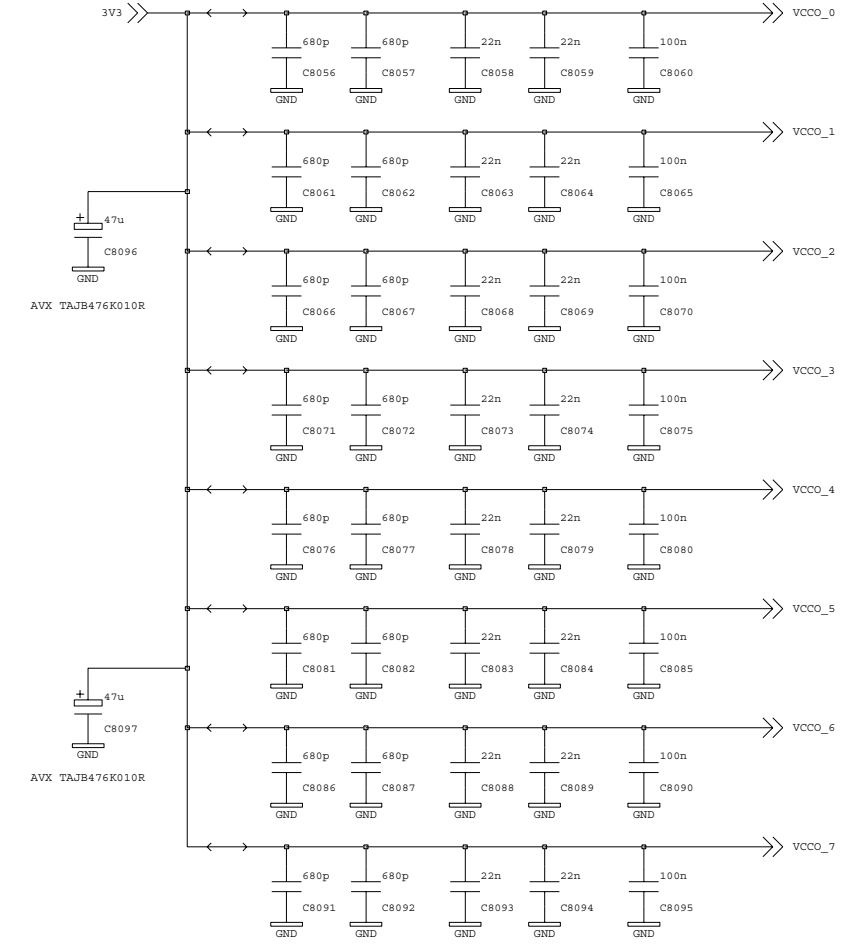
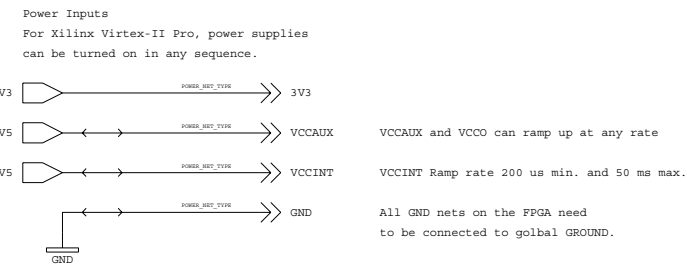
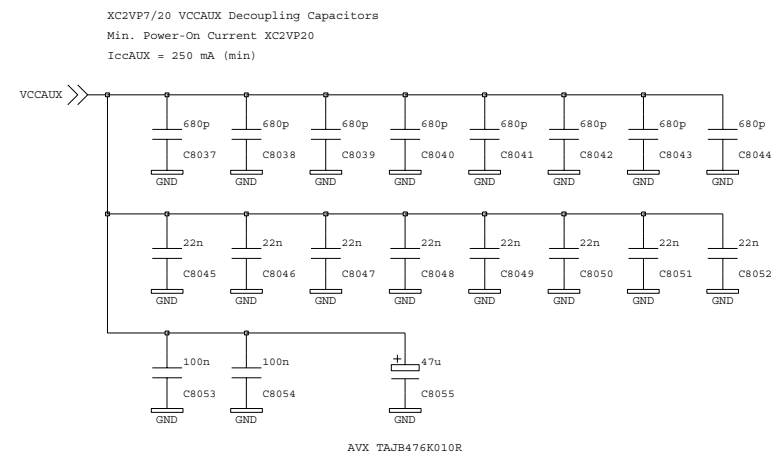
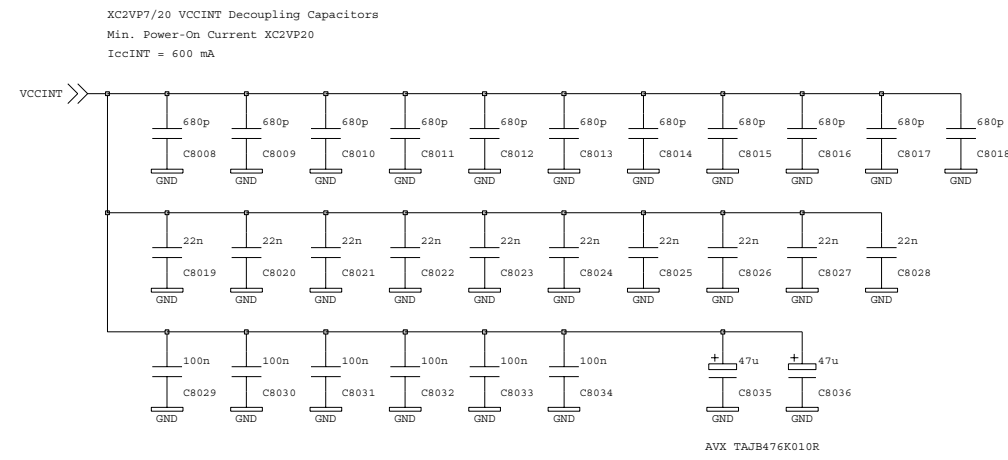
channel_in		Rev	V2	2
		Date	7 Feb 2006	
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
Size	A3	4 1 4 A		
Dim	420 x 297 mm			
Page	5 of 6			



channel_in		Rev	V2 2
Input FPGA Auxiliary Connections		Date	7 Feb 2006
Proj: MROD-X		Time	1:53:04 pm
Proj.No: 38405		Name	Ton van Reen
Peter Jansweijer		peterj@nikhef.nl	
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Size	A3 4 1 4 A
		Dim	420 x 297 mm
		Page	6 of 6



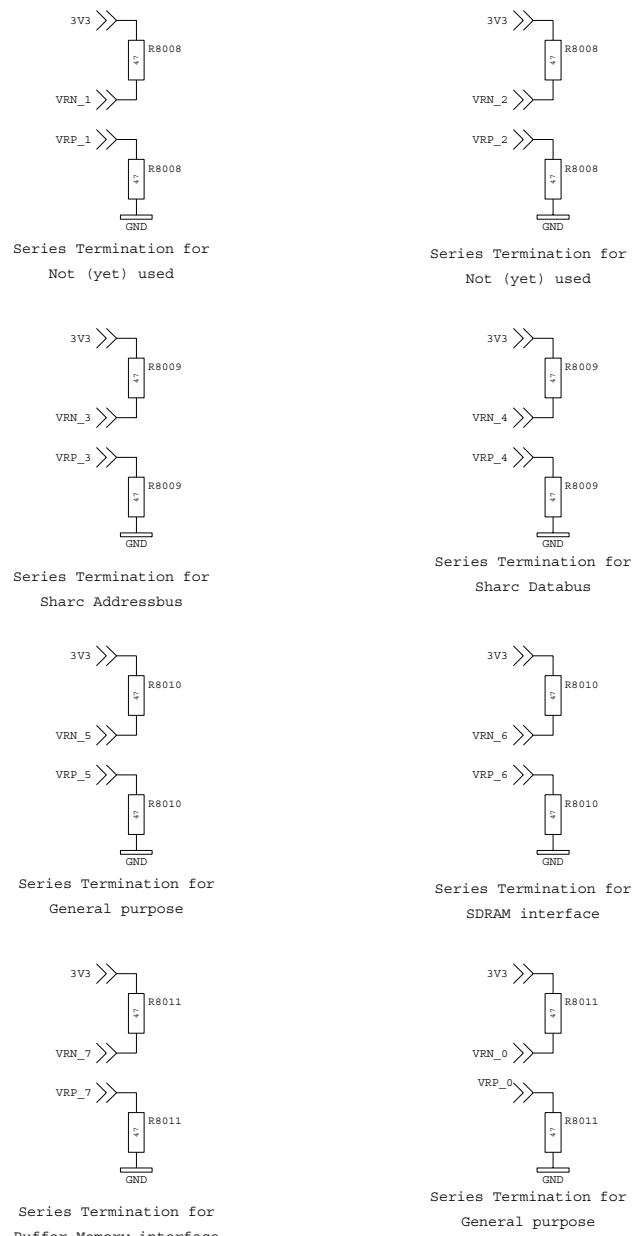
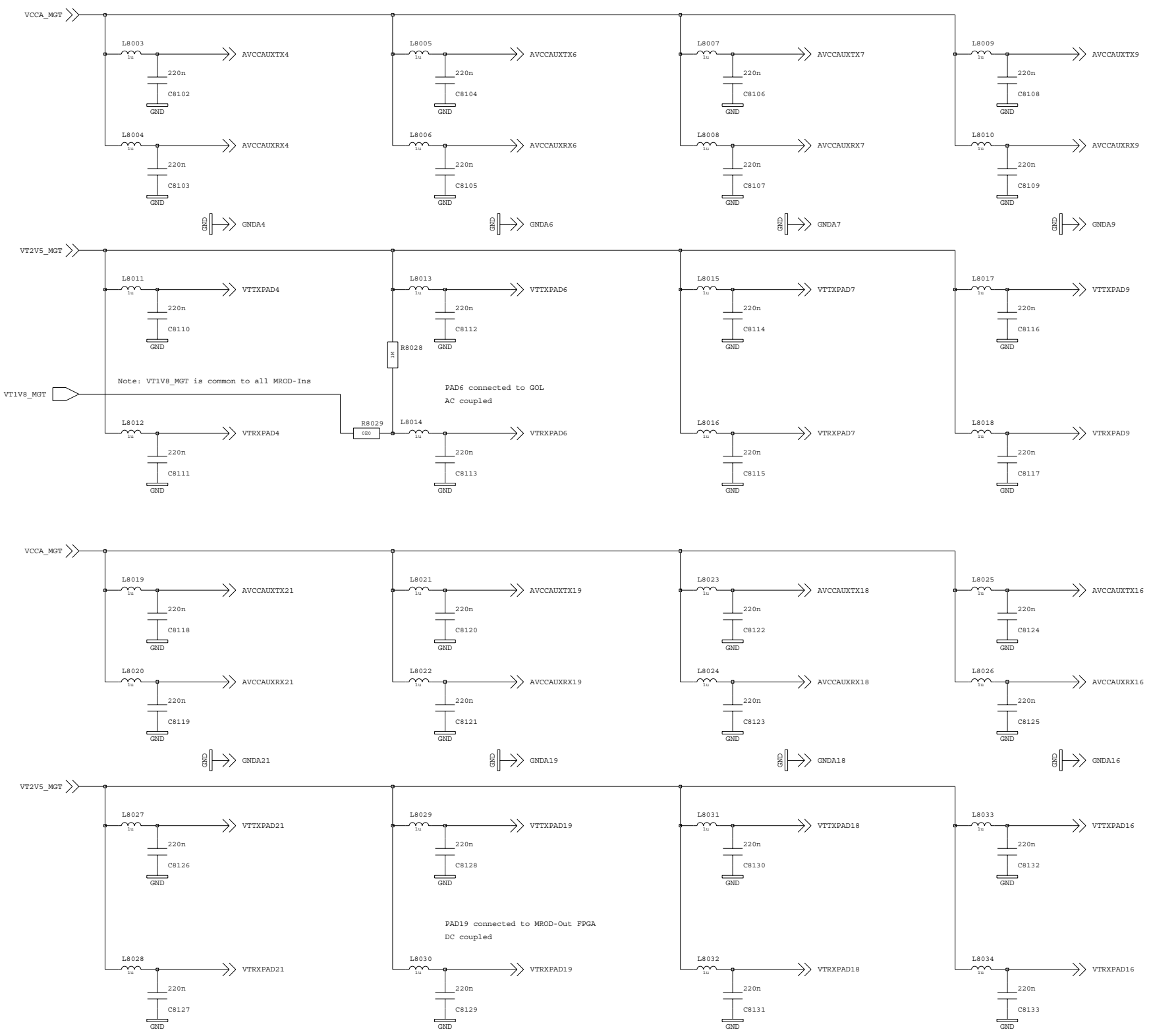
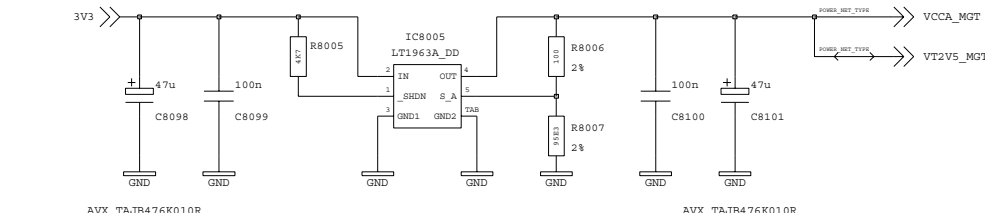
channel_in		Rev	V2	2
		Date	7 Feb 2006	
GOL Input		Time	1:50:33 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF <small>© ET-Nikhef Amsterdam</small>	<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Size	A3 4 1 4 A
			Dim	420 x 297 mm
			Page	1 of 6



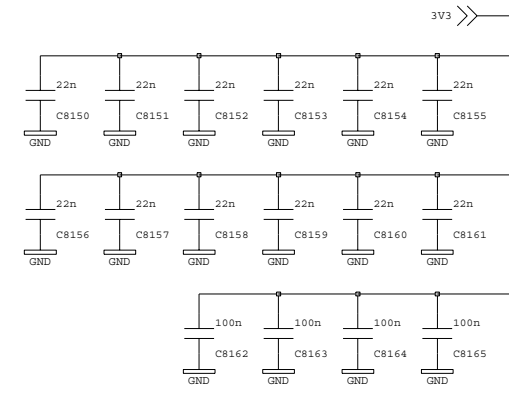
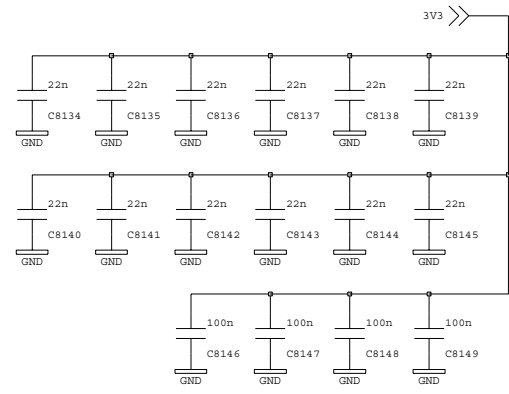
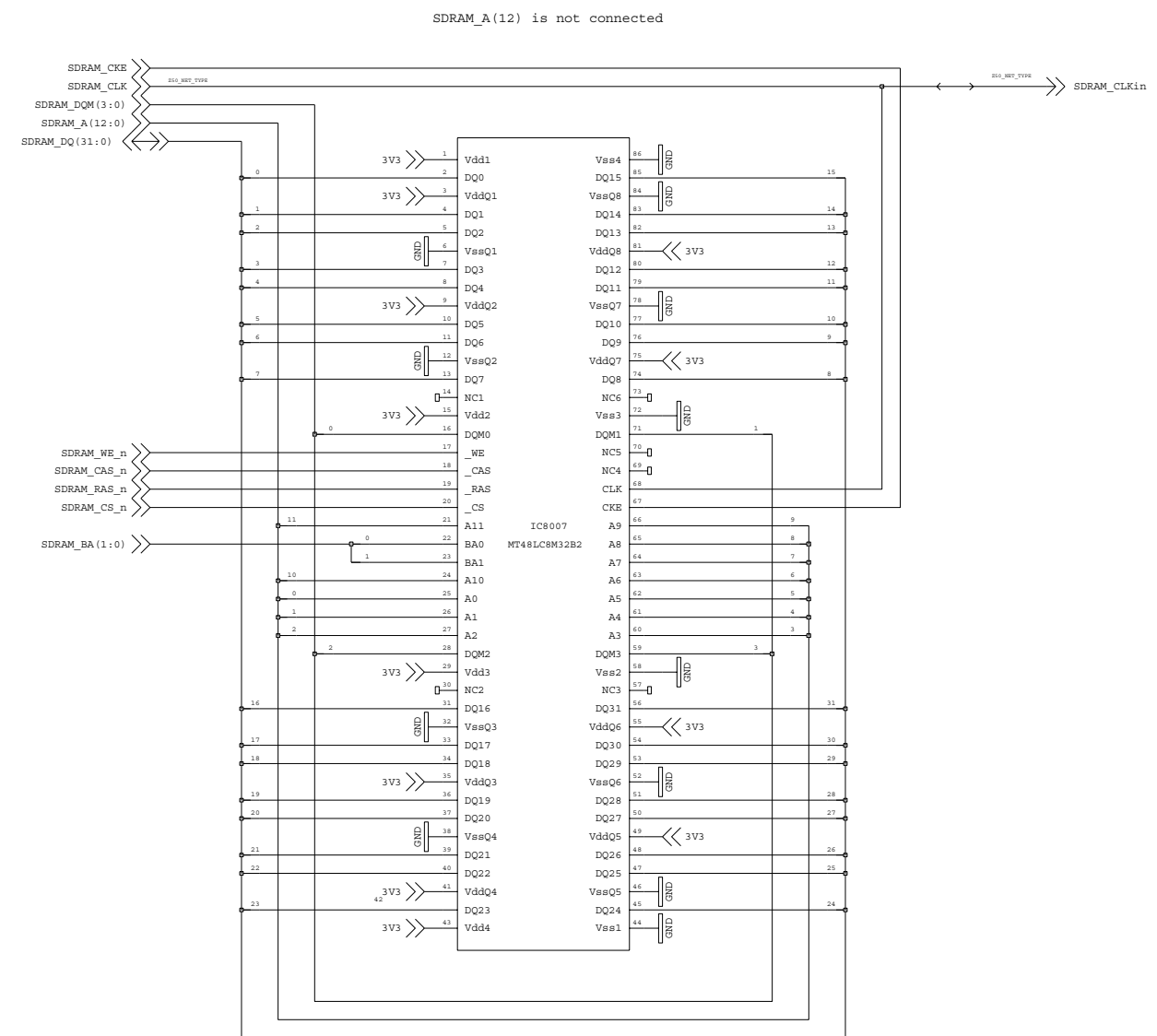
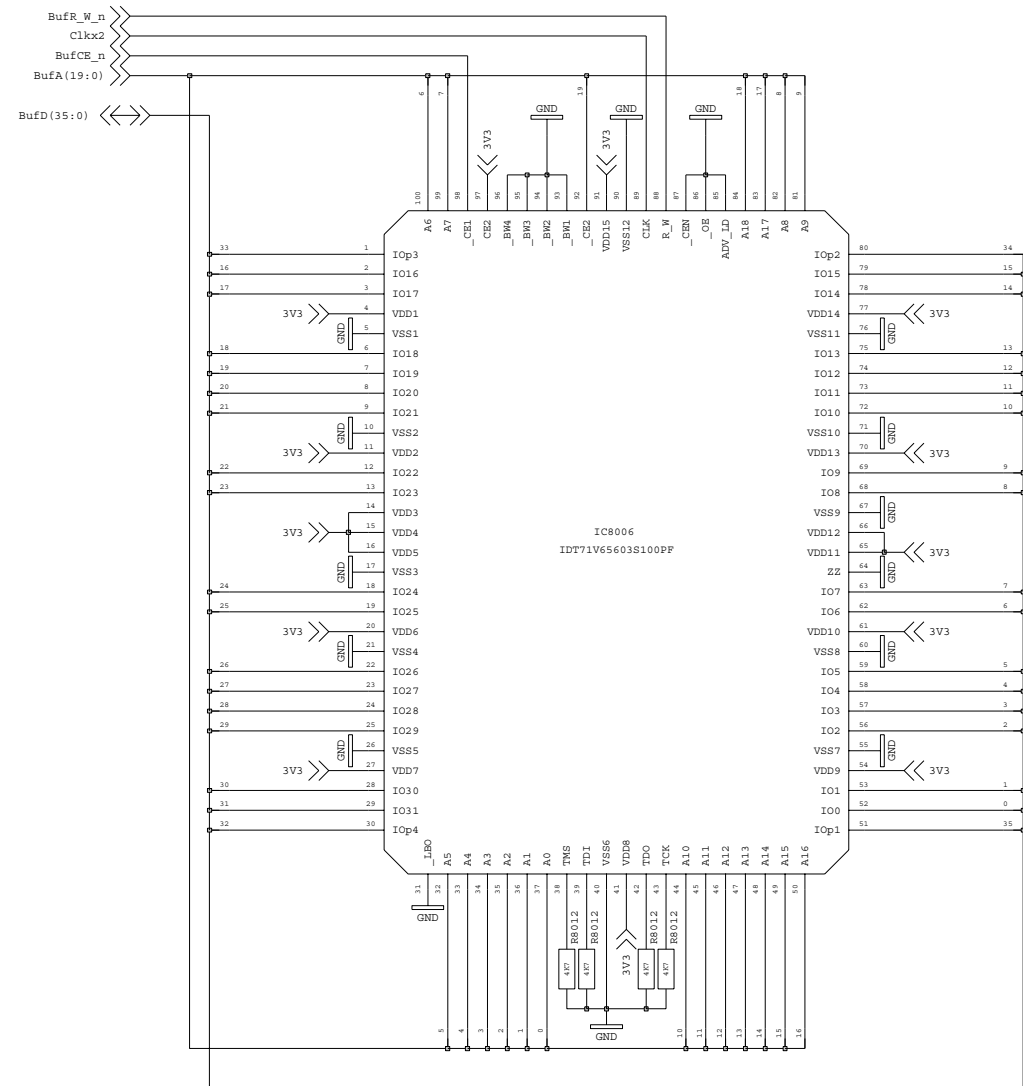
channel_in		Rev	V2	2			
		Date	7 Feb 2006				
Input FPGA Power Supply Decoupling		Time	1:51:34 pm				
Proj:	MROD-X	Proj.No:	38405				
Peter Jansweijer		peterj@nikhef.nl					
NIKHEF <small>© ET-Nikhef Amsterdam</small>		<small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>					
					Size	A3	4 1 4 A
					Dim	420 x 297 mm	
Page		3	of	6			

2V5 @ 1,5A

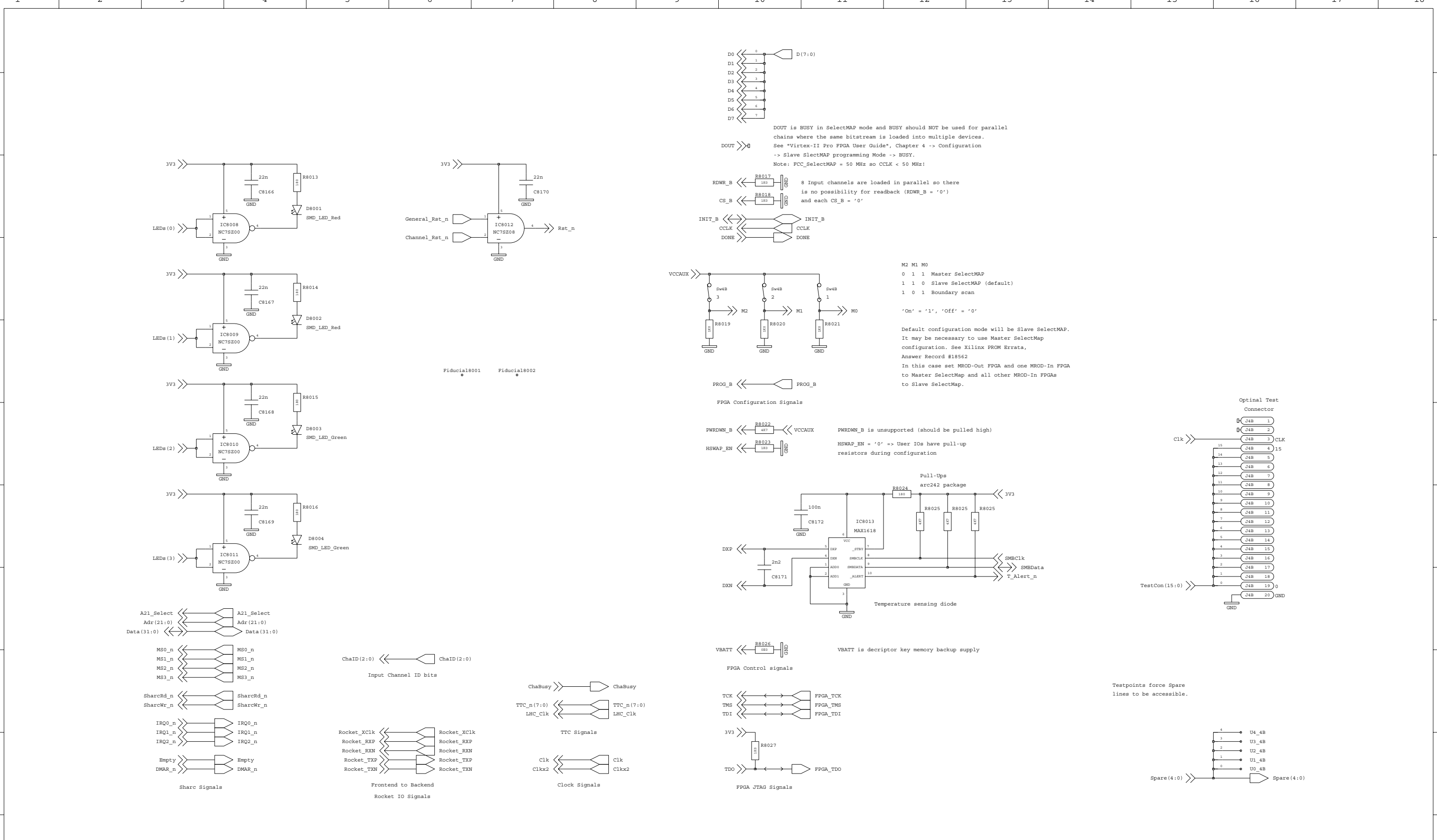
=> MGT Power (estimated 31 + 49 = 80 mA)
=> MGT TX (RX) Termination (estimated 11 mA)



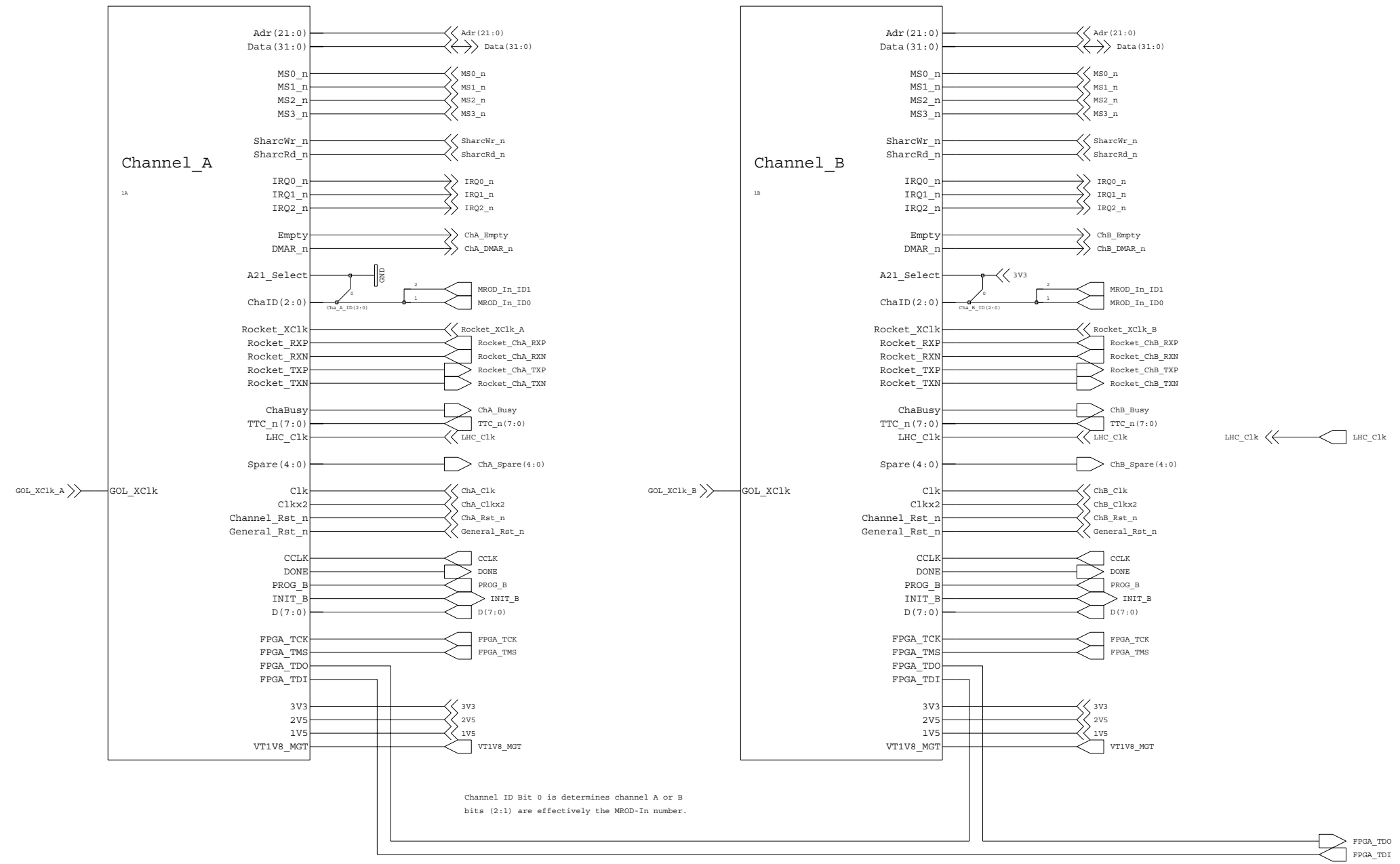
channel_in		Rev V2 2
		Date 7 Feb 2006
Input FPGA MGT Pwr Decoupling, Termination		Time 1:52:01 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF © NIKHEF Amsterdam		Size A3 4 1 4 A
		Dim 420 x 297 mm
		Page 4 of 6
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		



channel_in		Rev	V2	2
		Date	7 Feb 2006	
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © T-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	5	of 6



channel_in		Rev V2 2
		Date 7 Feb 2006
Input FPGA Auxiliary Connections		Time 1:53:04 pm
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Size A3 4 1 4 A
		Dim 420 x 297 mm
		Page 6 of 6



MROD- In		Rev	V2	2
		Date	7 Feb 2006	
Input Channels		Time	1:45:51 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl			
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	1 of 4	

IC101
ADSP21160N

A1	DATA(14)	A2	DATA(13)	A3	DATA(10)	A4	DATA(8)	A5	DATA(4)	A6	DATA(2)	A7	TDI	A8	TRST_n	A9	RESET_n	A10	PPBA	A11	IRQ0_n	A12	FLAG1	A13	TMEXP	A14	NC_A14	A15	NC_A15	A16	TPP1	A17	RFS1	A18	RCLK1	A19	DT0	A20	LOGAT(4)
B1	DATA(22)	B2	DATA(16)	B3	DATA(15)	B4	DATA(9)	B5	DATA(6)	B6	DATA(3)	B7	DATA(0)	B8	TCK	B9	Sharc_BMU_n	B10	IRQ2_n	B11	ChB_Empty	B12	FLAG2	B13	NC_B13	B14	NC_B14	B15	DT1	B16	RCLK1	B17	RFS0	B18	TCCLK	B19	LOGAT(5)	B20	LOGAT(2)
C1	DATA(24)	C2	DATA(18)	C3	DATA(17)	C4	DATA(11)	C5	DATA(7)	C6	DATA(5)	C7	DATA(1)	C8	TMS	C9	TDO	C10	IRQ1_n	C11	ChA_Empty	C12	NC_C12	C13	NC_C13	C14	TCCLK	C15	DT1	C16	DT0	C17	LOGAT(7)	C18	LOGAT(6)	C19	LOGAT(3)	C20	LOGAT(0)
D1	DATA(28)	D2	DATA(25)	D3	DATA(20)	D4	DATA(19)	D5	DATA(12)	D6	VDDINT_06	D7	VDDINT_07	D8	VDDINT_08	D9	VDDINT_09	D10	VDDINT_10	D11	VDDINT_11	D12	VDDINT_12	D13	VDDINT_13	D14	VDDINT_14	D15	TPP0	D16	L1DAT(7)	D17	LOCLK	D18	LOGAT(3)	D19	LOGAT(1)	D20	L1CLK
E1	DATA(30)	E2	DATA(29)	E3	DATA(23)	E4	DATA(21)	E5	VDDINT_05	E6	VDDINT_04	E7	VDDINT_03	E8	VDDINT_02	E9	VDDINT_01	E10	VDDINT_00	E11	GND	E12	VDDINT_15	E13	VDDINT_16	E14	VDDINT_17	E15	VDDINT_18	E16	VDDINT_19	E17	L1DAT(6)	E18	L1DAT(5)	E19	L1ACK	E20	L1DAT(1)
F1	DATA(34)	F2	DATA(33)	F3	DATA(27)	F4	DATA(26)	F5	VDDINT_05	F6	VDDINT_04	F7	GND_07	F8	GND_08	F9	GND_09	F10	GND_10	F11	GND_11	F12	GND_12	F13	GND_13	F14	GND_14	F15	VDDINT_15	F16	VDDINT_16	F17	L1DAT(4)	F18	L1DAT(3)	F19	L1DAT(0)	F20	L2DAT(7)
G1	DATA(38)	G2	DATA(35)	G3	DATA(32)	G4	DATA(31)	G5	VDDINT_05	G6	VDDINT_04	G7	GND_07	G8	GND_08	G9	GND_09	G10	GND_10	G11	GND_11	G12	GND_12	G13	GND_13	G14	GND_14	G15	VDDINT_15	G16	VDDINT_16	G17	L1DAT(2)	G18	L2DAT(6)	G19	L2DAT(4)	G20	L2CLK
H1	DATA(40)	H2	DATA(39)	H3	DATA(37)	H4	DATA(34)	H5	VDDINT_05	H6	VDDINT_04	H7	GND_07	H8	GND_08	H9	GND_09	H10	GND_10	H11	GND_11	H12	GND_12	H13	GND_13	H14	GND_14	H15	VDDINT_15	H16	VDDINT_16	H17	L1DAT(2)	H18	L2DAT(6)	H19	L2DAT(4)	H20	L2CLK
I1	DATA(44)	I2	DATA(43)	I3	DATA(42)	I4	DATA(41)	I5	VDDINT_05	I6	VDDINT_04	I7	GND_07	I8	GND_08	I9	GND_09	I10	GND_10	I11	GND_11	I12	GND_12	I13	GND_13	I14	GND_14	I15	VDDINT_15	I16	VDDINT_16	I17	L1DAT(2)	I18	L2DAT(2)	I19	HBG_n	I20	VDDINT
J1	DATA(48)	J2	DATA(47)	J3	DATA(46)	J4	DATA(45)	J5	VDDINT_05	J6	VDDINT_04	J7	GND_07	J8	GND_08	J9	GND_09	J10	GND_10	J11	GND_11	J12	GND_12	J13	GND_13	J14	GND_14	J15	VDDINT_15	J16	VDDINT_16	J17	L1DAT(2)	J18	L2DAT(2)	J19	HBG_n	J20	VDDINT
K1	CLK_CFG_0	K2	DATA(44)	K3	DATA(45)	K4	DATA(47)	K5	VDDINT_05	K6	VDDINT_04	K7	GND_07	K8	GND_08	K9	GND_09	K10	GND_10	K11	GND_11	K12	GND_12	K13	GND_13	K14	GND_14	K15	VDDINT_15	K16	VDDINT_16	K17	BREQ_n	K18	BREQ_n	K19	BREQ_n	K20	BREQ_n
L1	CLKIN	L2	CLK_CFG_1	L3	AGND	L4	CLK_CFG_2	L5	VDDINT_15	L6	VDDINT_14	L7	GND_17	L8	GND_18	L9	GND_19	L10	GND_110	L11	GND_111	L12	GND_112	L13	GND_113	L14	GND_114	L15	VDDINT_115	L16	VDDINT_116	L17	BREQ_n	L18	BREQ_n	L19	BREQ_n	L20	BREQ_n
M1	AVDD	M2	CLK_CFG_3	M3	CLKOUT	M4	NC_B4	M5	VDDINT_05	M6	VDDINT_04	M7	GND_07	M8	GND_08	M9	GND_09	M10	GND_10	M11	GND_11	M12	GND_12	M13	GND_13	M14	GND_14	M15	VDDINT_115	M16	VDDINT_116	M17	BREQ_n	M18	BREQ_n	M19	PA_n	M20	LOGAT(7)
N1	AVDD	GND	DATA(48)	N4	DATA(51)	N5	VDDINT_05	N6	VDDINT_04	N7	GND_07	N8	GND_08	N9	GND_09	N10	GND_10	N11	GND_11	N12	GND_12	N13	GND_13	N14	GND_14	N15	VDDINT_115	N16	VDDINT_116	N17	L3DAT(5)	N18	L3DAT(6)	N19	L3DAT(4)	N20	L3CLK		
O1	NC_B1	N2	NC_B2	N3	DATA(16)	N6	DATA(19)	O8	VDDINT	O9	GND	O10	GND	O11	GND	O12	GND	O13	GND	O14	GND	O15	GND	O16	GND	O17	VDDINT	O18	VDDINT	O19	L1DAT(5)	O20	L1DAT(6)	O21	L3DAT(4)	O22	L3CLK		
P1	DATA(49)	P2	DATA(50)	P3	DATA(52)	P4	DATA(55)	P5	VDDINT_05	P6	VDDINT_04	P7	GND_07	P8	GND_08	P9	GND_09	P10	GND_10	P11	GND_11	P12	GND_12	P13	GND_13	P14	GND_14	P15	VDDINT_115	P16	VDDINT_116	P17	L3DAT(2)	P18	L3DAT(1)	P19	L3DAT(3)	P20	L3ACK
Q1	DATA(53)	Q2	DATA(54)	Q3	DATA(57)	Q4	DATA(60)	Q5	VDDINT_05	Q6	VDDINT_04	Q7	GND_07	Q8	GND_08	Q9	GND_09	Q10	GND_10	Q11	GND_11	Q12	GND_12	Q13	GND_13	Q14	GND_14	Q15	GND_15	Q16	VDDINT_116	Q17	VDDINT_117	Q18	L4DAT(5)	Q19	L4DAT(6)	Q20	L4DAT(7)
R1	DATA(21)	R2	DATA(22)	R3	DATA(25)	R4	DATA(28)	R5	VDDINT	R6	VDDINT	R7	GND	R8	GND	R9	GND	R10	GND	R11	GND	R12	GND	R13	GND	R14	GND	R15	GND	R16	VDDINT	R17	VDDINT	R18	L4DAT(5)	R19	L4DAT(6)	R20	L4DAT(7)
S1	DATA(56)	S2	DATA(58)	S3	DATA(59)	S4	DATA(63)	S5	VDDINT_05	S6	VDDINT_04	S7	VDDINT_07	S8	VDDINT_08	S9	VDDINT_09	S10	VDDINT_10	S11	VDDINT_11	S12	VDDINT_12	S13	VDDINT_13	S14	VDDINT_14	S15	VDDINT_15	S16	VDDINT_16	S17	L4DAT(3)	S18	L4ACK	S19	L4CLK	S20	L4DAT(4)
T1	DATA(61)	T2	DATA(62)	T3	ADDR(3)	T4	ADDR(2)	T5	VDDINT_05	T6	VDDINT_04	T7	VDDINT_07	T8	VDDINT_08	T9	VDDINT_09	T10	VDDINT_10	T11	VDDINT_11	T12	VDDINT_12	T13	VDDINT_13	T14	VDDINT_14	T15	VDDINT_15	T16	VDDINT_16	T17	L4DAT(3)	T18	L4ACK	T19	L4CLK	T20	L4DAT(4)
U1	ADDR(4)	U2	ADDR(6)	U3	ADDR(17)	U4	ADDR(10)	U5	ADDR(14)	U6	ADDR(18)	U7	ADDR(22)	U8	ADDR(25)	U9	ADDR(28)	U10	ADDR(31)	U11	ADDR(35)	U12	MS1_n	U13	MS2_n	U14	MS3_n	U15	MS4_n	U16	MS5_n	U17	MS6_n	U18	MS7_n	U19	MS8_n	U20	MS9_n
V1	ADDR(5)	V2	ADDR(8)	V3	ADDR(12)	V4	ADDR(15)	V5	ADDR(19)	V6	ADDR(23)	V7	ADDR(27)	V8	ADDR(31)	V9	ADDR(35)	V10	ADDR(39)	V11	ADDR(43)	V12	MS1_n	V13	MS2_n	V14	MS3_n	V15	MS4_n	V16	MS5_n	V17	MS6_n	V18	MS7_n	V19	MS8_n	V20	MS9_n
W1	ADDR(6)	W2	ADDR(9)	W3	ADDR(13)	W4	ADDR(16)	W5	ADDR(20)	W6	ADDR(24)	W7	ADDR(28)	W8	ADDR(32)	W9	ADDR(36)	W10	ADDR(40)	W11	ADDR(44)	W12	MS1_n	W13	MS2_n	W14	MS3_n	W15	MS4_n	W16	MS5_n	W17	MS6_n	W18	MS7_n	W19	MS8_n	W20	MS9_n
X1	ADDR(7)	X2	ADDR(11)	X3	ADDR(14)	X4	ADDR(17)	X5	ADDR(21)	X6	ADDR(25)	X7	ADDR(29)	X8	ADDR(33)	X9	ADDR(37)	X10	ADDR(41)	X11	ADDR(45)	X12	MS1_n	X13	MS2_n	X14	MS3_n	X15	MS4_n	X16	MS5_n	X17	MS6_n	X18	MS7_n	X19	MS8_n	X20	MS9_n
Y1	ADDR(8)	Y2	ADDR(12)	Y3	ADDR(15)	Y4	ADDR(19)	Y5	ADDR(23)	Y6	ADDR(27)	Y7	ADDR(31)	Y8	ADDR(35)	Y9	ADDR(39)	Y10	ADDR(43)	Y11	ADDR(47)	Y12	MS1_n	Y13	MS2_n	Y14	MS3_n	Y15	MS4_n	Y16	MS5_n	Y17	MS6_n	Y18	MS7_n	Y19	MS8_n	Y20	MS9_n
Z1	ADDR(9)	Z2	ADDR(13)	Z3	ADDR(16)	Z4	ADDR(20)	Z5	ADDR(24)	Z6	ADDR(28)	Z7	ADDR(32)	Z8	ADDR(36)	Z9	ADDR(40)	Z10	ADDR(44)	Z11	ADDR(48)	Z12	MS1_n	Z13	MS2_n	Z14	MS3_n	Z15	MS4_n	Z16	MS5_n	Z17	MS6_n	Z18	MS7_n	Z19	MS8_n	Z20	MS9_n

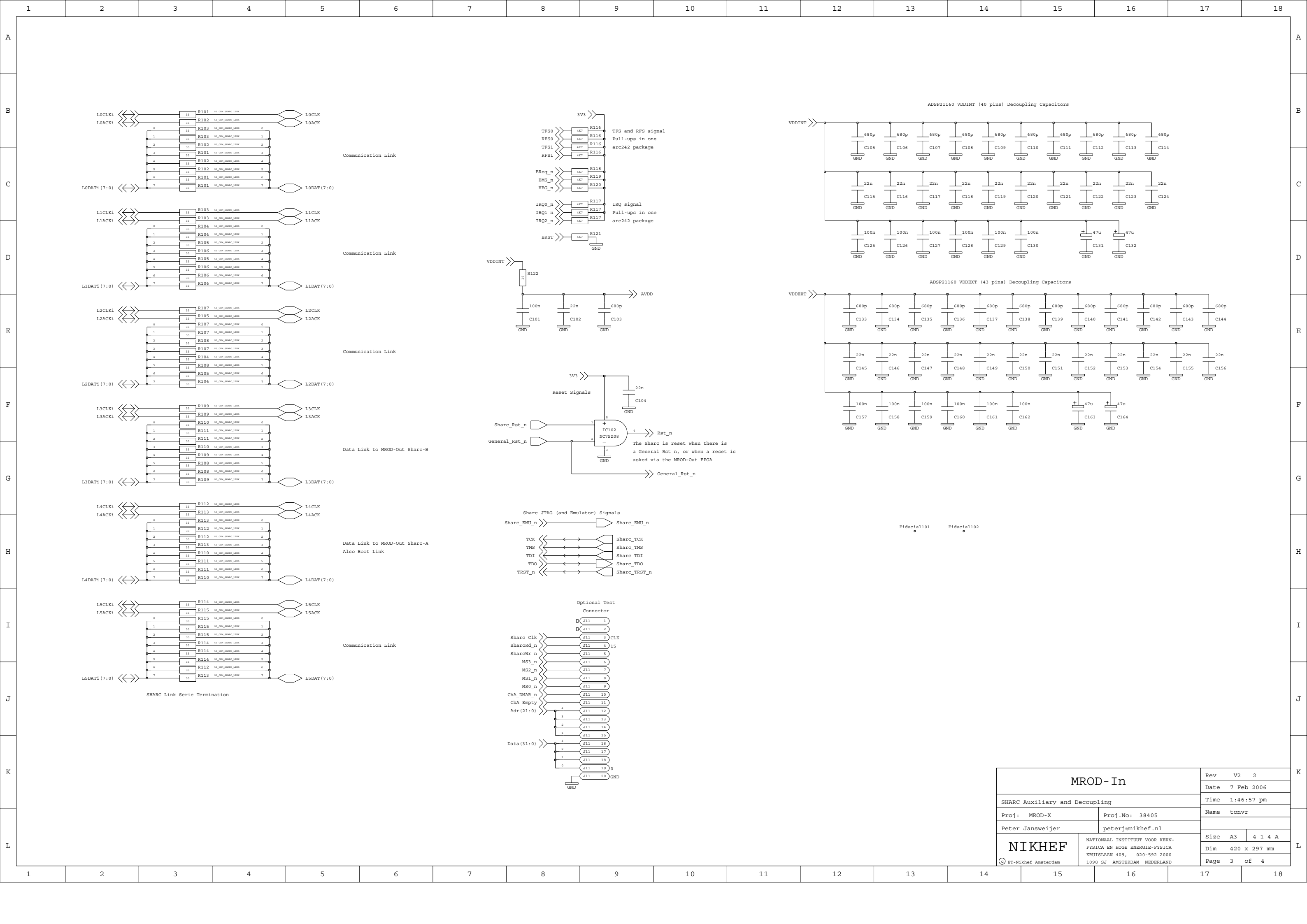
Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

ID = "000"

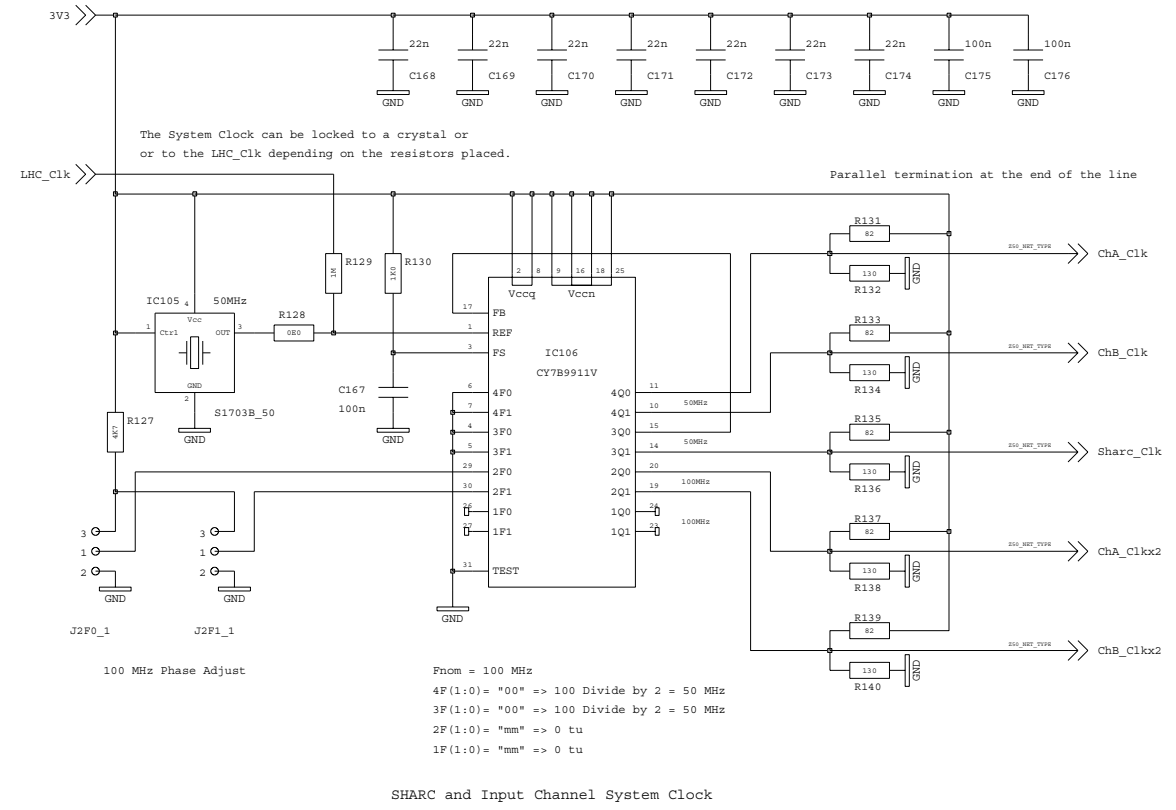
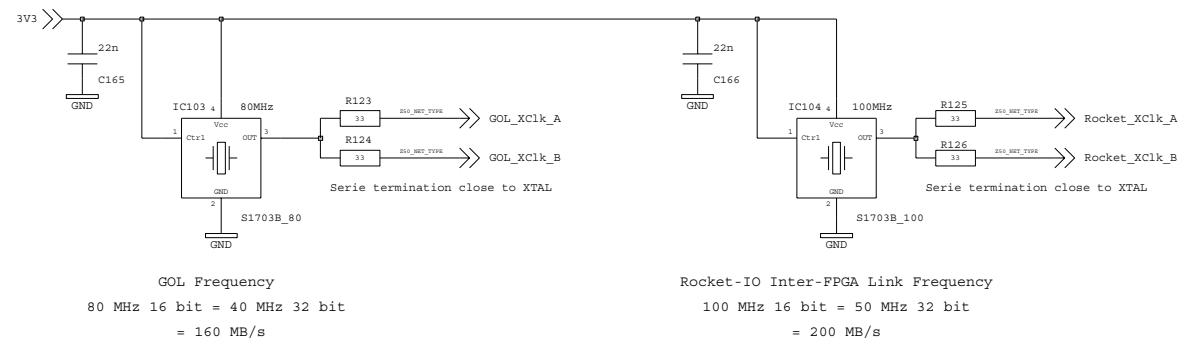
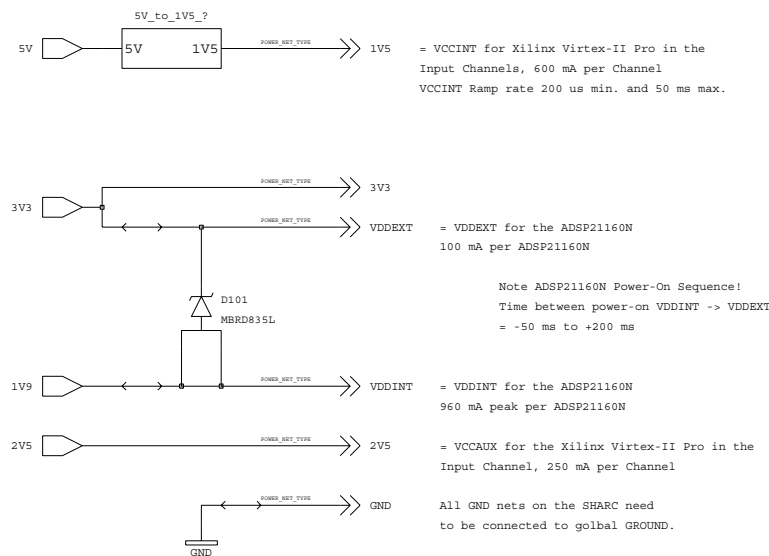
Booting Mode:
EBOOT = '0', LBOOT = '1', BMS_n = '1' (Input)
=> Link Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

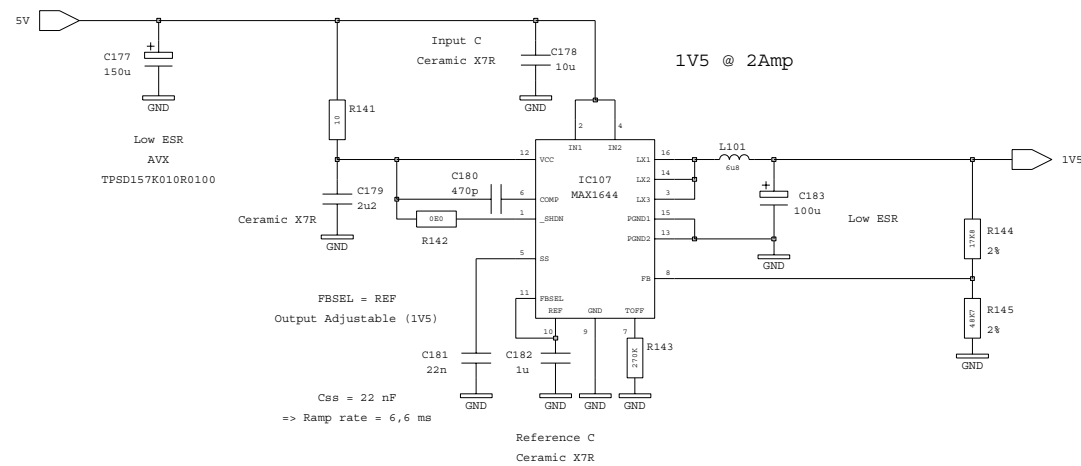
MROD- In		Rev	V2	2
		Date	7 Feb 2006	
SHARC		Time	1:46:33 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Dim	420 x 297 mm	
		Page	2 of 4	



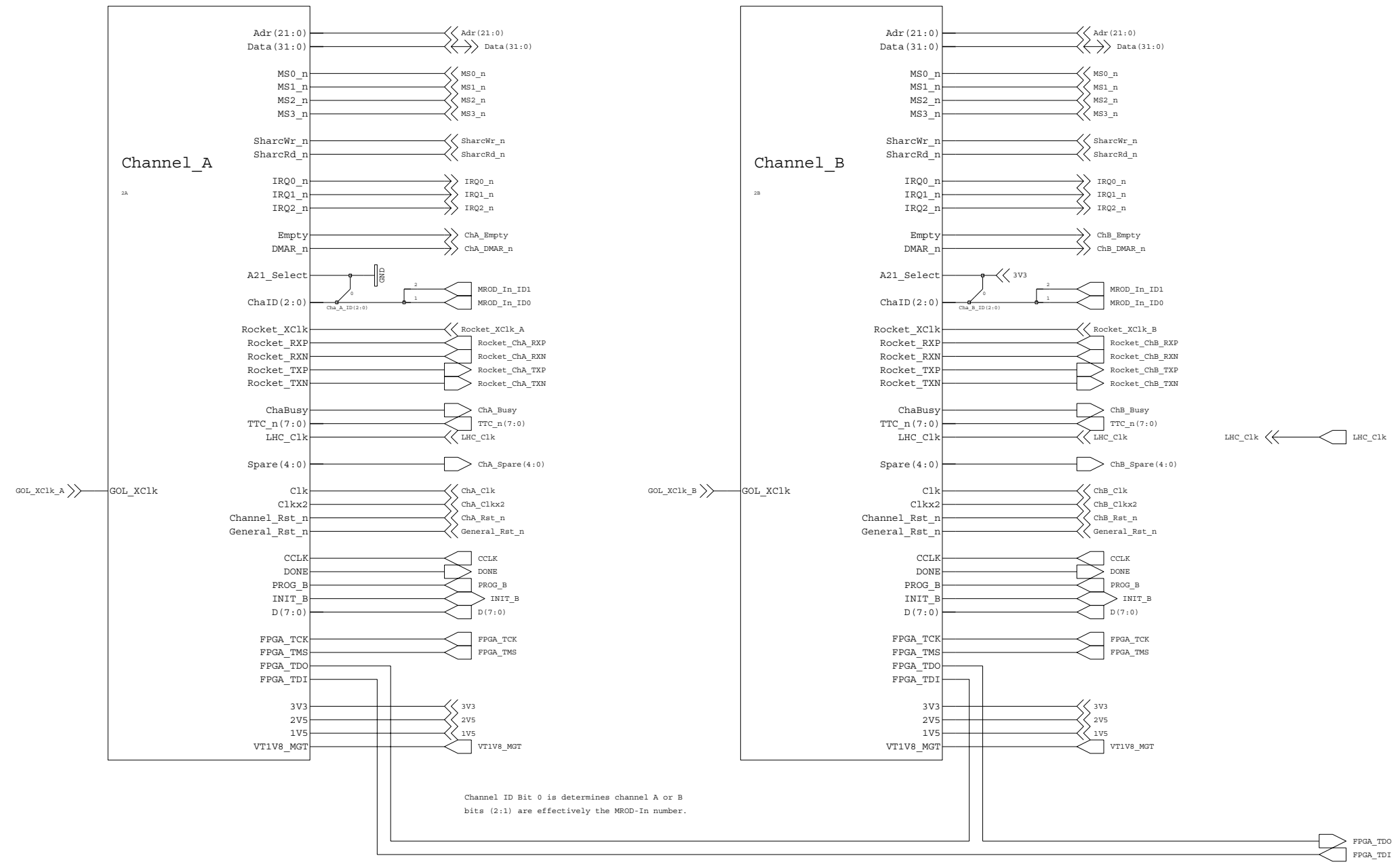
MROD- In		Rev V2 2
		Date 7 Feb 2006
SHARC Auxiliary and Decoupling		Time 1:46:57 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF © ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
		Dim 420 x 297 mm
		Page 3 of 4



MROD- In		Rev	V2	20
		Date	7 Feb 2006	
Power and Clocks		Time	1:47:20 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	4 of 4	



Power Supply		Rev	V2	2
		Date	7 Feb 2006	
5V -> 1V5 @ 2A		Time	1:38:24 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Dim	420 x 297 mm	
		Page	1 of 1	



Channel ID Bit 0 is determines channel A or B bits (2:1) are effectively the MROD-In number.

LHC_Clk ← LHC_Clk

MROD- In		Rev	V2	2
		Date	7 Feb 2006	
Input Channels		Time	1:45:51 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Dim	420 x 297 mm	
		Page	1 of 4	

IC201
ADSP21160N

A1	DATA(14)	A2	DATA(13)	A3	DATA(10)	A4	DATA(8)	A5	DATA(4)	A6	DATA(2)	A7	TDI	A8	TRST_n	A9	RESET_n	A10	PPBA	A11	IRQ0_n	A12	FLAG1	A13	TMEXF	A14	MC_A14	A15	MC_A15	A16	TPF1	A17	RFS1	A18	RCLK1	A19	DT0	A20	LOGAT(4)	
B1	DATA(22)	B2	DATA(16)	B3	DATA(15)	B4	DATA(9)	B5	DATA(6)	B6	DATA(3)	B7	DATA(0)	B8	TCK	B9	Sharc_BMU_n	B10	IRQ0_n	B11	FLAG3	B12	FLAG0	B13	MC_B13	B14	MC_B14	B15	DT1	B16	RCLK1	B17	RFS0	B18	TCLK0	B19	LOGAT(5)	B20	LOGAT(2)	
C1	DATA(24)	C2	DATA(18)	C3	DATA(17)	C4	DATA(11)	C5	DATA(7)	C6	DATA(5)	C7	DATA(1)	C8	TMS	C9	TDO	C10	IRQ1_n	C11	FLAG2	C12	MC_C12	C13	MC_C13	C14	TCLK1	C15	DT1	C16	DT0	C17	LOGAT(7)	C18	LOGAT(6)	C19	LOGAT(3)	C20	LOGAT(0)	
D1	DATA(28)	D2	DATA(25)	D3	DATA(20)	D4	DATA(19)	D5	DATA(12)	D6	VDDINT_06	D7	VDDINT_07	D8	VDDINT_08	D9	VDDINT_09	D10	VDDINT_10	D11	VDDINT_11	D12	VDDINT_12	D13	VDDINT_13	D14	VDDINT_14	D15	TPF0	D16	L1DAT(7)	D17	LOCLK	D18	LOGAT(3)	D19	LOGAT(1)	D20	L1CLK	
E1	DATA(30)	E2	DATA(29)	E3	DATA(23)	E4	DATA(21)	E5	VDDINT_05	E6	VDDINT_04	E7	VDDINT_03	E8	VDDINT_02	E9	VDDINT_01	E10	VDDINT_00	E11	GND	E12	VDDINT_15	E13	VDDINT_16	E14	VDDINT_17	E15	VDDINT_18	E16	VDDINT_19	E17	L1DAT(6)	E18	L1DAT(5)	E19	L1ACK	E20	L1DAT(1)	
F1	DATA(34)	F2	DATA(33)	F3	DATA(27)	F4	DATA(26)	F5	VDDINT_05	F6	VDDINT_04	F7	GND_07	F8	GND_08	F9	GND_09	F10	GND_10	F11	GND_11	F12	GND_12	F13	GND_13	F14	GND_14	F15	VDDINT_15	F16	VDDINT_16	F17	L1DAT(4)	F18	L1DAT(3)	F19	L1DAT(0)	F20	L2DAT(7)	
G1	DATA(38)	G2	DATA(35)	G3	DATA(32)	G4	DATA(31)	G5	VDDINT_05	G6	VDDINT_04	G7	GND_07	G8	GND_08	G9	GND_09	G10	GND_10	G11	GND_11	G12	GND_12	G13	GND_13	G14	GND_14	G15	VDDINT_15	G16	VDDINT_16	G17	L1DAT(2)	G18	L2DAT(6)	G19	L2DAT(4)	G20	L2CLK	
H1	DATA(40)	H2	DATA(39)	H3	DATA(37)	H4	DATA(34)	H5	VDDINT_05	H6	VDDINT_04	H7	GND_07	H8	GND_08	H9	GND_09	H10	GND_10	H11	GND_11	H12	GND_12	H13	GND_13	H14	GND_14	H15	VDDINT_15	H16	VDDINT_16	H17	L1DAT(2)	H18	L2DAT(6)	H19	L2DAT(4)	H20	L2CLK	
I1	DATA(44)	I2	DATA(43)	I3	DATA(42)	I4	DATA(41)	I5	VDDINT_05	I6	VDDINT_04	I7	GND_07	I8	GND_08	I9	GND_09	I10	GND_10	I11	GND_11	I12	GND_12	I13	GND_13	I14	GND_14	I15	VDDINT_15	I16	VDDINT_16	I17	L1DAT(2)	I18	L2DAT(2)	I19	HBG_n	I20	VDDINT	
J1	DATA(48)	J2	DATA(47)	J3	DATA(46)	J4	DATA(45)	J5	VDDINT_05	J6	VDDINT_04	J7	GND_07	J8	GND_08	J9	GND_09	J10	GND_10	J11	GND_11	J12	GND_12	J13	GND_13	J14	GND_14	J15	VDDINT_15	J16	VDDINT_16	J17	L1DAT(2)	J18	L2DAT(2)	J19	HBG_n	J20	VDDINT	
K1	CLK_CFG_0	K2	DATA(44)	K3	DATA(45)	K4	DATA(47)	K5	VDDINT_05	K6	VDDINT_04	K7	GND_07	K8	GND_08	K9	GND_09	K10	GND_10	K11	GND_11	K12	GND_12	K13	GND_13	K14	GND_14	K15	VDDINT_15	K16	VDDINT_16	K17	BREQ_n	K18	BREQ_n	K19	BREQ_n	K20	BREQ_n	
L1	CLKIN	L2	CLK_CFG_1	L3	AGND	L4	CLK_CFG_2	L5	VDDINT_15	L6	VDDINT_14	L7	GND_17	L8	GND_18	L9	GND_19	L10	GND_110	L11	GND_111	L12	GND_112	L13	GND_113	L14	GND_114	L15	VDDINT_115	L16	VDDINT_116	L17	BREQ_n	L18	BREQ_n	L19	ACK	L20	RDY	
M1	AVDD	M2	CLK_CFG_3	M3	CLKOUT	M4	MC_B4	M5	VDDINT_05	M6	VDDINT_04	M7	GND_07	M8	GND_08	M9	GND_09	M10	GND_10	M11	GND_11	M12	GND_12	M13	GND_13	M14	GND_14	M15	VDDINT_115	M16	VDDINT_116	M17	BREQ_n	M18	BREQ_n	M19	PA_n	M20	L3DAT(7)	
N1	AVDD	GND	0	0	0	0	0	VDDINT	VDDINT	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDINT	VDDINT	0	0	VDDINT	0	VDDINT	0	0	0	0	L3DAT(7)		
O1	MC_B1	MC_B2	MC_B3	DATA(48)	M4	DATA(51)	M5	VDDINT_05	M6	VDDINT_04	M7	GND_07	M8	GND_08	M9	GND_09	M10	GND_10	M11	GND_11	M12	GND_12	M13	GND_13	M14	GND_14	M15	VDDINT_115	M16	VDDINT_116	M17	L3DAT(5)	M18	L3DAT(6)	M19	L3DAT(4)	M20	L3CLK		
P1	DATA(49)	P2	DATA(50)	P3	DATA(52)	P4	DATA(55)	P5	VDDINT_05	P6	VDDINT_04	P7	GND_07	P8	GND_08	P9	GND_09	P10	GND_10	P11	GND_11	P12	GND_12	P13	GND_13	P14	GND_14	P15	VDDINT_115	P16	VDDINT_116	P17	L3DAT(2)	P18	L3DAT(1)	P19	L3DAT(3)	P20	L3ACK	
Q1	DATA(53)	Q2	DATA(54)	Q3	DATA(57)	Q4	DATA(60)	Q5	VDDINT_05	Q6	VDDINT_04	Q7	GND_07	Q8	GND_08	Q9	GND_09	Q10	GND_10	Q11	GND_11	Q12	GND_12	Q13	GND_13	Q14	GND_14	Q15	GND_115	Q16	VDDINT_116	Q17	VDDINT_117	Q18	L4DAT(5)	Q19	L4DAT(6)	Q20	L4DAT(0)	
R1	DATA(21)	DATA(22)	DATA(25)	DATA(28)	DATA(28)	DATA(28)	DATA(28)	VDDINT	VDDINT	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDINT	VDDINT	VDDINT	VDDINT	VDDINT	VDDINT	VDDINT	VDDINT	VDDINT	VDDINT	VDDINT	VDDINT
S1	DATA(56)	T2	DATA(58)	T3	DATA(59)	T4	DATA(63)	T5	VDDINT_05	T6	VDDINT_04	T7	VDDINT_07	T8	VDDINT_08	T9	VDDINT_09	T10	VDDINT_10	T11	VDDINT_11	T12	VDDINT_12	T13	VDDINT_13	T14	VDDINT_14	T15	VDDINT_15	T16	VDDINT_16	T17	L4DAT(3)	T18	L4ACK	T19	L4CLK	T20	L4DAT(4)	
U1	DATA(61)	U2	DATA(62)	U3	ADDR(3)	U4	ADDR(2)	U5	VDDINT_05	U6	VDDINT_04	U7	VDDINT_07	U8	VDDINT_08	U9	VDDINT_09	U10	VDDINT_10	U11	VDDINT_11	U12	VDDINT_12	U13	VDDINT_13	U14	VDDINT_14	U15	VDDINT_15	U16	VDDINT_16	U17	L4DAT(7)	U18	L4DAT(0)	U19	L4DAT(1)	U20	L4DAT(2)	
V1	ADDR(4)	Y2	ADDR(6)	V3	ADDR(17)	V4	ADDR(10)	V5	ADDR(14)	V6	ADDR(18)	V7	ADDR(22)	V8	ADDR(25)	V9	ADDR(28)	V10	100	V11	ADDR(1)	V12	MS1_n	V13	CS_n	V14	RD_n	V15	EMAR2_n	V16	LSACK	V17	LSACK	V18	LSACK	V19	LSACK	V20	LSACK	
W1	ADDR(5)	W2	ADDR(8)	W3	ADDR(12)	W4	ADDR(15)	W5	ADDR(17)	W6	ADDR(20)	W7	ADDR(23)	W8	ADDR(26)	W9	ADDR(29)	W10	101	W11	ADDR(0)	W12	BMS_n	W13	MS2_n	W14	CTF_n	W15	SharcR_n	W16	DMAG2_n	W17	LBOUT	W18	LSACK	W19	LSACK	W20	LSACK	
X1	ADDR(6)	X2	ADDR(11)	X3	ADDR(13)	X4	ADDR(14)	X5	ADDR(19)	X6	ADDR(21)	X7	ADDR(24)	X8	ADDR(27)	X9	ADDR(30)	X10	0	X11	ADDR(0)	X12	BMS_n	X13	MS2_n	X14	SharcR_n	X15	DMAG1_n	X16	DMAG1_n	X17	DMAG1_n	X18	DMAG1_n	X19	DMAG1_n	X20	DMAG1_n	
Y1	ADDR(8)	Y2	ADDR(11)	Y3	ADDR(13)	Y4	ADDR(14)	Y5	ADDR(19)	Y6	ADDR(21)	Y7	ADDR(24)	Y8	ADDR(27)	Y9	ADDR(30)	Y10	0	Y11	102	Y12	BRST	Y13	MS0_n	Y14	MS3_n	Y15	SharcWr_n	Y16	0	Y17	0	Y18	0	Y19	0	Y20	0	
Z1	ADDR(8)	Adr(11)	Adr(13)	Adr(16)	Adr(19)	Adr(21)																																		

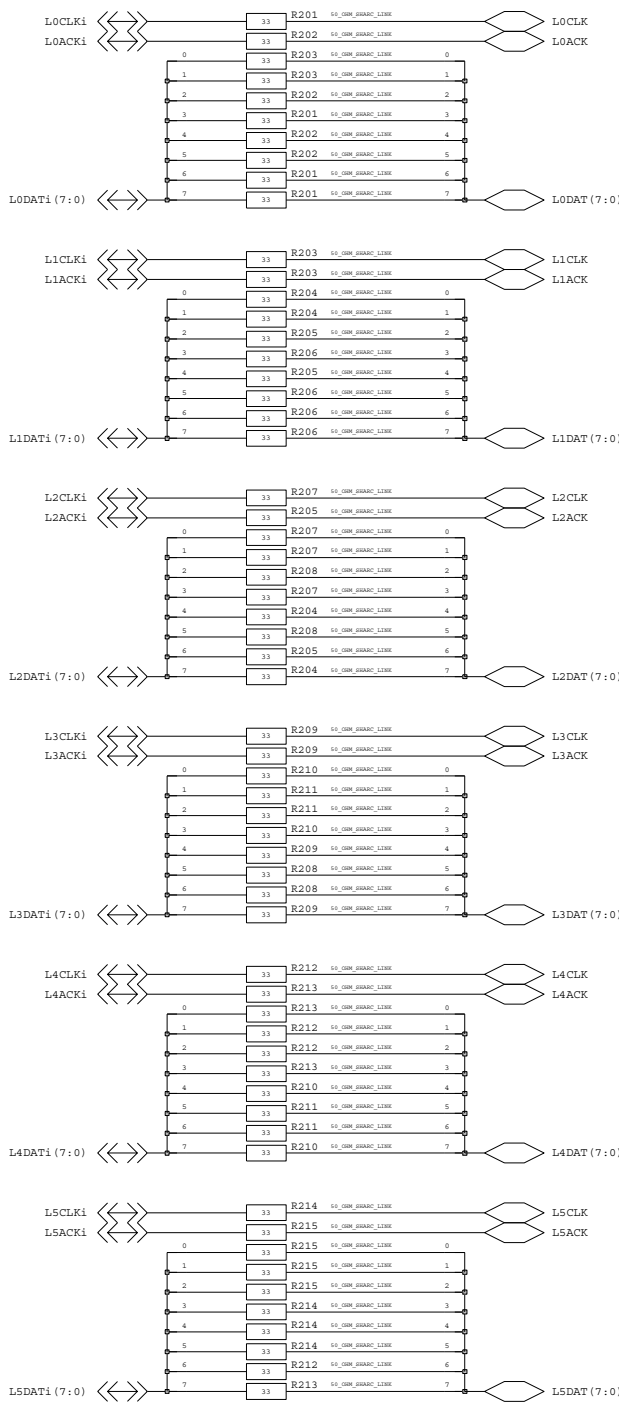
Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

ID = "000"

Booting Mode:
EBOOT = '0', LBOOT = '1', BMS_n = '1' (Input)
=> Link Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

MROD- In		Rev	V2	2
		Date	7 Feb 2006	
SHARC		Time	1:46:33 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Dim	420 x 297 mm	
		Page	2 of 4	



SHARC Link Serie Termination

Communication Link

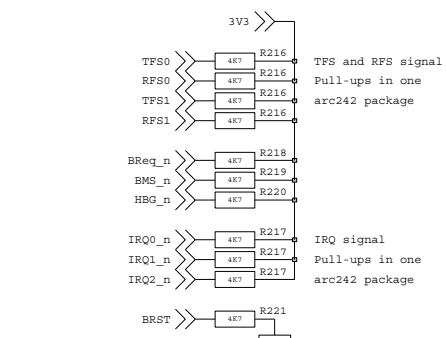
Communication Link

Communication Link

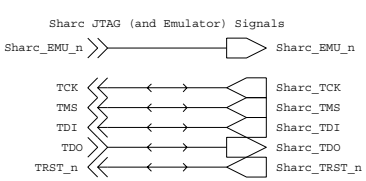
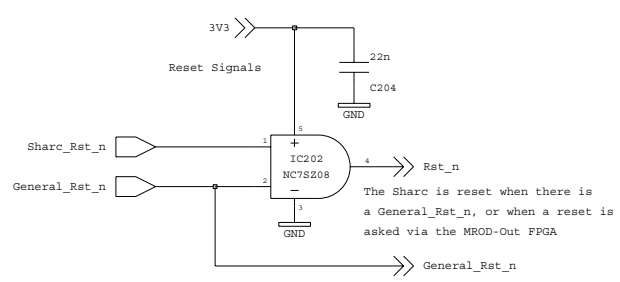
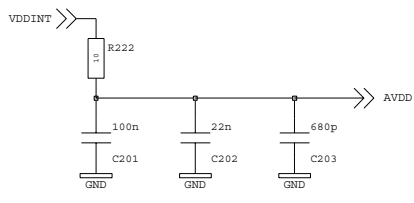
Data Link to MROD-Out Sharc-B

Data Link to MROD-Out Sharc-A Also Boot Link

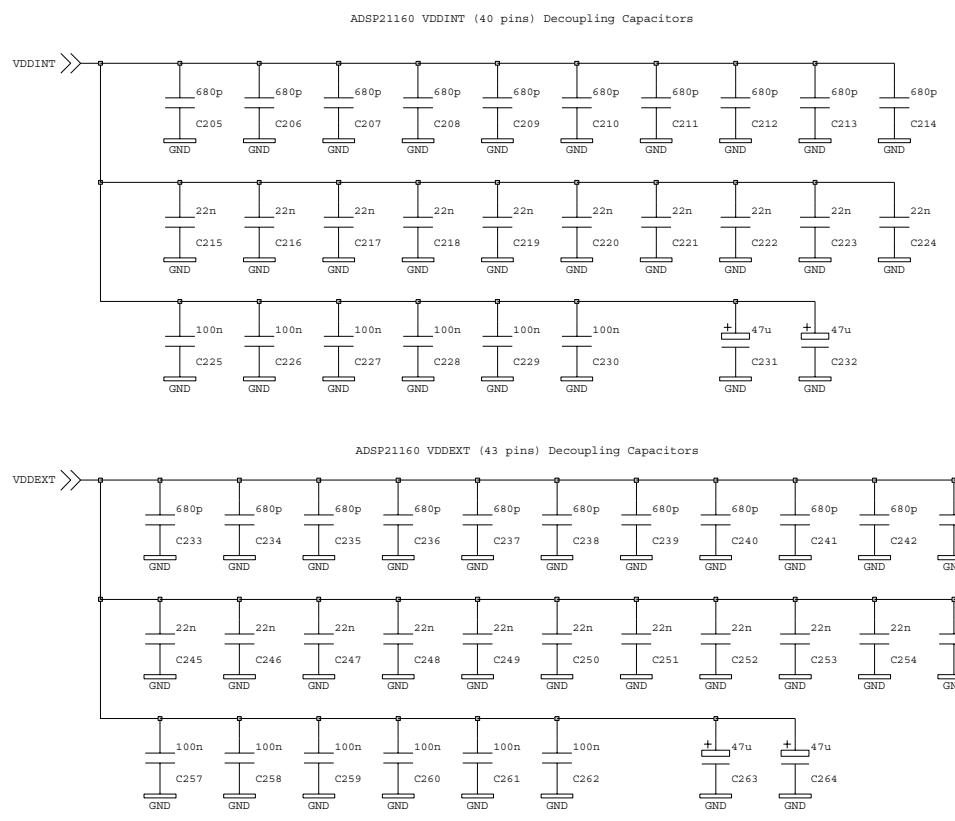
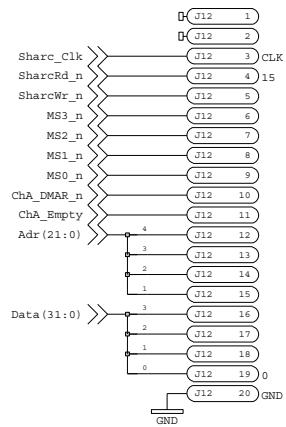
Communication Link



IRQ signal Pull-ups in one arc242 package

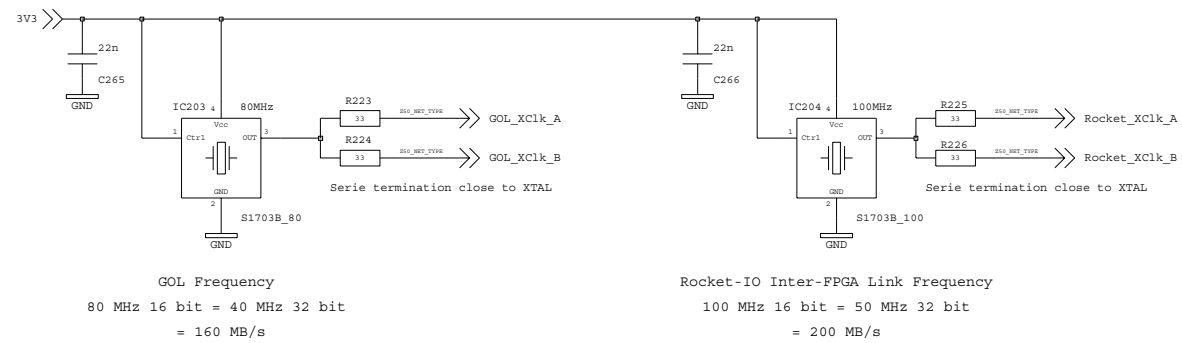
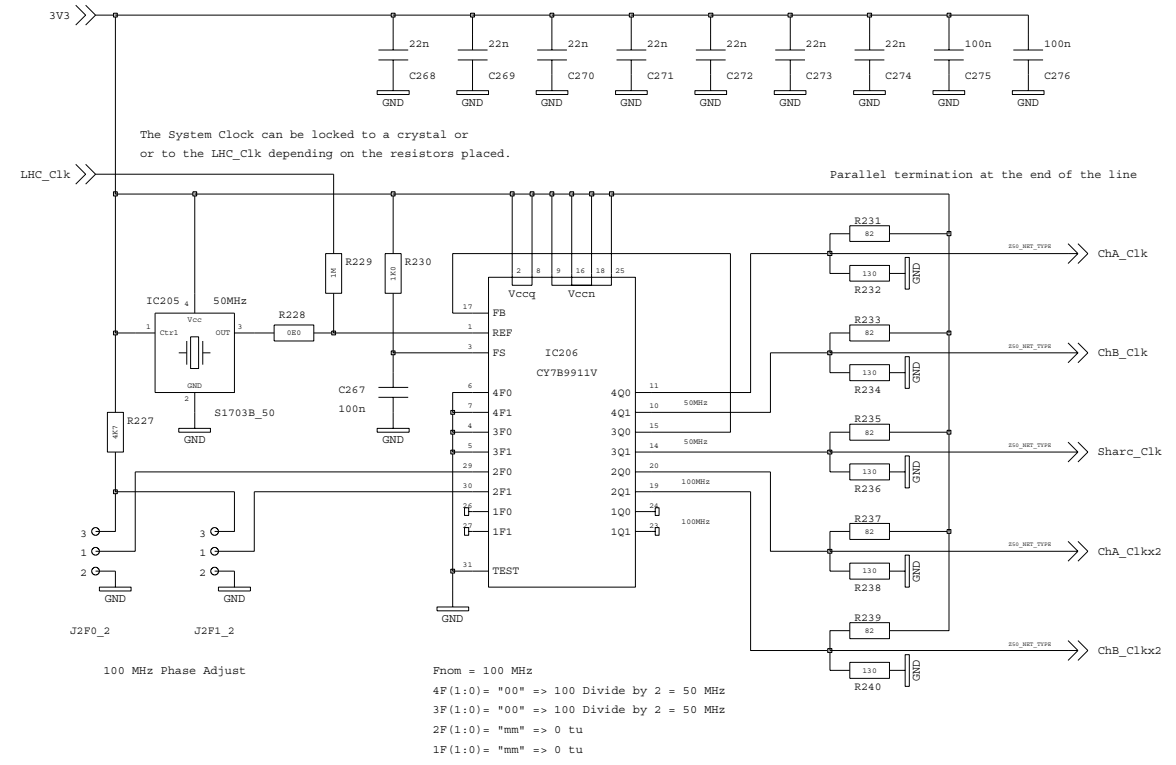
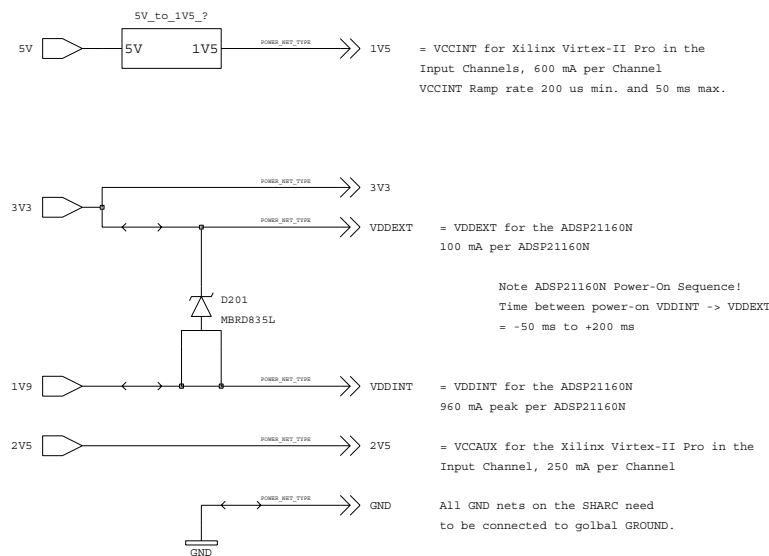


Optional Test Connector

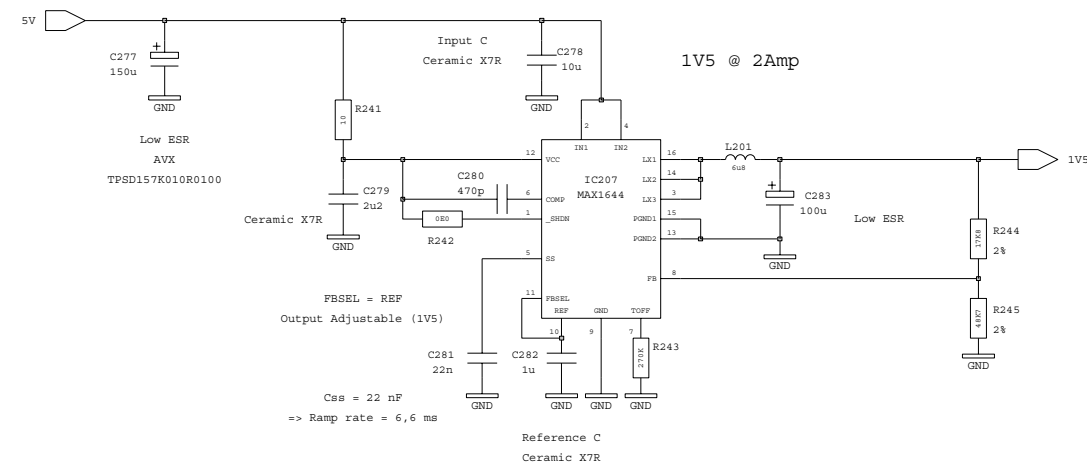


Fiducial1201 Fiducial1202

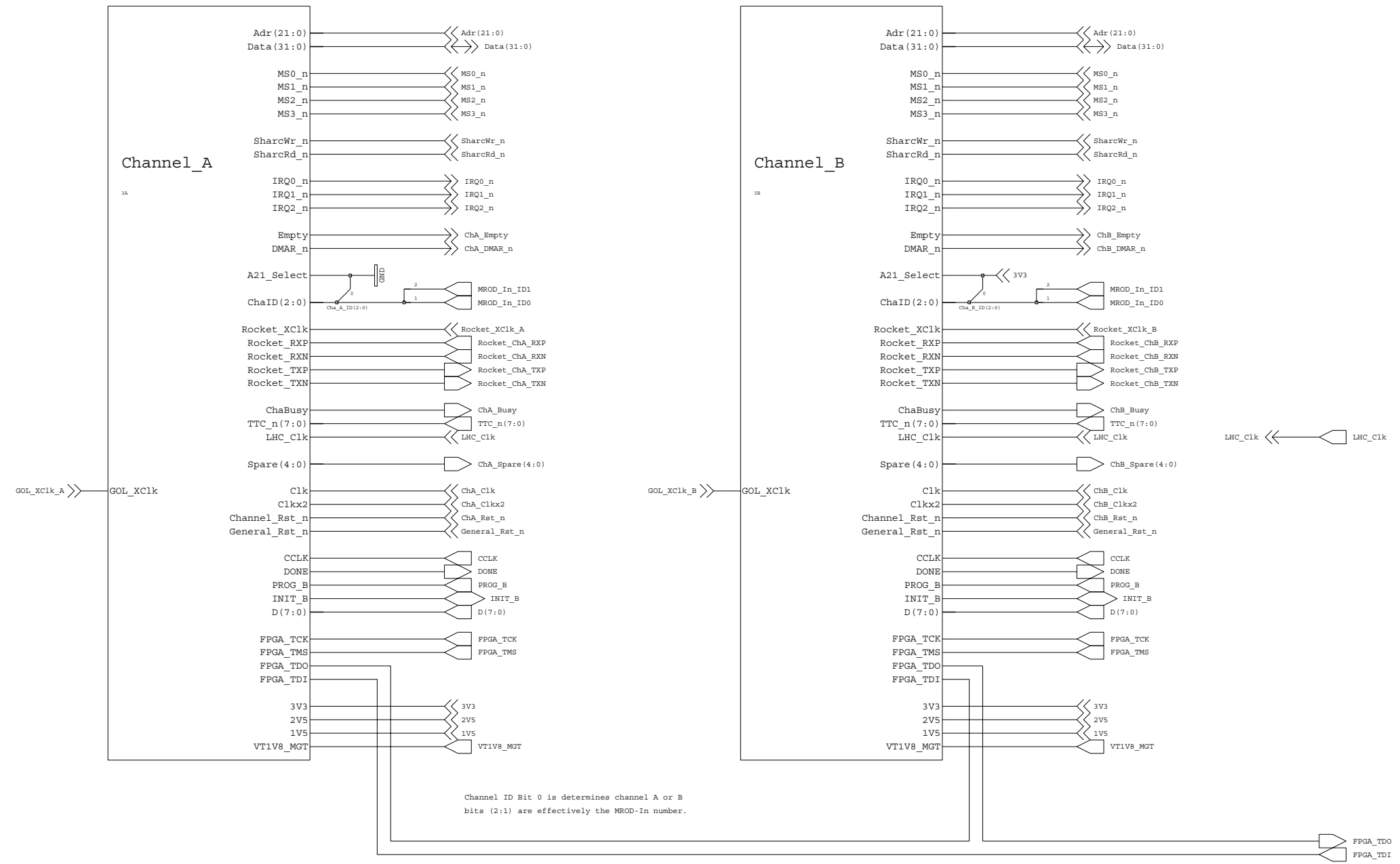
MROD- In		Rev V2 2
		Date 7 Feb 2006
SHARC Auxiliary and Decoupling		Time 1:46:57 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF © ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
		Dim 420 x 297 mm
		Page 3 of 4



MROD- In		Rev	V2	20	
		Date	7 Feb 2006		
Power and Clocks		Time	1:47:20 pm		
Proj:	MROD-X	Proj.No:	38405		
Peter Jansweijer		peterj@nikhef.nl			
NIKHEF NATIONAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size	A3	4 1 4 A	
		Dim	420 x 297 mm		
		Page	4 of 4		



Power Supply		Rev	V2	2
		Date	7 Feb 2006	
5V -> 1V5 @ 2A		Time	1:38:24 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>© ET-Nikhef Amsterdam</small>	<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>	Dim	420 x 297 mm	
		Page	1 of 1	



MROD- In		Rev	V2	2
		Date	7 Feb 2006	
Input Channels		Time	1:45:51 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		Name	tonvr	
		Size	A3	4 1 4 A
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Dim	420 x 297 mm	
		Page	1 of 4	

IC301
ADSP21160N

A1	DATA(14)	A2	DATA(13)	A3	DATA(10)	A4	DATA(8)	A5	DATA(4)	A6	DATA(2)	A7	TDI	A8	TRST_n	A9	RESET_n	A10	PPBA	A11	IRQ0_n	A12	FLAG1	A13	TMEXP	A14	NC_A14	A15	NC_A15	A16	TPP1	A17	RFS1	A18	RCLK1	A19	DT0	A20	LOGAT(4)
B1	DATA(22)	B2	DATA(16)	B3	DATA(15)	B4	DATA(9)	B5	DATA(6)	B6	DATA(3)	B7	DATA(0)	B8	TCK	B9	Sharc_BMU_n	B10	IRQ0_n	B11	ChB_Empty	B12	FLAG0	B13	NC_B13	B14	NC_B14	B15	DT1	B16	RCLK1	B17	RFS0	B18	TCCLK	B19	LOGAT(5)	B20	LOGAT(2)
C1	DATA(24)	C2	DATA(18)	C3	DATA(17)	C4	DATA(11)	C5	DATA(7)	C6	DATA(5)	C7	DATA(1)	C8	TMS	C9	TDO	C10	IRQ1_n	C11	ChA_Empty	C12	NC_C12	C13	NC_C13	C14	TCCLK	C15	DT1	C16	DT0	C17	LOGAT(7)	C18	LOGAT(6)	C19	LOGAT(3)	C20	LOGAT(0)
D1	DATA(28)	D2	DATA(25)	D3	DATA(20)	D4	DATA(19)	D5	DATA(12)	D6	VDDINT_06	D7	VDDINT_07	D8	VDDINT_08	D9	VDDINT_09	D10	VDDINT_10	D11	VDDINT_11	D12	VDDINT_12	D13	VDDINT_13	D14	VDDINT_14	D15	TPP0	D16	L1DAT(7)	D17	LOCLK	D18	LOGAT(3)	D19	LOGAT(1)	D20	L1CLK
E1	DATA(30)	E2	DATA(29)	E3	DATA(23)	E4	DATA(21)	E5	VDDINT_05	E6	VDDINT_04	E7	VDDINT_03	E8	VDDINT_02	E9	VDDINT_01	E10	VDDINT_00	E11	GND	E12	VDDINT_15	E13	VDDINT_16	E14	VDDINT_17	E15	VDDINT_18	E16	VDDINT_19	E17	L1DAT(6)	E18	L1DAT(5)	E19	L1ACK	E20	L1DAT(1)
F1	DATA(34)	F2	DATA(33)	F3	DATA(27)	F4	DATA(26)	F5	VDDINT_05	F6	VDDINT_04	F7	GND_07	F8	GND_08	F9	GND_09	F10	GND_10	F11	GND_11	F12	GND_12	F13	GND_13	F14	GND_14	F15	VDDINT_15	F16	VDDINT_16	F17	L1DAT(4)	F18	L1DAT(3)	F19	L1DAT(0)	F20	L2DAT(7)
G1	DATA(38)	G2	DATA(35)	G3	DATA(32)	G4	DATA(31)	G5	VDDINT_05	G6	VDDINT_04	G7	GND_07	G8	GND_08	G9	GND_09	G10	GND_10	G11	GND_11	G12	GND_12	G13	GND_13	G14	GND_14	G15	VDDINT_15	G16	VDDINT_16	G17	L1DAT(2)	G18	L2DAT(6)	G19	L2DAT(4)	G20	L2CLK
H1	DATA(40)	H2	DATA(39)	H3	DATA(37)	H4	DATA(34)	H5	VDDINT_05	H6	VDDINT_04	H7	GND_07	H8	GND_08	H9	GND_09	H10	GND_10	H11	GND_11	H12	GND_12	H13	GND_13	H14	GND_14	H15	VDDINT_15	H16	VDDINT_16	H17	L1DAT(2)	H18	L2DAT(6)	H19	L2DAT(4)	H20	L2CLK
I1	DATA(44)	I2	DATA(43)	I3	DATA(42)	I4	DATA(41)	I5	VDDINT_05	I6	VDDINT_04	I7	GND_07	I8	GND_08	I9	GND_09	I10	GND_10	I11	GND_11	I12	GND_12	I13	GND_13	I14	GND_14	I15	VDDINT_15	I16	VDDINT_16	I17	L1DAT(2)	I18	L2DAT(2)	I19	HBG_n	I20	VDDINT
J1	DATA(48)	J2	DATA(47)	J3	DATA(46)	J4	DATA(45)	J5	VDDINT_05	J6	VDDINT_04	J7	GND_07	J8	GND_08	J9	GND_09	J10	GND_10	J11	GND_11	J12	GND_12	J13	GND_13	J14	GND_14	J15	VDDINT_15	J16	VDDINT_16	J17	L1DAT(2)	J18	L2DAT(2)	J19	HBG_n	J20	VDDINT
K1	CLK_CFG_0	K2	DATA(44)	K3	DATA(45)	K4	DATA(47)	K5	VDDINT_05	K6	VDDINT_04	K7	GND_07	K8	GND_08	K9	GND_09	K10	GND_10	K11	GND_11	K12	GND_12	K13	GND_13	K14	GND_14	K15	VDDINT_15	K16	VDDINT_16	K17	BREQ_n	K18	BREQ_n	K19	BREQ_n	K20	BREQ_n
L1	CLKIN	L2	CLK_CFG_1	L3	AGND	L4	CLK_CFG_2	L5	VDDINT_15	L6	VDDINT_14	L7	GND_17	L8	GND_18	L9	GND_19	L10	GND_110	L11	GND_111	L12	GND_112	L13	GND_113	L14	GND_114	L15	VDDINT_115	L16	VDDINT_116	L17	BREQ_n	L18	BREQ_n	L19	BREQ_n	L20	BREQ_n
M1	AVDD	M2	CLK_CFG_3	M3	CLKOUT	M4	NC_B4	M5	VDDINT_05	M6	VDDINT_04	M7	GND_07	M8	GND_08	M9	GND_09	M10	GND_10	M11	GND_11	M12	GND_12	M13	GND_13	M14	GND_14	M15	VDDINT_115	M16	VDDINT_116	M17	BREQ_n	M18	BREQ_n	M19	PA_n	M20	LOGAT(7)
N1	AVDD	GND	DATA(48)	N4	DATA(51)	N5	VDDINT_05	N6	VDDINT_04	N7	GND_07	N8	GND_08	N9	GND_09	N10	GND_10	N11	GND_11	N12	GND_12	N13	GND_13	N14	GND_14	N15	VDDINT_115	N16	VDDINT_116	N17	L3DAT(5)	N18	L3DAT(6)	N19	L3DAT(4)	N20	L3CLK		
O1	NC_B1	N2	NC_B2	N3	DATA(16)	N6	DATA(19)	O8	VDDINT	O9	GND	O10	GND	O11	GND	O12	GND	O13	GND	O14	GND	O15	GND	O16	GND	O17	VDDINT	O18	VDDINT	O19	L1DAT(5)	O20	L1DAT(6)	O21	L3DAT(4)	O22	L3CLK		
P1	DATA(49)	P2	DATA(50)	P3	DATA(52)	P4	DATA(55)	P5	VDDINT_05	P6	VDDINT_04	P7	GND_07	P8	GND_08	P9	GND_09	P10	GND_10	P11	GND_11	P12	GND_12	P13	GND_13	P14	GND_14	P15	VDDINT_115	P16	VDDINT_116	P17	L3DAT(2)	P18	L3DAT(1)	P19	L3DAT(3)	P20	L3ACK
Q1	DATA(53)	Q2	DATA(54)	Q3	DATA(57)	Q4	DATA(60)	Q5	VDDINT_05	Q6	VDDINT_04	Q7	GND_07	Q8	GND_08	Q9	GND_09	Q10	GND_10	Q11	GND_11	Q12	GND_12	Q13	GND_13	Q14	GND_14	Q15	GND_15	Q16	VDDINT_116	Q17	VDDINT_117	Q18	L4DAT(5)	Q19	L4DAT(6)	Q20	L4DAT(7)
R1	DATA(21)	R2	DATA(22)	R3	DATA(25)	R4	DATA(28)	R5	VDDINT	R6	VDDINT	R7	GND	R8	GND	R9	GND	R10	GND	R11	GND	R12	GND	R13	GND	R14	GND	R15	GND	R16	VDDINT	R17	VDDINT	R18	L4DAT(5)	R19	L4DAT(6)	R20	L4DAT(7)
S1	DATA(56)	S2	DATA(58)	S3	DATA(59)	S4	DATA(63)	S5	VDDINT_05	S6	VDDINT_04	S7	VDDINT_07	S8	VDDINT_08	S9	VDDINT_09	S10	VDDINT_10	S11	VDDINT_11	S12	VDDINT_12	S13	VDDINT_13	S14	VDDINT_14	S15	VDDINT_15	S16	VDDINT_16	S17	L4DAT(3)	S18	L4ACK	S19	L4CLK	S20	L4DAT(4)
T1	DATA(61)	T2	DATA(62)	T3	ADDR(3)	T4	ADDR(2)	T5	VDDINT_05	T6	VDDINT_04	T7	VDDINT_07	T8	VDDINT_08	T9	VDDINT_09	T10	VDDINT_10	T11	VDDINT_11	T12	VDDINT_12	T13	VDDINT_13	T14	VDDINT_14	T15	VDDINT_15	T16	VDDINT_16	T17	L4DAT(3)	T18	L4ACK	T19	L4CLK	T20	L4DAT(4)
U1	ADDR(4)	U2	ADDR(6)	U3	ADDR(17)	U4	ADDR(10)	U5	VDDINT	U6	VDDINT	U7	VDDINT	U8	VDDINT	U9	VDDINT	U10	VDDINT	U11	VDDINT	U12	VDDINT	U13	VDDINT	U14	VDDINT	U15	VDDINT	U16	VDDINT	U17	L5DAT(7)	U18	L5DAT(2)	U19	L5ACK	U20	L5DAT(4)
V1	Adr(4)	V2	Adr(6)	V3	Adr(7)	V4	Adr(10)	V5	Adr(14)	V6	Adr(18)	V7	Adr(18)	V8	Adr(22)	V9	Adr(25)	V10	100	V11	ADDR(1)	V12	MS1_n	V13	CS_n	V14	RD_n	V15	EMAR2_n	V16	LSAT(0)	V17	LSAT(2)	V18	LSACK	V19	LSAT(4)	V20	LSAT(6)
W1	ADDR(5)	W2	ADDR(8)	W3	ADDR(12)	W4	ADDR(15)	W5	ADDR(17)	W6	ADDR(20)	W7	ADDR(23)	W8	ADDR(26)	W9	ADDR(29)	W10	101	W11	ADDR(0)	W12	BMS_n	W13	MS2_n	W14	CTF_n	W15	RD_n	W16	DMAG2_n	W17	LBOUT	W18	LSAT(1)	W19	LSAT(3)	W20	LSAT(5)
X1	Adr(5)	X2	Adr(9)	X3	Adr(12)	X4	Adr(15)	X5	Adr(17)	X6	Adr(20)	X7	Adr(23)	X8	Adr(26)	X9	Adr(29)	X10	GND	X11	Adr(0)	X12	BMS_n	X13	MS2_n	X14	SharcR_n	X15	VDDINT	X16	VDDINT	X17	LSAT(1)	X18	LSAT(3)	X19	LSAT(5)	X20	LSCLK
Y1	ADDR(8)	Y2	ADDR(11)	Y3	ADDR(13)	Y4	ADDR(14)	Y5	ADDR(19)	Y6	ADDR(21)	Y7	ADDR(24)	Y8	ADDR(27)	Y9	ADDR(30)	Y10	ADDR(31)	Y11	102	Y12	BRST	Y13	MS0_n	Y14	MS1_n	Y15	MS2_n	Y16	MS3_n	Y17	MS4_n	Y18	MS5_n	Y19	MS6_n	Y20	MS7_n

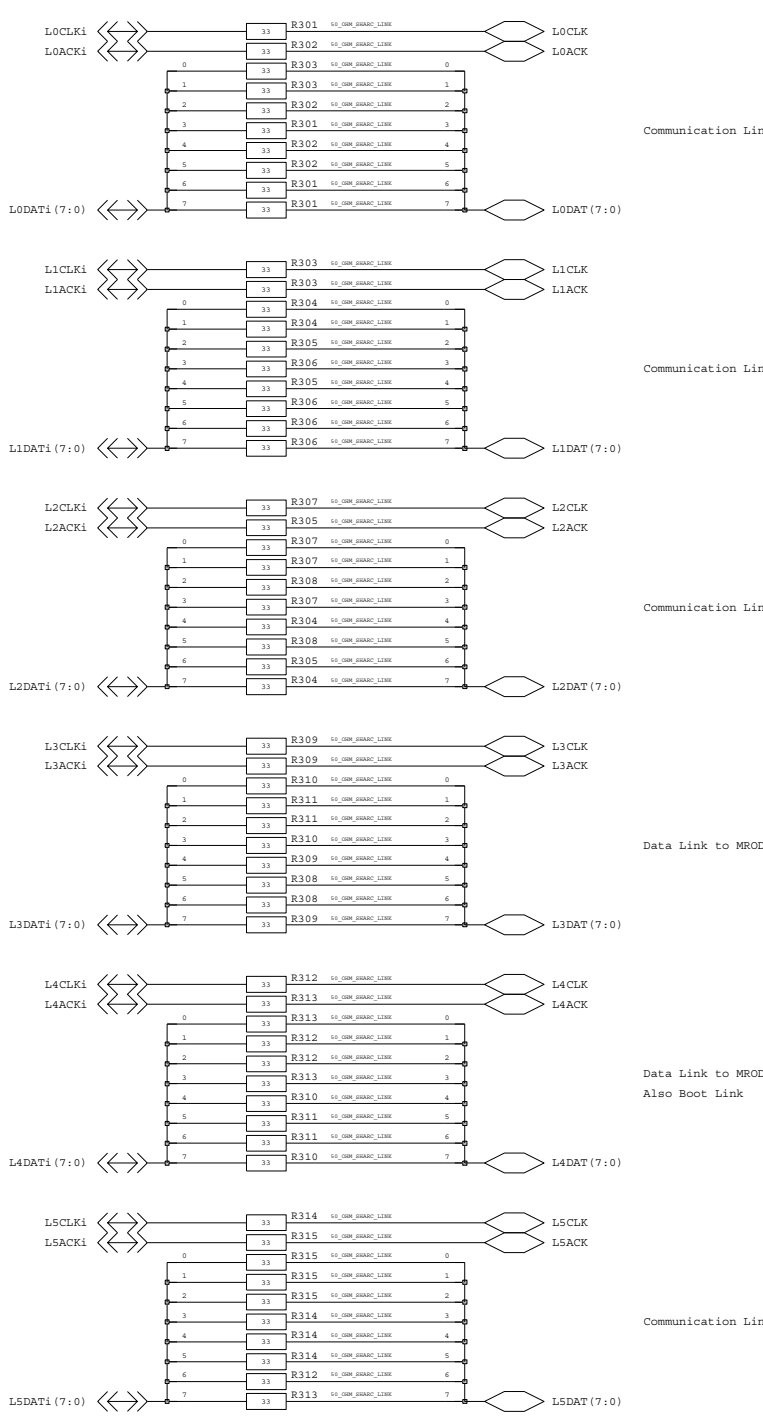
Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

ID = "000"

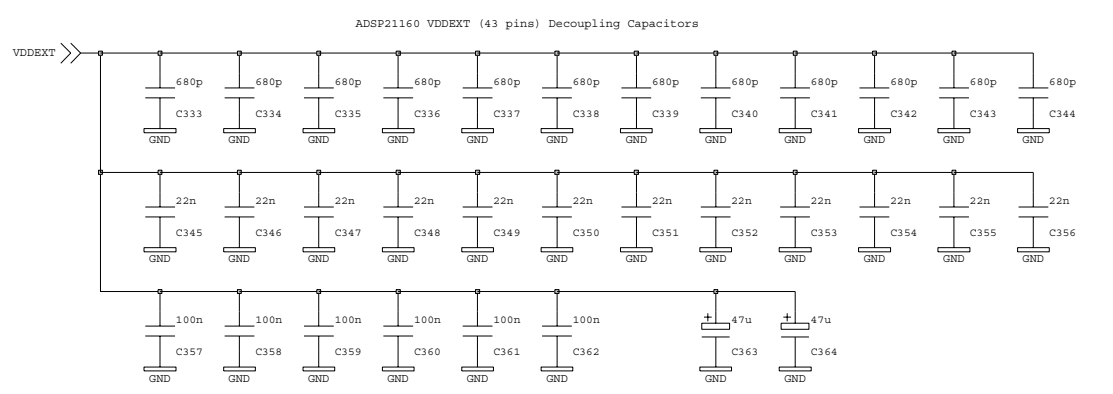
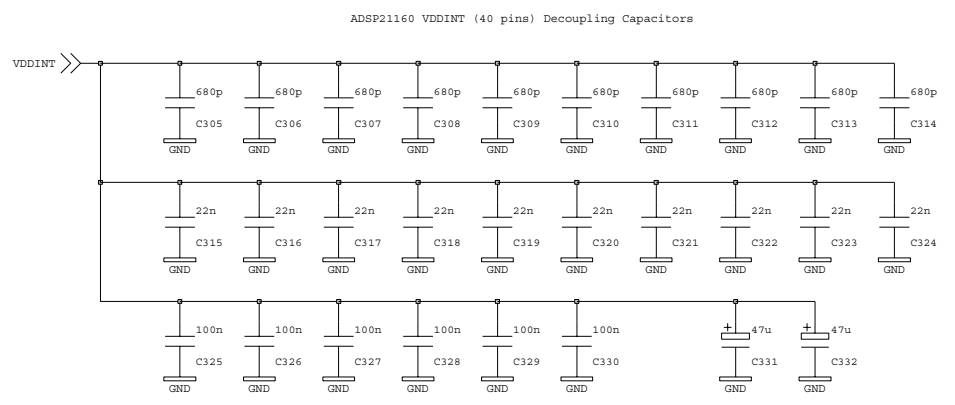
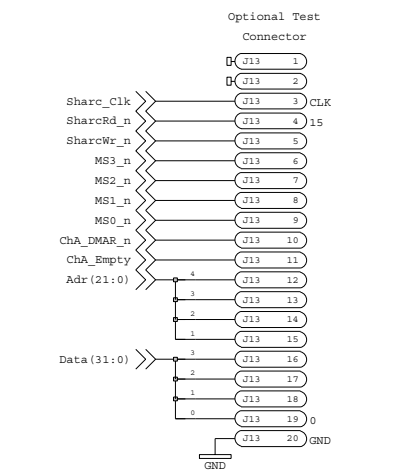
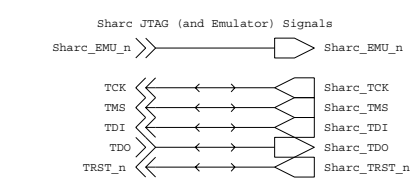
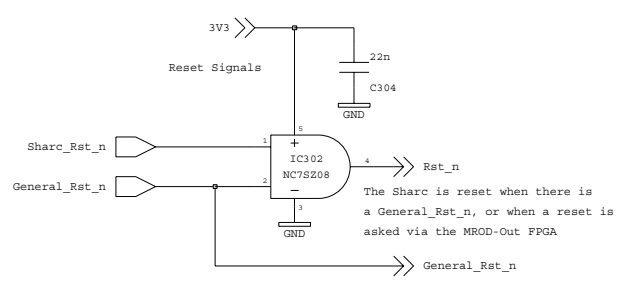
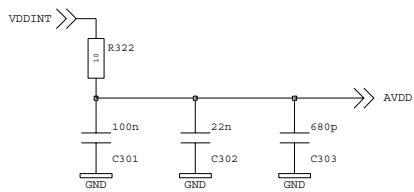
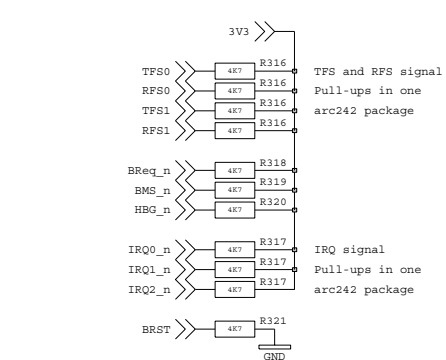
Booting Mode:
EBOOT = '0', LBOOT = '1', BMS_n = '1' (Input)
=> Link Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

MROD- In		Rev	V2	2
		Date	7 Feb 2006	
SHARC		Time	1:46:33 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>© Nikhef Amsterdam</small>		<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		
		Dim	420 x 297 mm	
		Page	2 of 4	

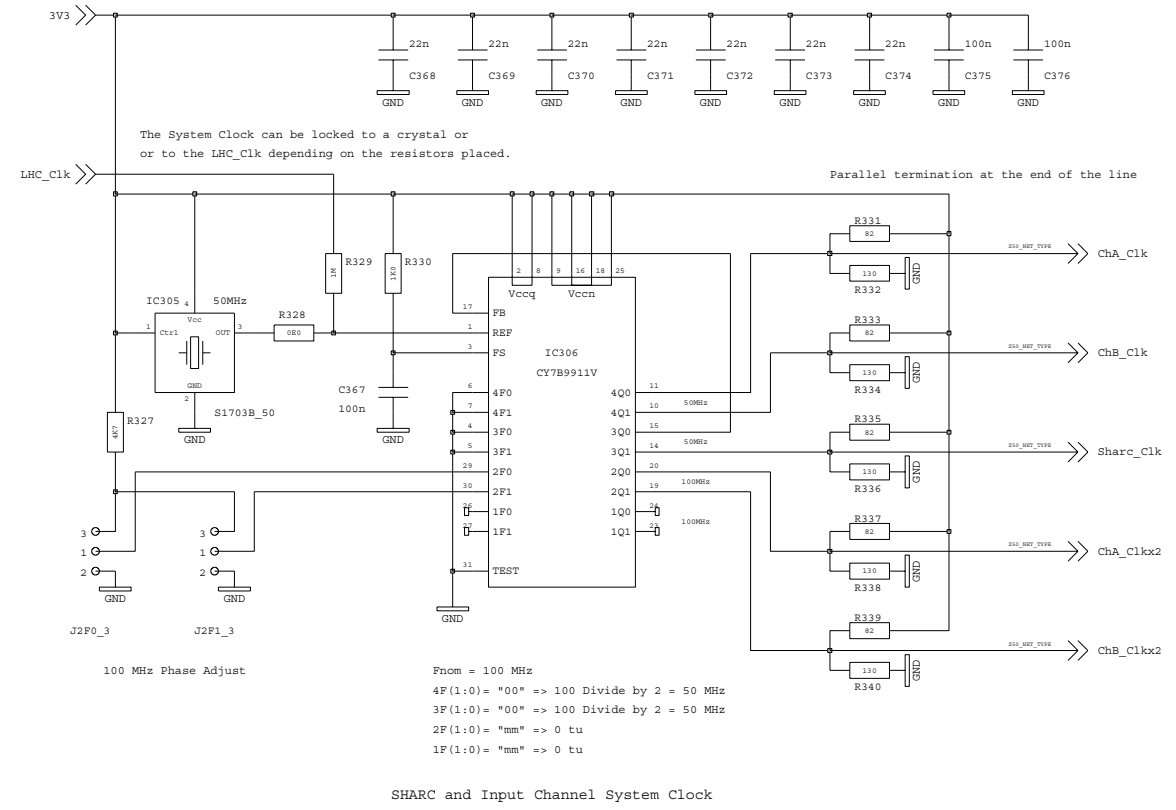
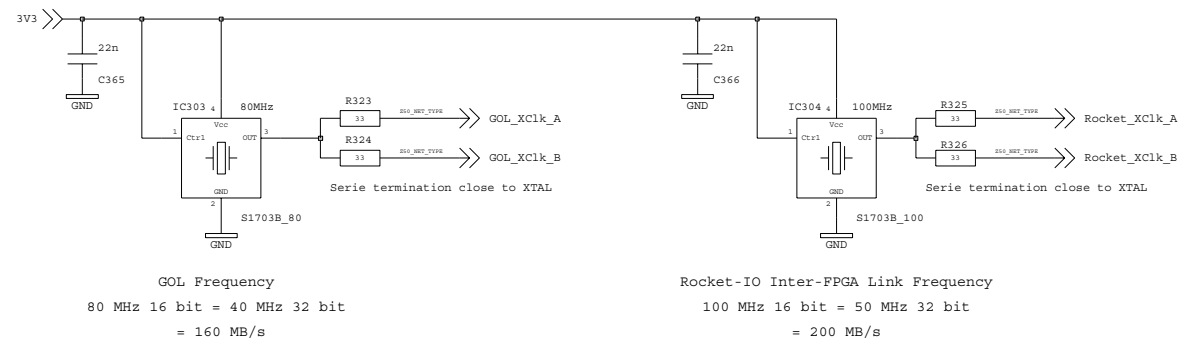
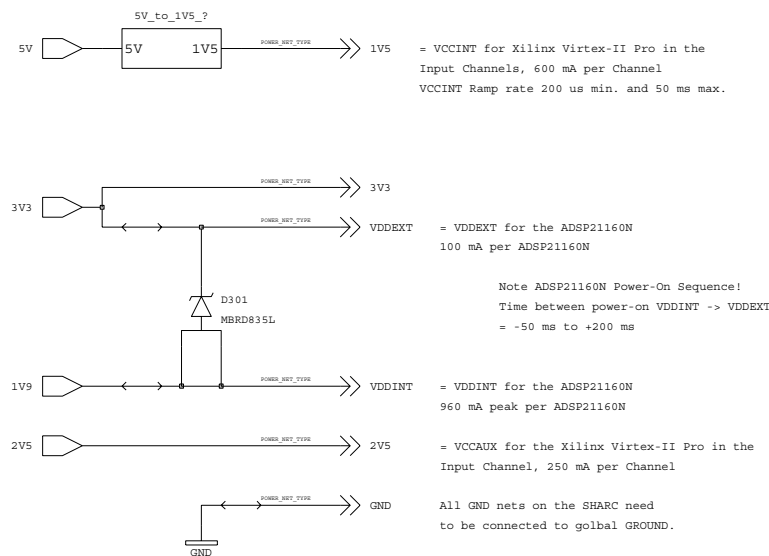


SHARC Link Serie Termination

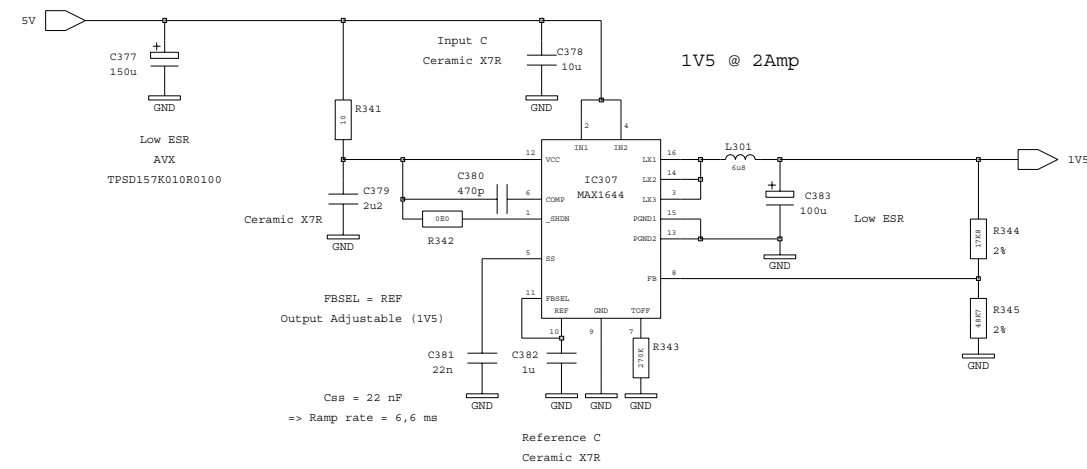


Fiducial1301 Fiducial1302

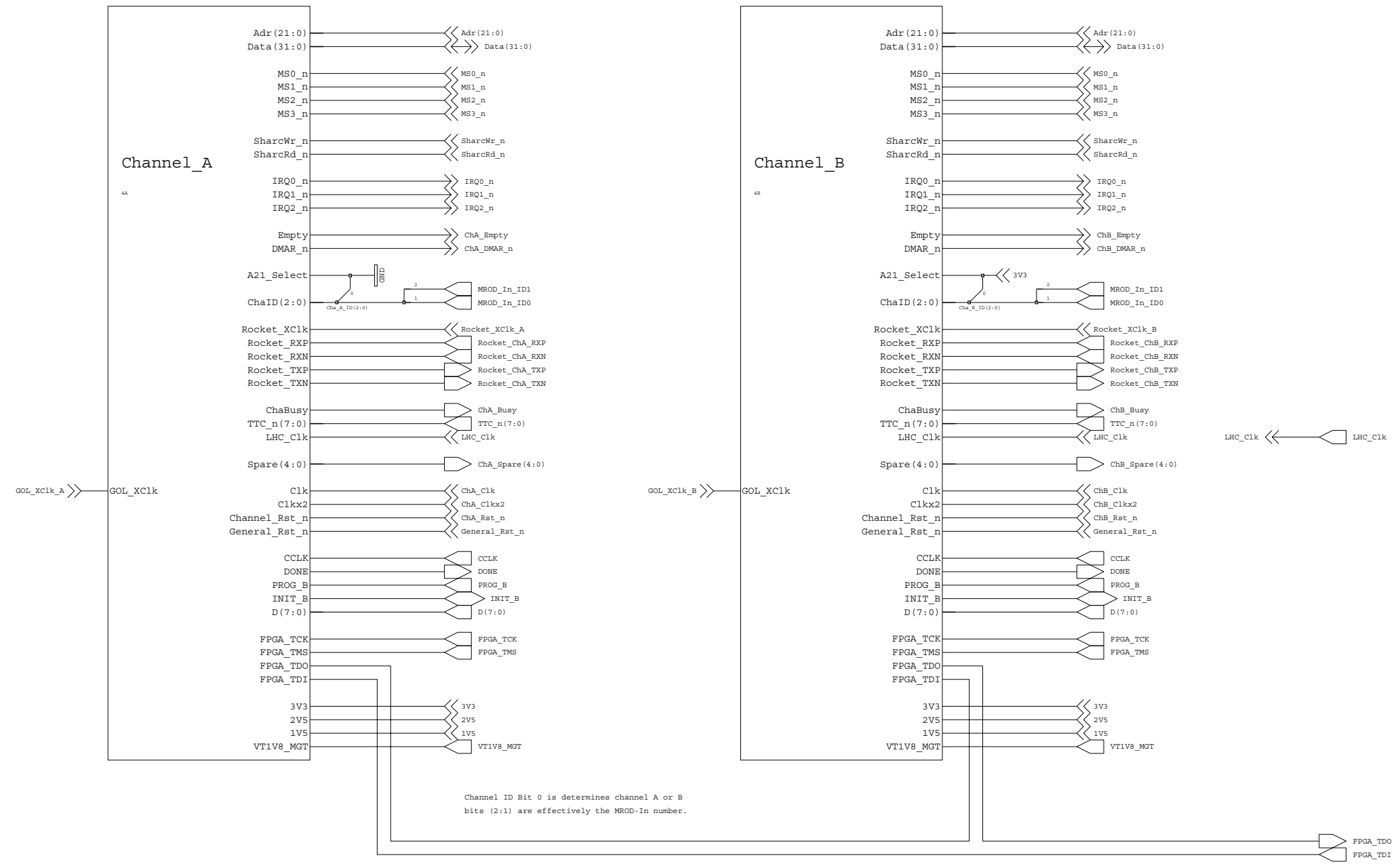
MROD- In		Rev	V2	2						
		Date	7 Feb 2006							
SHARC Auxiliary and Decoupling		Time	1:46:57 pm							
Proj:	MROD-X	Proj.No:	38405							
Peter Jansweijer		peterj@nikhef.nl								
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND			Size	A3	4	1	4	A
					Dim	420 x 297 mm				
					Page	3 of 4				



MROD- In		Rev	V2	20						
		Date	7 Feb 2006							
Power and Clocks		Time	1:47:20 pm							
Proj:	MROD-X	Proj.No:	38405							
Peter Jansweijer		peterj@nikhef.nl								
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND			Size	A3	4	1	4	A
					Dim	420 x 297 mm				
					Page	4 of 4				



Power Supply		Rev	V2	2
		Date	7 Feb 2006	
5V -> 1V5 @ 2A		Time	1:38:24 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>© ET-Nikhef Amsterdam</small>	<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>	Dim	420 x 297 mm	
		Page	1	of



MROD- In		Rev	V2	2
		Date	7 Feb 2006	
Input Channels		Time	1:45:51 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		Name	tonvr	
peterj@nikhef.nl		Size	A3	4 1 4 A
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Dim	420 x 297 mm	
		Page	1 of 4	

IC401
ADSP21160N

A1	DATA(14)	A2	DATA(13)	A3	DATA(10)	A4	DATA(8)	A5	DATA(4)	A6	DATA(2)	A7	TDI	A8	TRST_n	A9	RESET_n	A10	PPBA	A11	IRQ0_n	A12	FLAG1	A13	TMEXF	A14	MC_A14	A15	MC_A15	A16	TPF1	A17	RFS1	A18	RCLK0	A19	DT0	A20	LOGAT(4)
B1	DATA(22)	B2	DATA(16)	B3	DATA(15)	B4	DATA(9)	B5	DATA(6)	B6	DATA(3)	B7	DATA(0)	B8	TCK	B9	Sharc_BMU_n	B10	IRQ0_n	B11	ChB_Empty	B12	FLAG0	B13	MC_B13	B14	MC_B14	B15	DT1	B16	RCLK1	B17	RFS0	B18	TCLK0	B19	LOGAT(5)	B20	LOGAT(2)
C1	DATA(24)	C2	DATA(18)	C3	DATA(17)	C4	DATA(11)	C5	DATA(7)	C6	DATA(5)	C7	DATA(1)	C8	TMS	C9	TDO	C10	IRQ1_n	C11	ChA_Empty	C12	MC_C12	C13	MC_C13	C14	TCLK1	C15	DT1	C16	DT0	C17	LOGAT(7)	C18	LOGAT(6)	C19	LOGAT(3)	C20	LOGAT(0)
D1	DATA(28)	D2	DATA(25)	D3	DATA(20)	D4	DATA(19)	D5	DATA(12)	D6	VDDINT_06	D7	VDDINT_07	D8	VDDINT_08	D9	VDDINT_09	D10	VDDINT_10	D11	VDDINT_11	D12	VDDINT_12	D13	VDDINT_13	D14	VDDINT_14	D15	TPF0	D16	L1DAT(7)	D17	LOCLK	D18	LOGAT(3)	D19	LOGAT(1)	D20	L1CLK
E1	DATA(30)	E2	DATA(29)	E3	DATA(23)	E4	DATA(21)	E5	VDDINT_05	E6	VDDINT_04	E7	VDDINT_03	E8	VDDINT_02	E9	VDDINT_01	E10	VDDINT_00	E11	GND	E12	VDDINT	E13	VDDINT	E14	VDDINT	E15	TPF0	E16	L1DAT(7)	E17	LOCLK	E18	LOGAT(3)	E19	LOGAT(1)	E20	L1CLK
F1	DATA(34)	F2	DATA(33)	F3	DATA(27)	F4	DATA(26)	F5	VDDINT_05	F6	VDDINT_04	F7	GND_07	F8	GND_08	F9	GND_09	F10	GND_10	F11	GND_11	F12	GND_12	F13	GND_13	F14	GND_14	F15	VDDINT_05	F16	VDDINT_04	F17	L1DAT(4)	F18	L1DAT(3)	F19	L1DAT(0)	F20	L2DAT(7)
G1	DATA(38)	G2	DATA(35)	G3	DATA(32)	G4	DATA(31)	G5	VDDINT_05	G6	VDDINT_04	G7	GND_07	G8	GND_08	G9	GND_09	G10	GND_10	G11	GND_11	G12	GND_12	G13	GND_13	G14	GND_14	G15	VDDINT_05	G16	VDDINT_04	G17	L1DAT(4)	G18	L1DAT(3)	G19	L1DAT(0)	G20	L2DAT(7)
H1	DATA(40)	H2	DATA(39)	H3	DATA(37)	H4	DATA(34)	H5	VDDINT_05	H6	VDDINT_04	H7	GND_07	H8	GND_08	H9	GND_09	H10	GND_10	H11	GND_11	H12	GND_12	H13	GND_13	H14	GND_14	H15	VDDINT_05	H16	VDDINT_04	H17	L1DAT(4)	H18	L1DAT(3)	H19	L1DAT(0)	H20	L2DAT(7)
I1	DATA(44)	I2	DATA(43)	I3	DATA(42)	I4	DATA(41)	I5	VDDINT_05	I6	VDDINT_04	I7	GND_07	I8	GND_08	I9	GND_09	I10	GND_10	I11	GND_11	I12	GND_12	I13	GND_13	I14	GND_14	I15	VDDINT_05	I16	VDDINT_04	I17	L1DAT(4)	I18	L1DAT(3)	I19	L1DAT(0)	I20	L2DAT(7)
J1	DATA(48)	J2	DATA(47)	J3	DATA(46)	J4	DATA(45)	J5	VDDINT_05	J6	VDDINT_04	J7	GND_07	J8	GND_08	J9	GND_09	J10	GND_10	J11	GND_11	J12	GND_12	J13	GND_13	J14	GND_14	J15	VDDINT_05	J16	VDDINT_04	J17	L1DAT(4)	J18	L1DAT(3)	J19	L1DAT(0)	J20	L2DAT(7)
K1	CLK_CFG_0	K2	DATA(44)	K3	DATA(45)	K4	DATA(47)	K5	VDDINT_05	K6	VDDINT_04	K7	GND_07	K8	GND_08	K9	GND_09	K10	GND_10	K11	GND_11	K12	GND_12	K13	GND_13	K14	GND_14	K15	VDDINT_05	K16	VDDINT_04	K17	BREQ_n	K18	BREQ_n	K19	BREQ_n	K20	BREQ_n
L1	CLKIN	L2	CLK_CFG_1	L3	AGND	L4	CLK_CFG_2	L5	VDDINT_05	L6	VDDINT_04	L7	GND_07	L8	GND_08	L9	GND_09	L10	GND_10	L11	GND_11	L12	GND_12	L13	GND_13	L14	GND_14	L15	VDDINT_05	L16	VDDINT_04	L17	BREQ_n	L18	BREQ_n	L19	BREQ_n	L20	BREQ_n
M1	AVDD	M2	CLK_CFG_3	M3	CLKOUT	M4	MC_BM4	M5	VDDINT_05	M6	VDDINT_04	M7	GND_07	M8	GND_08	M9	GND_09	M10	GND_10	M11	GND_11	M12	GND_12	M13	GND_13	M14	GND_14	M15	VDDINT_05	M16	VDDINT_04	M17	BREQ_n	M18	BREQ_n	M19	BREQ_n	M20	BREQ_n
N1	AVDD	GND	DATA(1)	N4	DATA(1)	N5	VDDINT_05	N6	VDDINT_04	N7	GND_07	N8	GND_08	N9	GND_09	N10	GND_10	N11	GND_11	N12	GND_12	N13	GND_13	N14	GND_14	N15	VDDINT_05	N16	VDDINT_04	N17	BREQ_n	N18	BREQ_n	N19	BREQ_n	N20	BREQ_n		
O1	DATA(49)	O2	DATA(50)	O3	DATA(52)	O4	DATA(55)	O5	VDDINT_05	O6	VDDINT_04	O7	GND_07	O8	GND_08	O9	GND_09	O10	GND_10	O11	GND_11	O12	GND_12	O13	GND_13	O14	GND_14	O15	VDDINT_05	O16	VDDINT_04	O17	L1DAT(5)	O18	L1DAT(6)	O19	L1DAT(4)	O20	L1CLK
P1	DATA(17)	P2	DATA(18)	P3	DATA(20)	P4	DATA(23)	P5	VDDINT_05	P6	VDDINT_04	P7	GND_07	P8	GND_08	P9	GND_09	P10	GND_10	P11	GND_11	P12	GND_12	P13	GND_13	P14	GND_14	P15	VDDINT_05	P16	VDDINT_04	P17	L1DAT(5)	P18	L1DAT(6)	P19	L1DAT(4)	P20	L1CLK
Q1	DATA(53)	Q2	DATA(54)	Q3	DATA(57)	Q4	DATA(60)	Q5	VDDINT_05	Q6	VDDINT_04	Q7	GND_07	Q8	GND_08	Q9	GND_09	Q10	GND_10	Q11	GND_11	Q12	GND_12	Q13	GND_13	Q14	GND_14	Q15	VDDINT_05	Q16	VDDINT_04	Q17	L1DAT(5)	Q18	L1DAT(6)	Q19	L1DAT(4)	Q20	L1CLK
R1	DATA(21)	R2	DATA(22)	R3	DATA(25)	R4	DATA(28)	R5	VDDINT_05	R6	VDDINT_04	R7	GND_07	R8	GND_08	R9	GND_09	R10	GND_10	R11	GND_11	R12	GND_12	R13	GND_13	R14	GND_14	R15	VDDINT_05	R16	VDDINT_04	R17	L1DAT(5)	R18	L1DAT(6)	R19	L1DAT(4)	R20	L1CLK
S1	DATA(56)	S2	DATA(58)	S3	DATA(59)	S4	DATA(63)	S5	VDDINT_05	S6	VDDINT_04	S7	VDDINT_07	S8	VDDINT_08	S9	VDDINT_09	S10	VDDINT_10	S11	VDDINT_11	S12	VDDINT_12	S13	VDDINT_13	S14	VDDINT_14	S15	VDDINT_15	S16	VDDINT_16	S17	L1DAT(3)	S18	L1DAT(1)	S19	L1DAT(0)	S20	L1CLK
T1	DATA(61)	T2	DATA(62)	T3	ADDR(3)	T4	ADDR(2)	T5	VDDINT_05	T6	VDDINT_04	T7	VDDINT_07	T8	VDDINT_08	T9	VDDINT_09	T10	VDDINT_10	T11	VDDINT_11	T12	VDDINT_12	T13	VDDINT_13	T14	VDDINT_14	T15	VDDINT_15	T16	VDDINT_16	T17	L1DAT(3)	T18	L1DAT(1)	T19	L1DAT(0)	T20	L1CLK
U1	ADDR(4)	U2	ADDR(6)	U3	ADDR(17)	U4	ADDR(10)	U5	ADDR(14)	U6	ADDR(18)	U7	ADDR(22)	U8	ADDR(25)	U9	ADDR(28)	U10	ADDR(31)	U11	ADDR(35)	U12	ADDR(39)	U13	ADDR(43)	U14	ADDR(47)	U15	ADDR(51)	U16	ADDR(55)	U17	ADDR(59)	U18	ADDR(63)	U19	ADDR(67)	U20	ADDR(71)
V1	ADDR(5)	V2	ADDR(8)	V3	ADDR(12)	V4	ADDR(15)	V5	ADDR(19)	V6	ADDR(23)	V7	ADDR(27)	V8	ADDR(31)	V9	ADDR(35)	V10	ADDR(39)	V11	ADDR(43)	V12	ADDR(47)	V13	ADDR(51)	V14	ADDR(55)	V15	ADDR(59)	V16	ADDR(63)	V17	ADDR(67)	V18	ADDR(71)	V19	ADDR(75)	V20	ADDR(79)
W1	ADDR(6)	W2	ADDR(11)	W3	ADDR(13)	W4	ADDR(16)	W5	ADDR(19)	W6	ADDR(21)	W7	ADDR(24)	W8	ADDR(27)	W9	ADDR(30)	W10	ADDR(33)	W11	ADDR(36)	W12	ADDR(39)	W13	ADDR(42)	W14	ADDR(45)	W15	ADDR(48)	W16	ADDR(51)	W17	ADDR(54)	W18	ADDR(57)	W19	ADDR(60)	W20	ADDR(63)
X1	ADDR(7)	X2	ADDR(12)	X3	ADDR(14)	X4	ADDR(17)	X5	ADDR(20)	X6	ADDR(23)	X7	ADDR(26)	X8	ADDR(29)	X9	ADDR(32)	X10	ADDR(35)	X11	ADDR(38)	X12	ADDR(41)	X13	ADDR(44)	X14	ADDR(47)	X15	ADDR(50)	X16	ADDR(53)	X17	ADDR(56)	X18	ADDR(59)	X19	ADDR(62)	X20	ADDR(65)
Y1	ADDR(8)	Y2	ADDR(11)	Y3	ADDR(13)	Y4	ADDR(16)	Y5	ADDR(19)	Y6	ADDR(21)	Y7	ADDR(24)	Y8	ADDR(27)	Y9	ADDR(30)	Y10	ADDR(33)	Y11	ADDR(36)	Y12	ADDR(39)	Y13	ADDR(42)	Y14	ADDR(45)	Y15	ADDR(48)	Y16	ADDR(51)	Y17	ADDR(54)	Y18	ADDR(57)	Y19	ADDR(60)	Y20	ADDR(63)

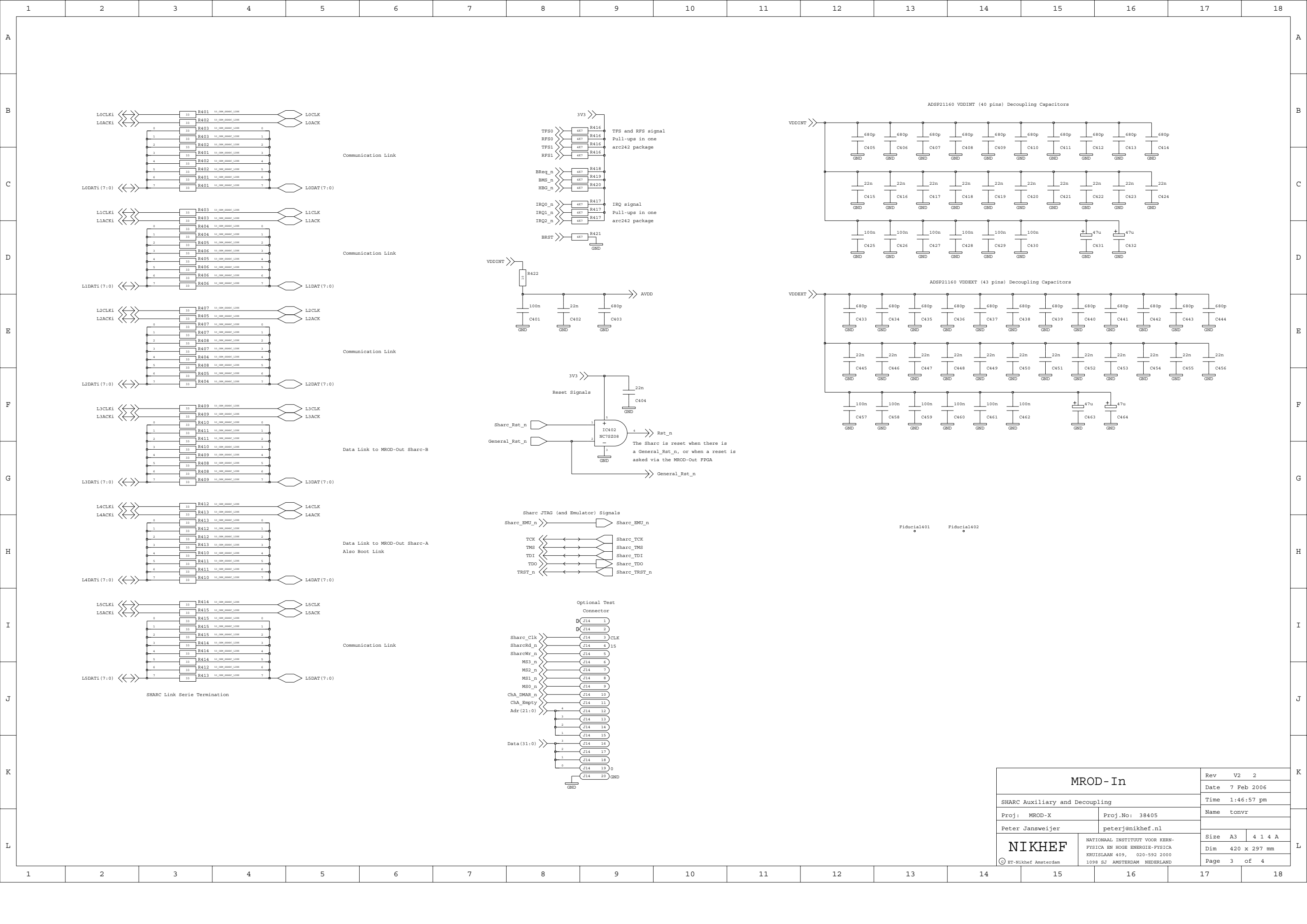
Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

ID = "000"

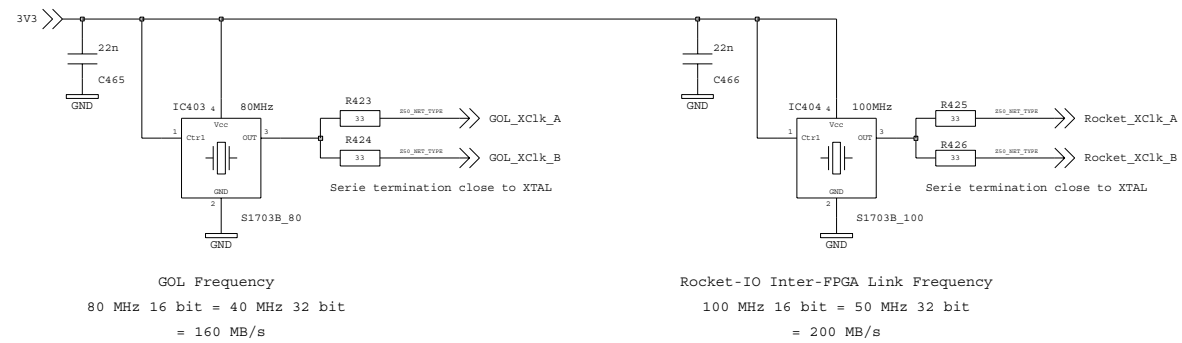
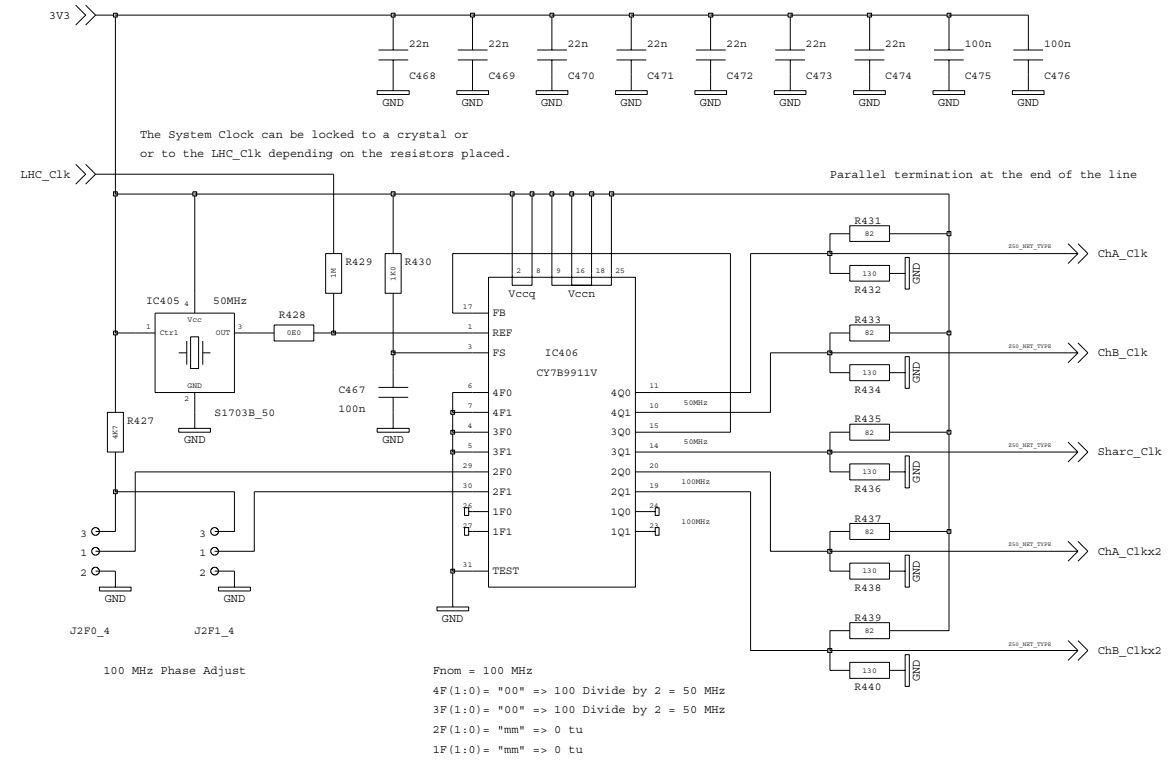
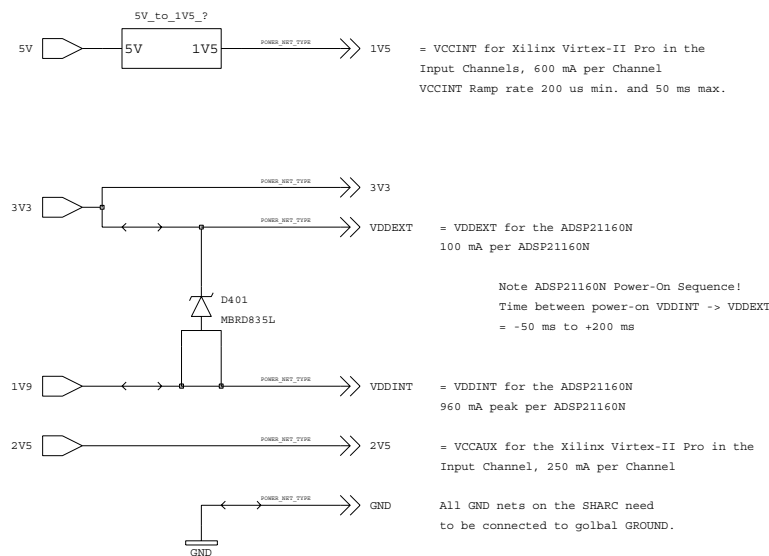
Booting Mode:
EBOOT = '0', LBOOT = '1', BMS_n = '1' (Input)
=> Link Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

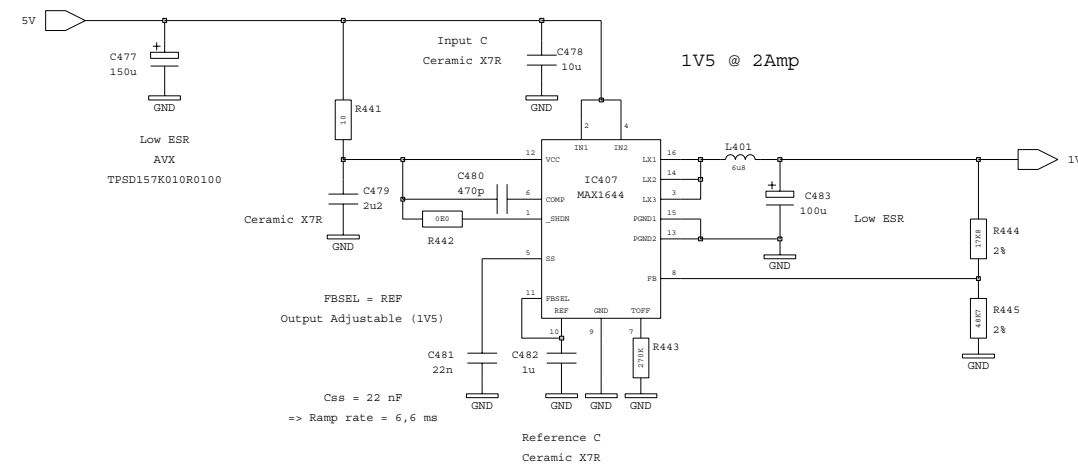
MROD- In		Rev	V2	2
		Date	7 Feb 2006	
SHARC		Time	1:46:33 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF NATIONAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Dim	420 x 297 mm	
		Page	2 of 4	



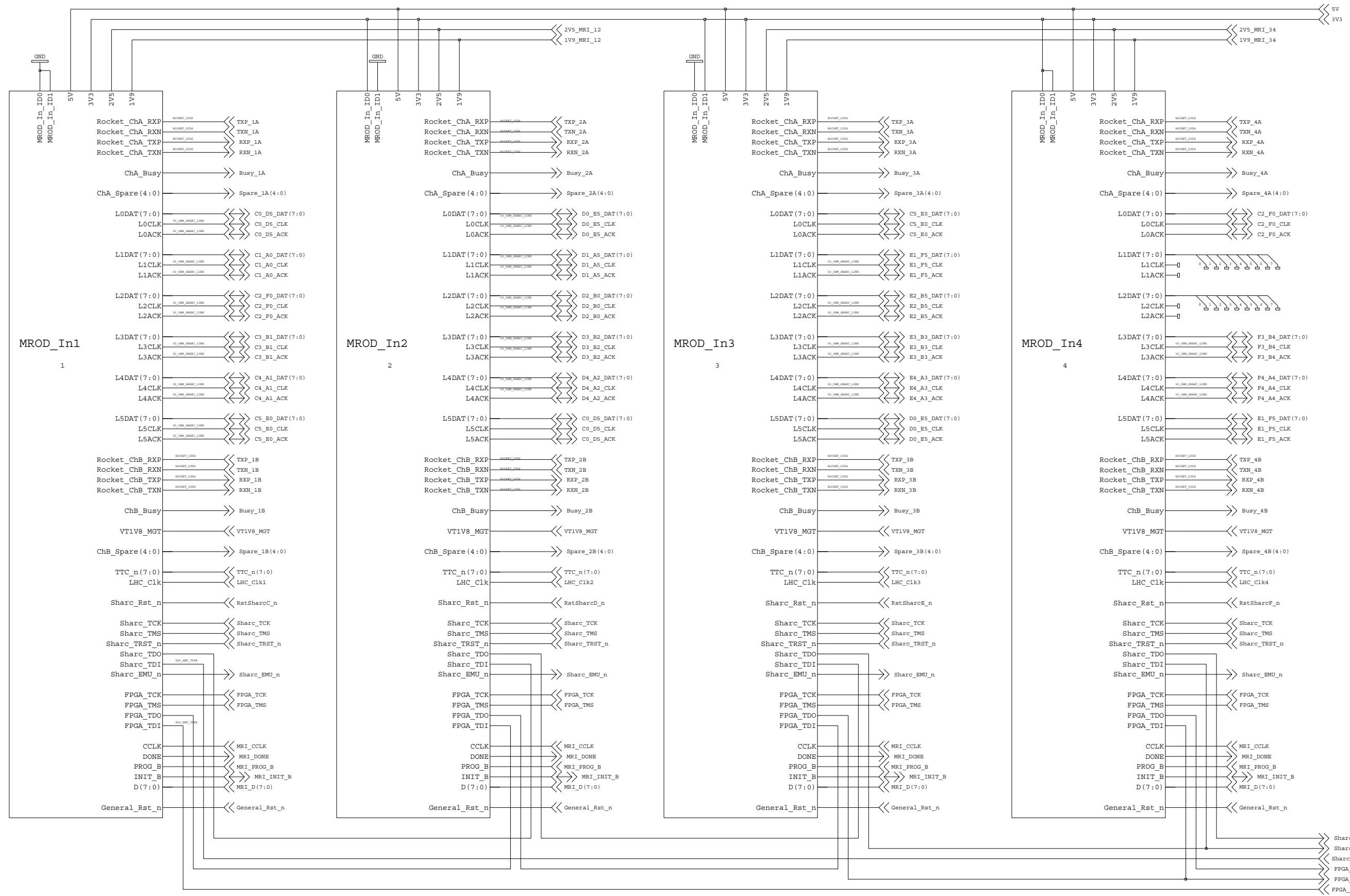
MROD- In		Rev V2 2
		Date 7 Feb 2006
SHARC Auxiliary and Decoupling		Time 1:46:57 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF		NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND
© ET-Nikhef Amsterdam		Size A3 4 1 4 A Dim 420 x 297 mm Page 3 of 4



MROD- In		Rev	V2	20	
		Date	7 Feb 2006		
Power and Clocks		Time	1:47:20 pm		
Proj:	MROD-X	Proj.No:	38405		
Peter Jansweijer		peterj@nikhef.nl			
NIKHEF NATIONAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size	A3	4 1 4 A	
		Dim	420 x 297 mm		
		Page	4 of 4		



Power Supply		Rev	V2	2
5V -> 1V5 @ 2A		Date	7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time	1:38:24 pm	
Peter Jansweijer	peterj@nikhef.nl	Name	tonvr	
NIKHEF		Size	A3	4 1 4 A
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Dim	420 x 297 mm	
© ET-Nikhef Amsterdam		Page	1 of 1	



MROD-Out		Rev	V2	3
		Date	7 Feb 2006	
MROD-Ins		Time	1:25:06 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOOG ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Dim	420 x 297 mm	
		Page	1 of 19	

IC501
ADSP21160N

A1	DATA(14)	A2	DATA(13)	A3	DATA(10)	A4	DATA(8)	A5	DATA(4)	A6	DATA(2)	A7	TRST_n	A8	RESET_n	A10	RSPA	A11	IRQ0_n	A12	FLAG1	A13	TIMEP	A14	NC_A14	A15	NC_A15	A16	TPS1a	A17	RFS1a	A18	RFS1a	A19	DT0	A20	LOGAT(4)	A21	LOGAT(5)	A22	LOGAT(2)
B1	DATA(22)	B2	DATA(16)	B3	DATA(15)	B4	DATA(9)	B5	DATA(6)	B6	DATA(3)	B7	DATA(0)	B8	Share_TCK	B9	Share_EMU_n	B10	IRQ2a_n	B11	FLAG2	B12	FLAG0	B13	NC_B13	B14	NC_B14	B15	DT1	B16	RCLS2	B17	RFS1a	B18	RFS0a	B19	TCLK0	B20	LOGAT(5)	B21	LOGAT(2)
C1	DATA(24)	C2	DATA(18)	C3	DATA(17)	C4	DATA(11)	C5	DATA(7)	C6	DATA(5)	C7	DATA(1)	C8	Share_TMS	C9	Share_TDO	C10	IRQ1a_n	C11	FLAG2	C12	NC_C12	C13	NC_C13	C14	DT1	C15	DT1	C16	DT0	C17	LOGAT(7)	C18	LOGAT(6)	C19	LOGAT(4)	C20	LOGAT(5)		
D1	DATA(28)	D2	DATA(25)	D3	DATA(20)	D4	DATA(19)	D5	DATA(12)	D6	VDDEXT_04	D7	VDDINT_07	D8	VDDEXT_08	D9	VDDEXT_09	D10	VDDEXT_010	D11	VDDEXT_011	D12	VDDEXT_012	D13	VDDINT_013	D14	VDDEXT_014	D15	TPS0a	D16	L1DATA(7)	D17	LOGAT(7)	D18	LOGAT(6)	D19	LOGAT(3)	D20	LOGAT(1)	D21	L1CLK
E1	DATA(30)	E2	DATA(29)	E3	DATA(23)	E4	DATA(21)	E5	VDDEXT_05	E6	VDDINT_06	E7	VDDINT_07	E8	VDDINT_08	E9	VDDINT_09	E10	VDDINT_010	E11	VDDINT_011	E12	VDDINT_012	E13	VDDINT_013	E14	VDDINT_014	E15	VDDINT_015	E16	VDDEXT_016	E17	L1DATA(6)	E18	L1DATA(5)	E19	L1DATA(5)	E20	L1DATA(1)	E21	L1DATA(1)
F1	DATA(34)	F2	DATA(33)	F3	DATA(27)	F4	DATA(26)	F5	VDDEXT_05	F6	VDDINT_06	F7	GND	F8	GND	F9	GND	F10	GND	F11	GND	F12	GND	F13	GND	F14	GND	F15	VDDINT_015	F16	VDDEXT_016	F17	L1DATA(4)	F18	L1DATA(3)	F19	L1DATA(3)	F20	L1DATA(0)	F21	L2DATA(7)
G1	DATA(38)	G2	DATA(35)	G3	DATA(32)	G4	DATA(31)	G5	VDDEXT_05	G6	VDDINT_06	G7	GND	G8	GND	G9	GND	G10	GND	G11	GND	G12	GND	G13	GND	G14	GND	G15	VDDINT_015	G16	VDDEXT_016	G17	L1DATA(2)	G18	L2DATA(6)	G19	L2DATA(4)	G20	L2CLK		
H1	DATA(40)	H2	DATA(39)	H3	DATA(37)	H4	DATA(36)	H5	VDDEXT_05	H6	VDDINT_06	H7	GND	H8	GND	H9	GND	H10	GND	H11	GND	H12	GND	H13	GND	H14	GND	H15	VDDINT_015	H16	VDDEXT_016	H17	L2DATA(5)	H18	L2DATA(3)	H19	L2DATA(3)	H20	L2DATA(1)		
I1	DATA(44)	I2	DATA(43)	I3	DATA(42)	I4	DATA(41)	I5	VDDEXT_05	I6	VDDINT_06	I7	GND	I8	GND	I9	GND	I10	GND	I11	GND	I12	GND	I13	GND	I14	GND	I15	VDDINT_015	I16	VDDEXT_016	I17	L2DATA(2)	I18	L2DATA(2)	I19	HBB_n	I20	HBB_n		
J1	DATA(44)	J2	DATA(43)	J3	DATA(42)	J4	DATA(41)	J5	VDDEXT_05	J6	VDDINT_06	J7	GND	J8	GND	J9	GND	J10	GND	J11	GND	J12	GND	J13	GND	J14	GND	J15	VDDINT_015	J16	VDDEXT_016	J17	L2DATA(2)	J18	L2DATA(2)	J19	HBB_n	J20	HBB_n		
K1	CLK_CFG_0	K2	DATA(46)	K3	DATA(45)	K4	DATA(47)	K5	VDDEXT_05	K6	VDDINT_06	K7	GND	K8	GND	K9	GND	K10	GND	K11	GND	K12	GND	K13	GND	K14	GND	K15	VDDINT_015	K16	VDDEXT_016	K17	BR6_n	K18	BR6_n	K19	BR6_n	K20	BR6_n		
L1	CLKIN	L2	CLK_CFG_1	L3	AGND	L4	CLK_CFG_2	L5	VDDEXT_05	L6	VDDINT_06	L7	GND	L8	GND	L9	GND	L10	GND	L11	GND	L12	GND	L13	GND	L14	GND	L15	VDDINT_015	L16	VDDEXT_016	L17	BR6_n	L18	BR6_n	L19	BR6_n	L20	BR6_n		
M1	AVDD	M2	CLK_CFG_3	M3	CLKOUT	M4	NC_M4	M5	VDDEXT_05	M6	VDDINT_06	M7	GND	M8	GND	M9	GND	M10	GND	M11	GND	M12	GND	M13	GND	M14	GND	M15	VDDINT_015	M16	VDDEXT_016	M17	PAGE	M18	PAGE	M19	PAGE	M20	L1DATA(7)		
N1	NC_N1	N2	NC_N2	N3	DATA(48)	N4	DATA(51)	N5	VDDEXT_05	N6	VDDINT_06	N7	GND	N8	GND	N9	GND	N10	GND	N11	GND	N12	GND	N13	GND	N14	GND	N15	VDDINT_015	N16	VDDEXT_016	N17	L3DATA(5)	N18	L3DATA(6)	N19	L3DATA(4)	N20	L3CLK		
O1	DATA(49)	O2	DATA(50)	O3	DATA(52)	O4	DATA(55)	O5	VDDEXT_05	O6	VDDINT_06	O7	GND	O8	GND	O9	GND	O10	GND	O11	GND	O12	GND	O13	GND	O14	GND	O15	VDDINT_015	O16	VDDEXT_016	O17	L3DATA(2)	O18	L3DATA(1)	O19	L3DATA(3)	O20	L3ACK		
P1	DATA(53)	P2	DATA(54)	P3	DATA(57)	P4	DATA(60)	P5	VDDEXT_05	P6	VDDINT_06	P7	GND	P8	GND	P9	GND	P10	GND	P11	GND	P12	GND	P13	GND	P14	GND	P15	VDDINT_015	P16	VDDEXT_016	P17	L4DATA(5)	P18	L4DATA(6)	P19	L4DATA(7)	P20	L4DATA(0)		
Q1	DATA(56)	Q2	DATA(58)	Q3	DATA(59)	Q4	DATA(63)	Q5	VDDEXT_05	Q6	VDDINT_06	Q7	GND	Q8	GND	Q9	GND	Q10	GND	Q11	VDDINT_011	Q12	VDDINT_012	Q13	VDDINT_013	Q14	VDDINT_014	Q15	VDDINT_015	Q16	VDDEXT_016	Q17	L4DATA(3)	Q18	L4DATA(3)	Q19	L4CLK	Q20	L4DATA(4)		
R1	DATA(61)	R2	DATA(62)	R3	ADDR(3)	R4	ADDR(2)	R5	VDDEXT_05	R6	VDDEXT_06	R7	VDDEXT_07	R8	VDDEXT_08	R9	VDDEXT_09	R10	VDDEXT_010	R11	VDDEXT_011	R12	VDDEXT_012	R13	VDDEXT_013	R14	VDDEXT_014	R15	VDDEXT_015	R16	VDDEXT_016	R17	LOGAT(7)	R18	L4DATA(0)	R19	L4DATA(1)	R20	L4DATA(2)		
S1	ADDR(4)	S2	ADDR(6)	S3	ADDR(7)	S4	ADDR(10)	S5	ADDR(14)	S6	ADDR(18)	S7	ADDR(22)	S8	ADDR(25)	S9	ADDR(28)	S10	ADDR(28)	S11	ADDR(1)	S12	MS1_n	S13	CSA_n	S14	RDL_n	S15	DMAR2_n	S16	L5DATA(0)	S17	L5DATA(2)	S18	L5ACK	S19	L5DATA(4)	S20	L5DATA(6)		
T1	ADDR(5)	T2	ADDR(9)	T3	ADDR(12)	T4	ADDR(15)	T5	ADDR(17)	T6	ADDR(20)	T7	ADDR(23)	T8	ADDR(26)	T9	ADDR(29)	T10	ADDR(29)	T11	ADDR(0)	T12	BMS_n	T13	MS2_n	T14	CIF_n	T15	RDW_n	T16	DMAG2_n	T17	GND	T18	L5DATA(1)	T19	L5DATA(3)	T20	L5DATA(5)		
U1	ADDR(8)	U2	ADDR(11)	U3	ADDR(13)	U4	ADDR(16)	U5	ADDR(19)	U6	ADDR(21)	U7	ADDR(24)	U8	ADDR(27)	U9	ADDR(30)	U10	ADDR(31)	U11	TD0	U12	BRST	U13	MS0_n	U14	MS3_n	U15	WRH_n	U16	WRL_n	U17	DMAG1_n	U18	DMAR1_n	U19	EBOOT	U20	L5CLK		
V1	ADDR(9)	V2	ADDR(11)	V3	ADDR(13)	V4	ADDR(16)	V5	ADDR(19)	V6	ADDR(21)	V7	ADDR(24)	V8	ADDR(27)	V9	ADDR(30)	V10	ADDR(31)	V11	TD0	V12	BRST	V13	MS0_n	V14	MS3_n	V15	WRH_n	V16	WRL_n	V17	DMAG1_n	V18	DMAR1_n	V19	EBOOT	V20	L5CLK		

Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

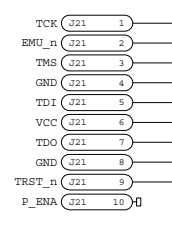
SHARC A
ID = "001"

Booting Mode:
EBOOT = '0', LBOOT = '0', BMS_n = '1' (Input)
=> Host Port Booting

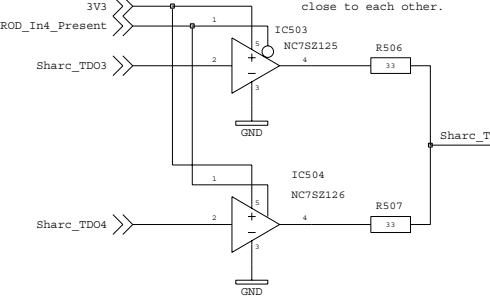
SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

MROD-Out		Rev	V2	3
		Date	7 Feb 2006	
SHARC-A		Time	1:25:29 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF © ET-Nikhef Amsterdam		Dim	420 x 297 mm	
		Page	2 of 19	
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND				

Note that pin 2 (EMU_n) and pin 9 (TRST_n) are not connected in the ByteBlaster

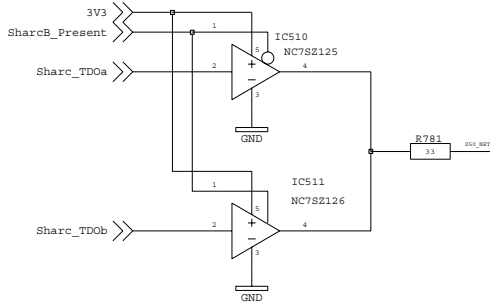


Series termination is added because Sharc_TDO might be a long traces. Place close to the buffers and buffers close to each other.

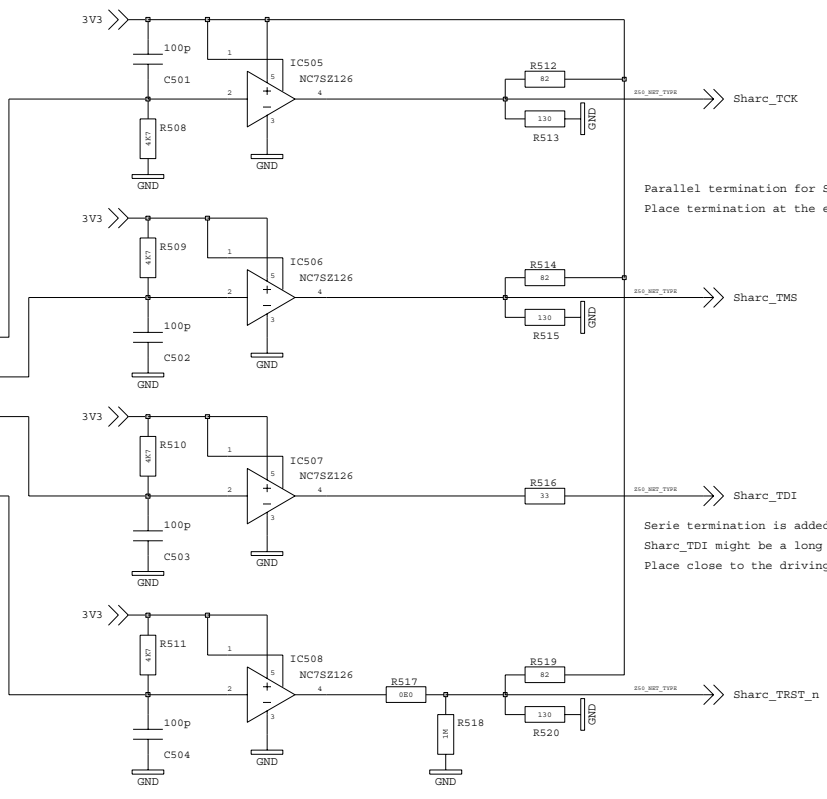
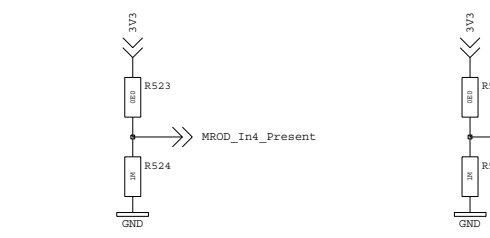


Select either Sharc_TDO3 or 4 depending on whether SharcF (MROD_In4) is placed on the board.
MROD_In4_Present = '0' => SharcF is absent.
MROD_In4_Present = '1' => SharcF is present.

Place R21 (0 ohm) when using the EZ-ICE. Check the pinout of J21!



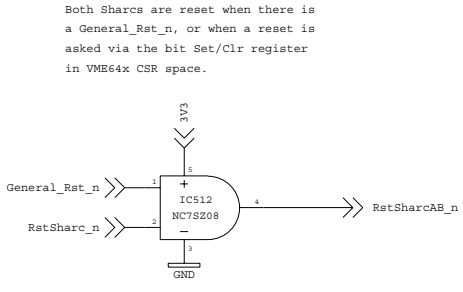
Select either Sharc_TDOa or b depending on whether SharcB is placed on the board.
Sharcb_Present = '0' => SharcB is absent.
Sharcb_Present = '1' => SharcB is present.



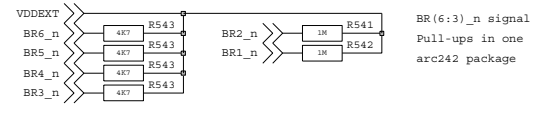
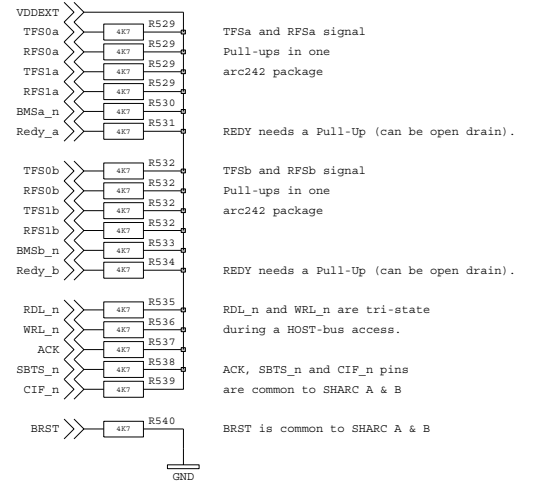
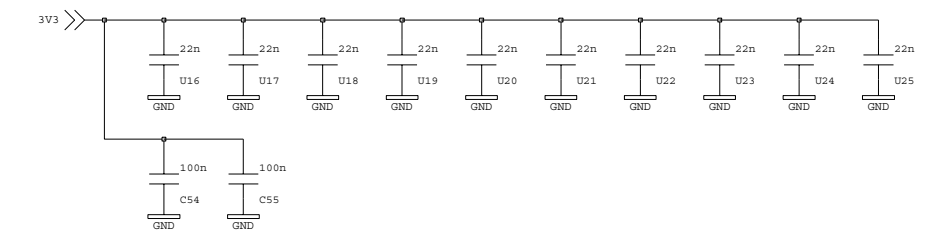
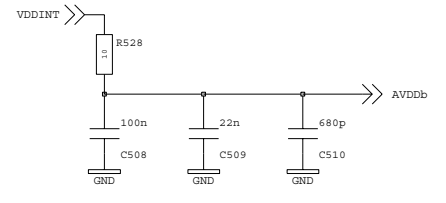
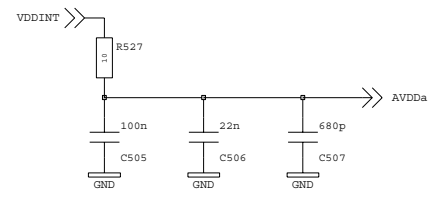
Parallel termination for Sharc_TCK/TMS. Place termination at the end of the line.

Series termination is added because Sharc_TDI might be a long trace. Place close to the driving buffer.

The SHARC Datasheet explicitly states that TRST_n is (Pulsed) Low after Power-Up. Note. Parallel Termination can be placed depending on the resistor configuration.



Both Sharcs are reset when there is a General_Rst_n, or when a reset is asked via the bit Set/Clr register in VME64x CSR space.

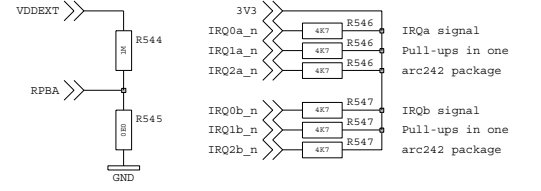


BR_n pins are common to SHARC A & B. Unused BR_n lines need Pull-Up (see datasheet). Note that BR2_n and BR1_n pull-ups can be installed when only SHARC A is mounted on the board.

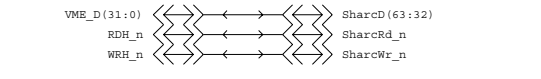
PAGE and PA_n are common to SHARC A & B. No need for Pull-Ups. MS0_n .. MS3_n, RDH_n, RDL_n, WRH_n and WRL_n are common to SHARC A & B and have internal Pull-Ups.

HBR_n and HBG_n are common to SHARC A & B. No need for Pull-Ups. HBR_n is always driven by the FPGA. HBG_n is always driven by the Bus Master.

DMAR1_n and DMAR2_n are common to SHARC A & B. No need for Pull-Ups. They are always driven by the FPGA. DMAG1_n and DMAG2_n are common to SHARC A & B. No need for Pull-Ups, they are driven by the Bus Master.

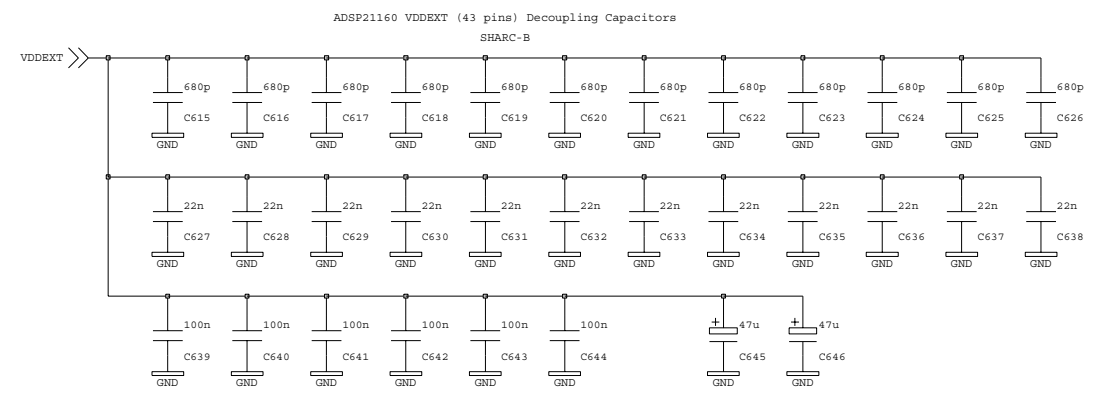
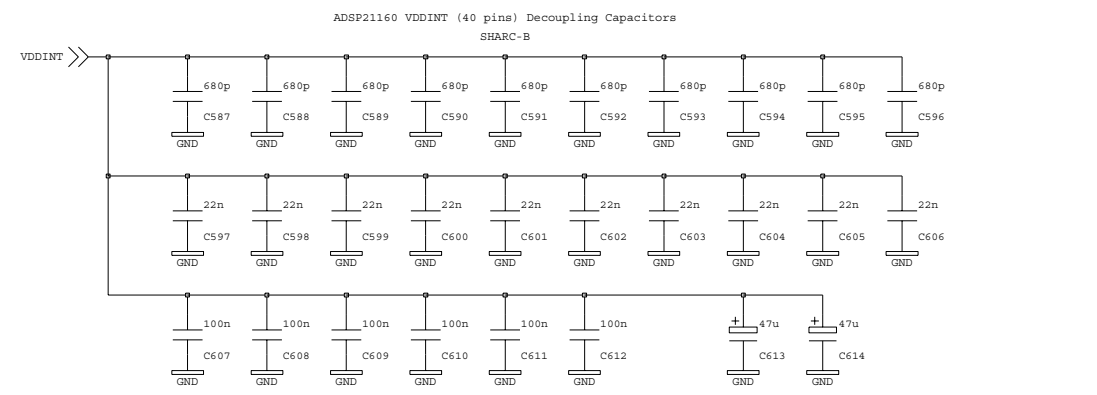
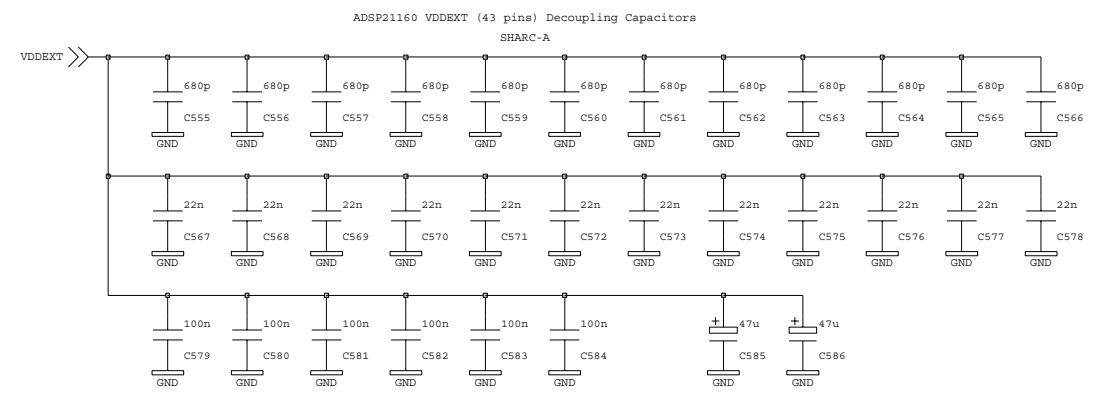
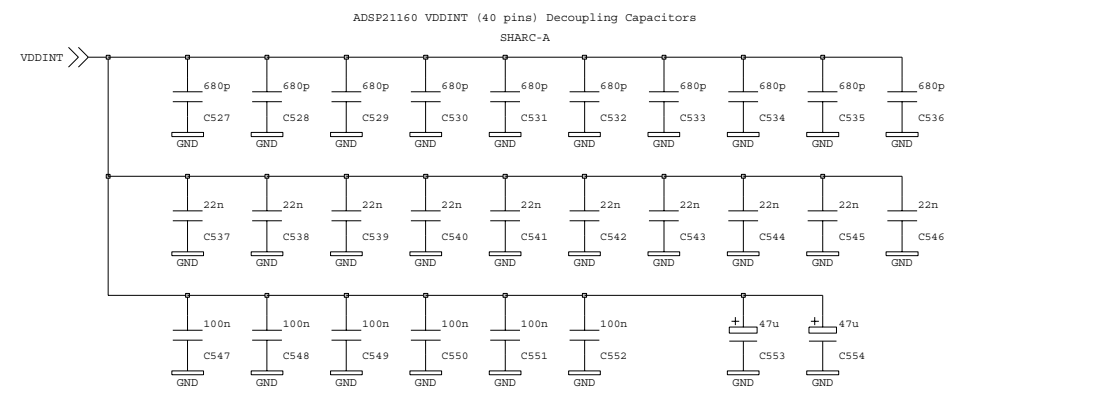
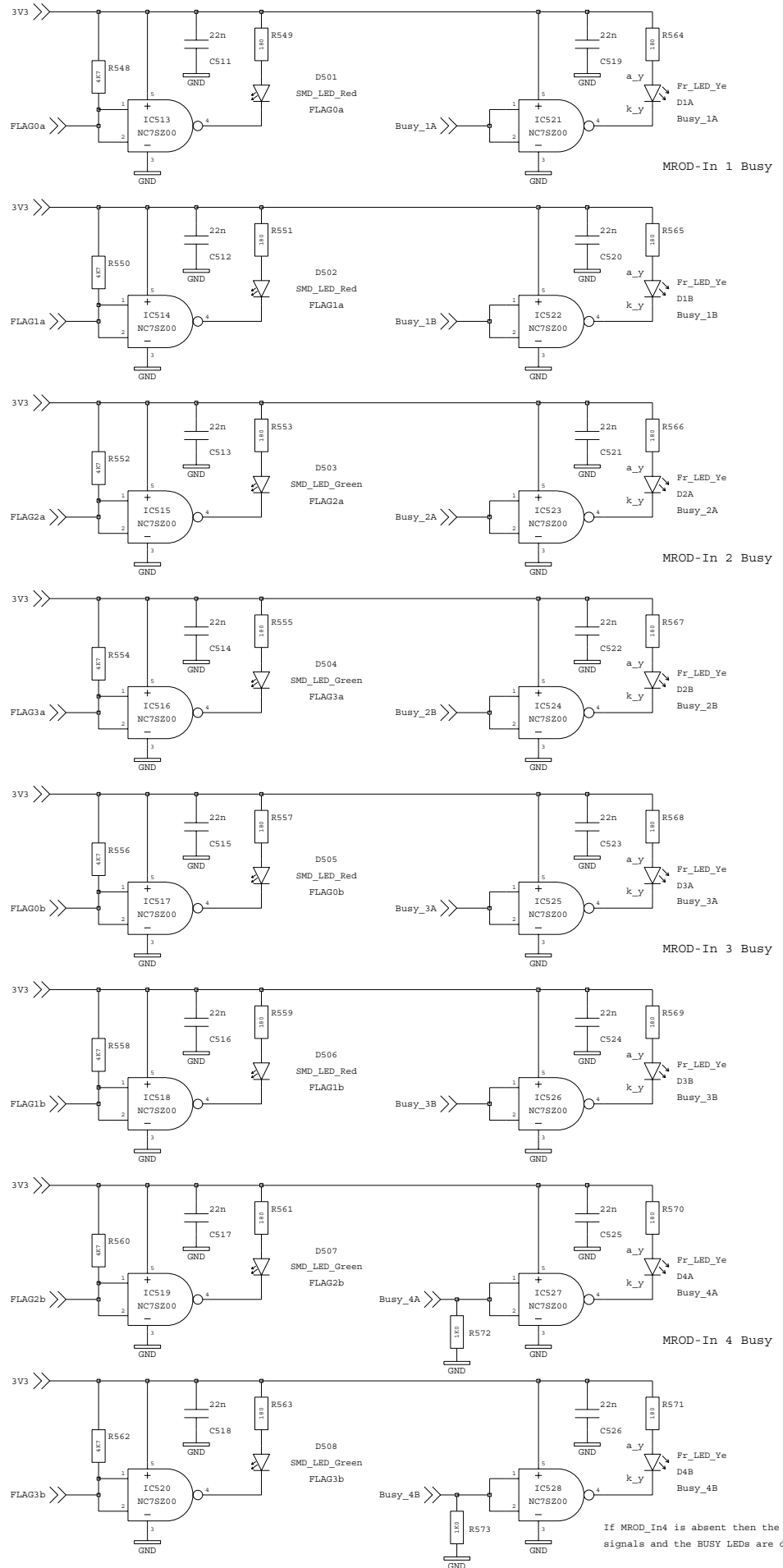


Rotating Priority Bus Arbitration select is set to "Fixed Priority" by default (SHARC A has priority).

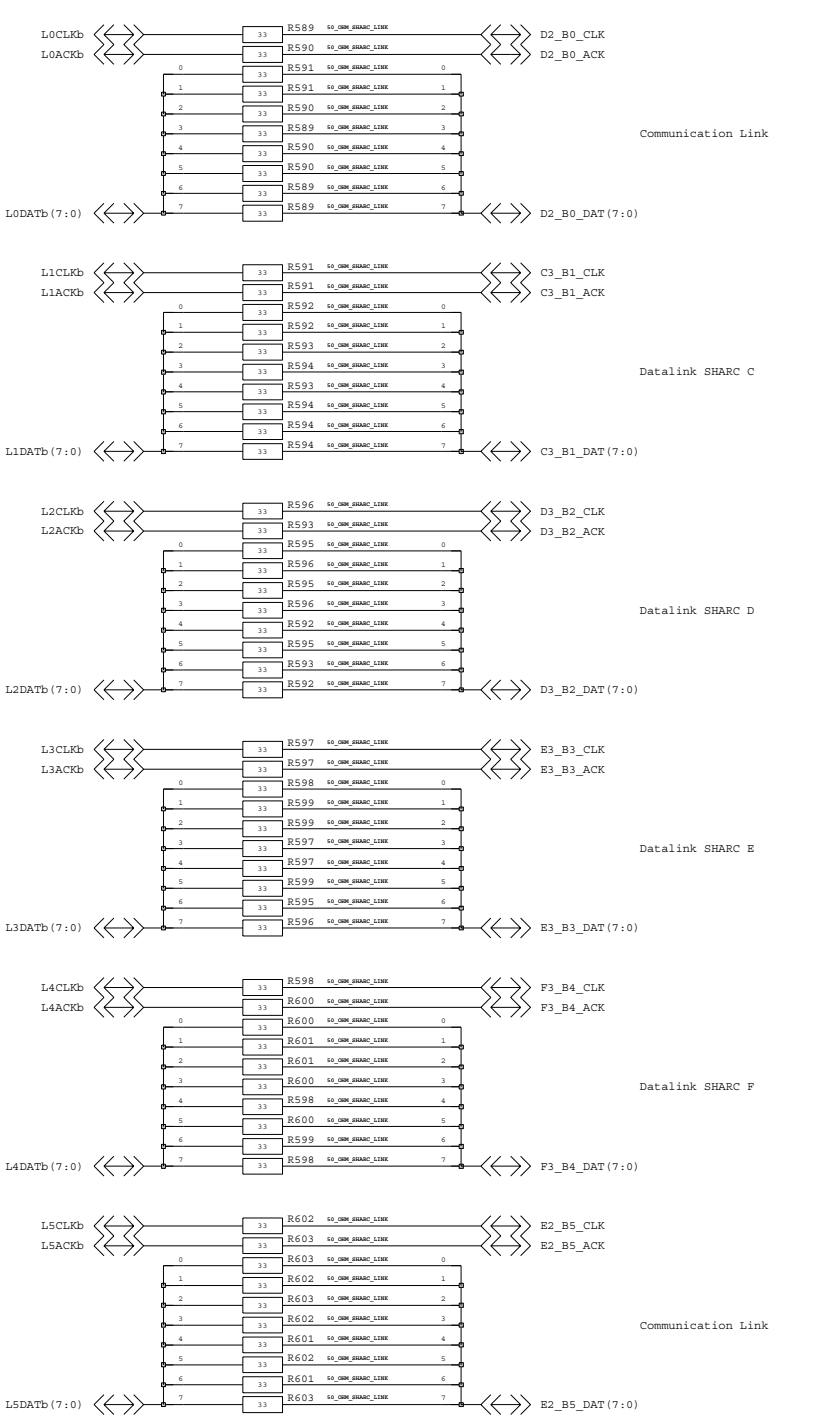
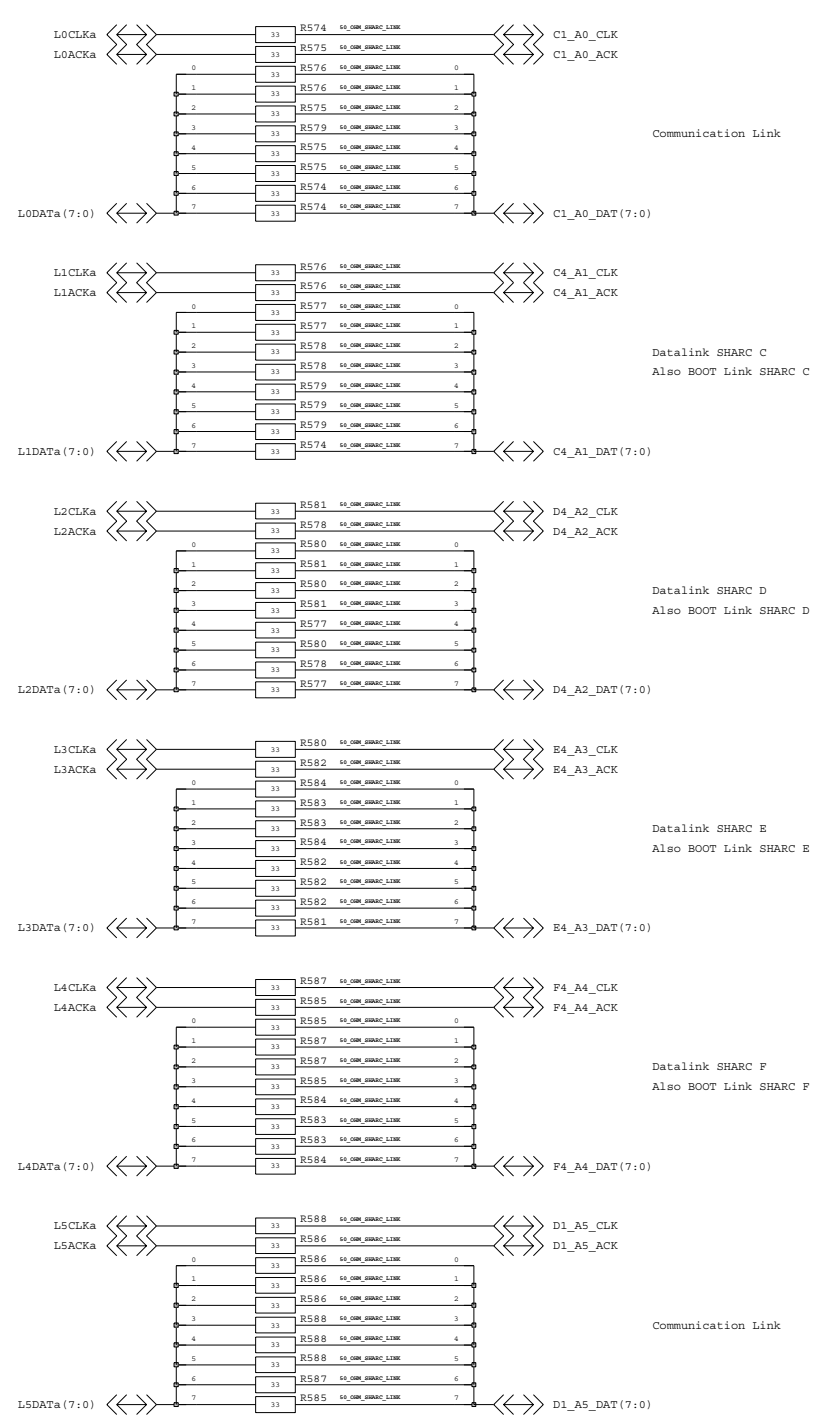


MROD-Out		Rev	V2	3	
		Date	7 Feb 2006		
SHARC JTAG and Auxiliary connections		Time	1:26:10 pm		
Proj:	MROD-X	Proj.No:	38405		
Peter Jansweijer		peterj@nikhef.nl			
NIKHEF © ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size	A3	4 1 4 A
			Dim	420 x 297 mm	
			Page	4 of 19	

Sharc Flag pin is an Input by default after Power-Up.
This means the LEDs light up during and after Power-Up.



MROD-Out		Rev	V2	3
		Date	7 Feb 2006	
SHARC Power Supply Decoupling and LEDs		Time	1:26:41 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
Page		5	of 19	



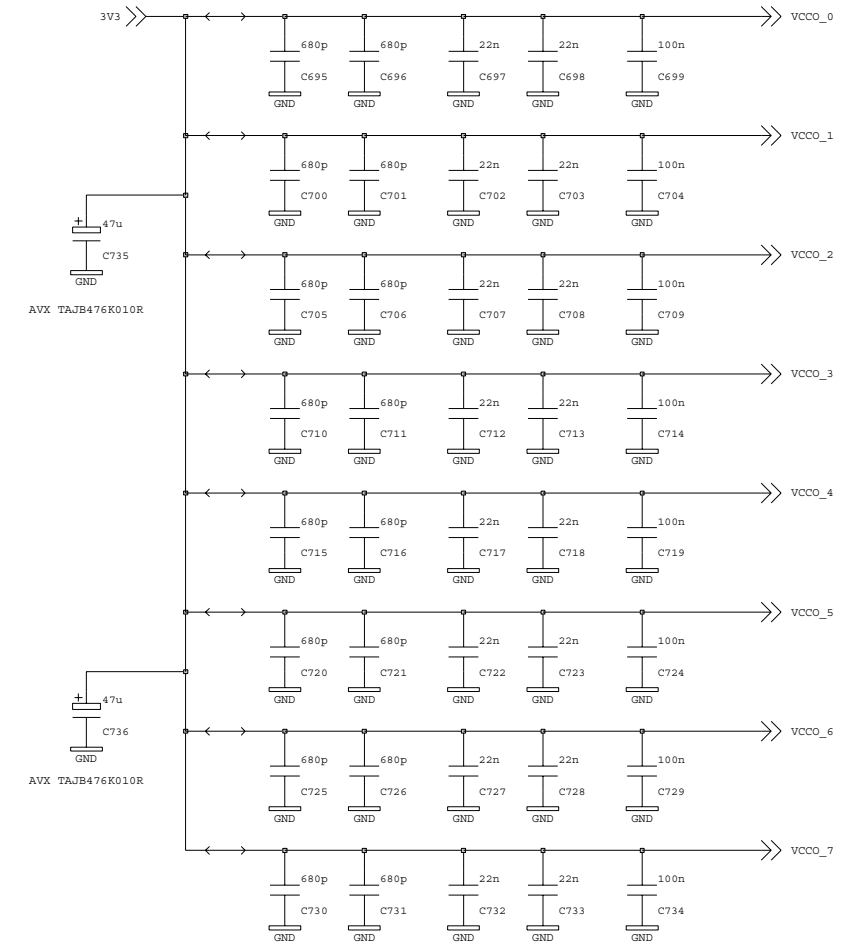
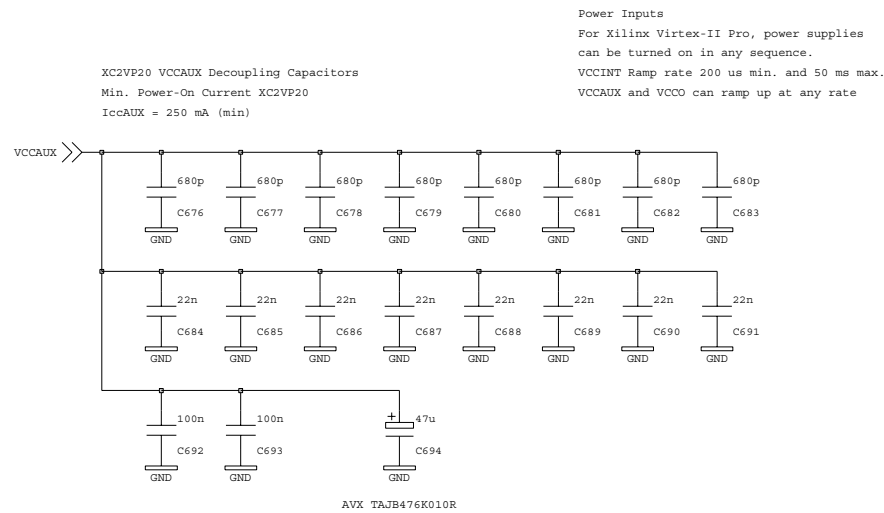
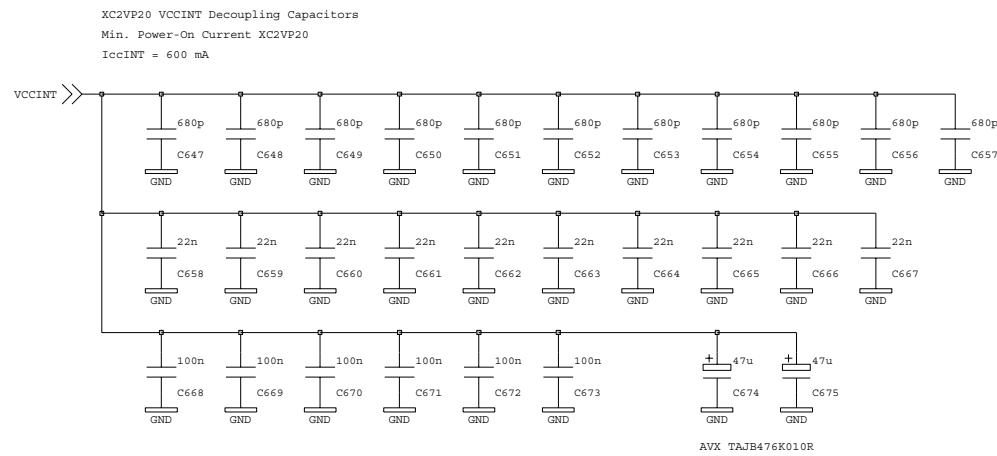
MROD-Out		Rev	V2	3
		Date	7 Feb 2006	
Sharc AB Link termination		Time	1:26:56 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	6	of 19

IC529
XC2VP20FF896

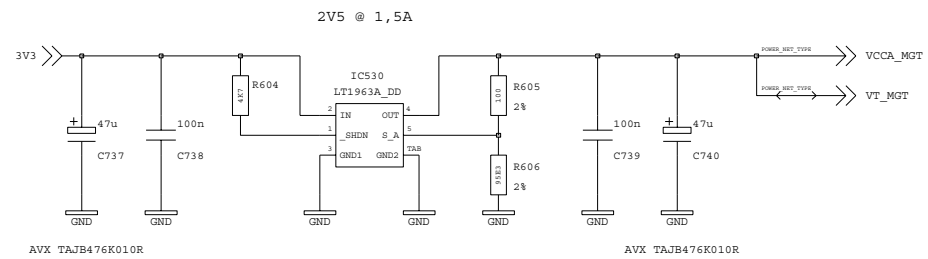
Pinout table for IC529 XC2VP20FF896. Columns 1-18 represent pin numbers. Rows A-J represent pin names and functions. The table lists various pins such as VCCAUX, VCCINT, VCCO, and various control signals like RST_n, WAKEUP_n, and memory-related signals like SDRAM_A[0:15].

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

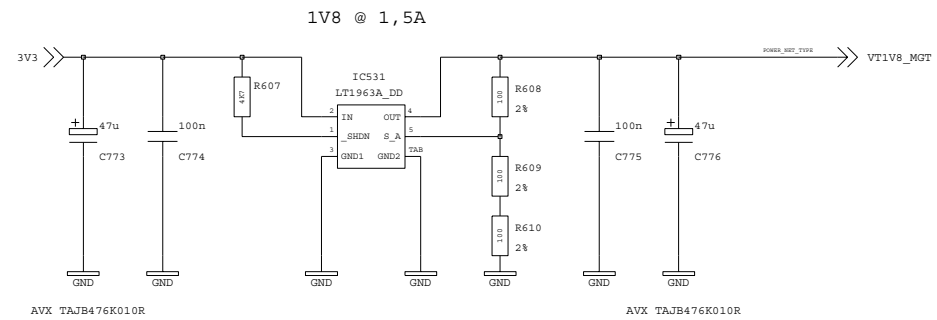
MROD-Out
Rev V2 4
Date 7 Feb 2006
Time 1:27:21 pm
Name tonvr
Proj: MROD-X Proj.No: 38405
Peter Jansweijer peterj@nikhef.nl
Size A3 4 1 4 A
Dim 420 x 297 mm
Page 7 of 19
NIKHEF
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND
© T-Nikhef Amsterdam



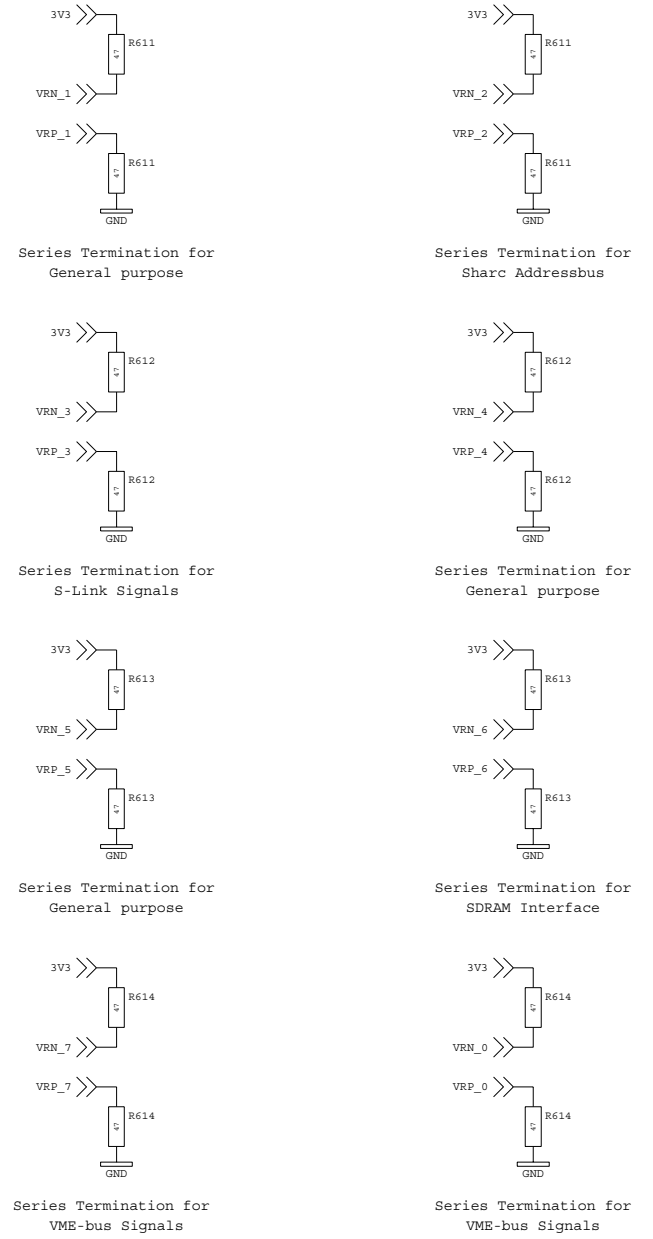
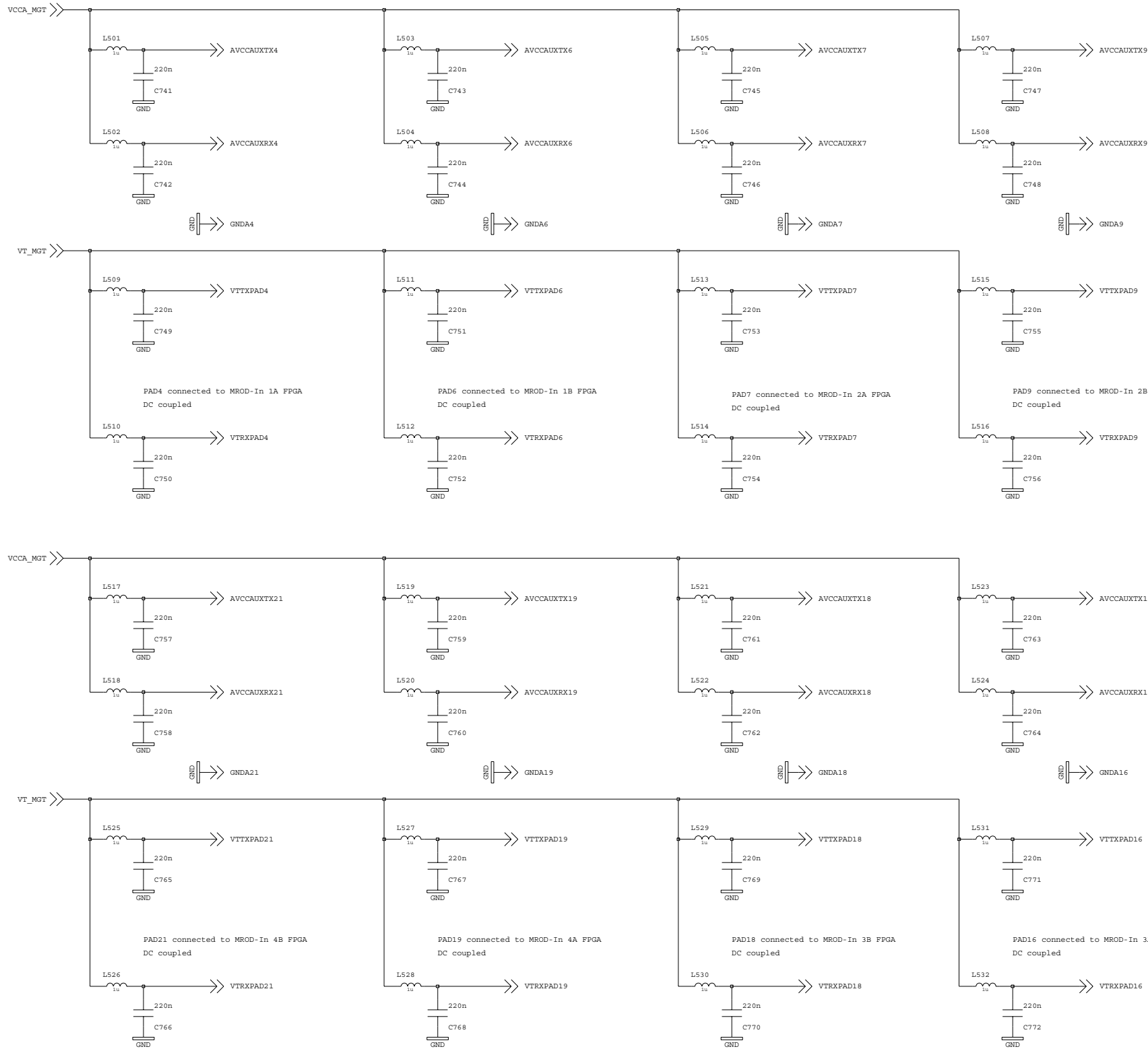
MROD-Out		Rev	V2	3
		Date	7 Feb 2006	
Output FPGA Power Supply Decoupling		Time	1:27:36 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF <small>© ET-Nikhef Amsterdam</small>		<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
Page		8	of 19	



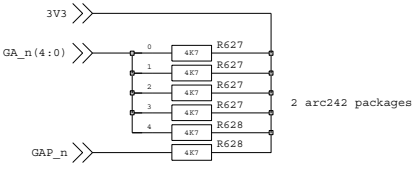
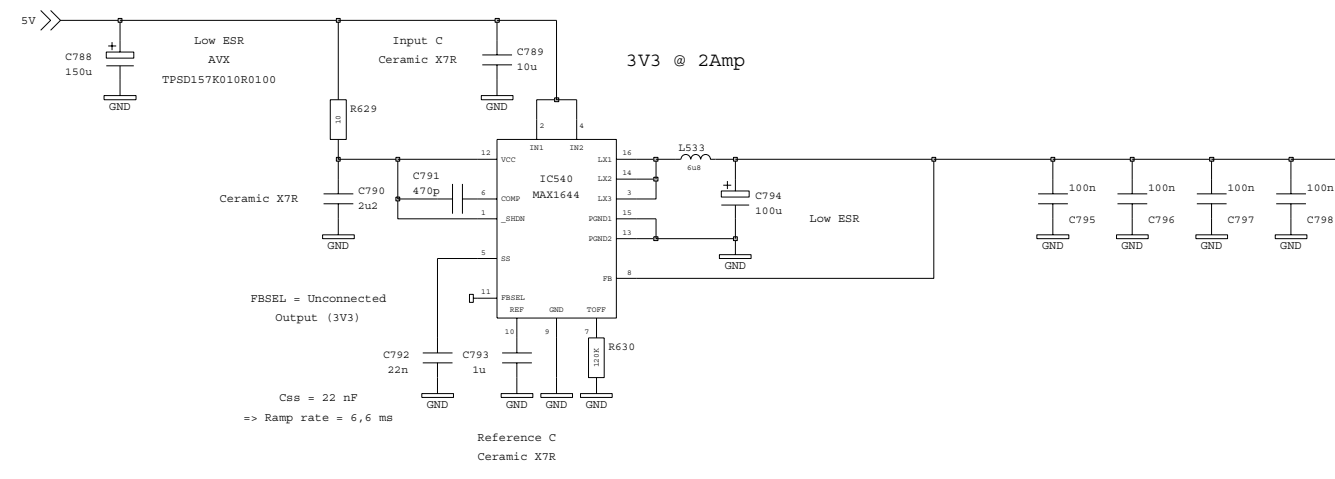
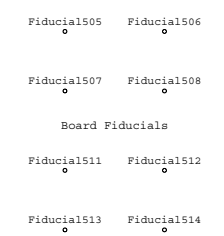
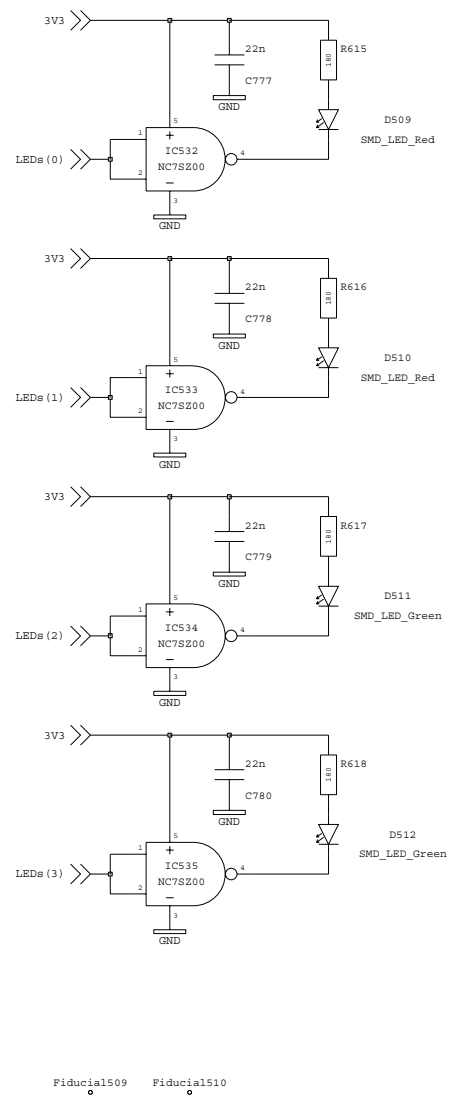
=> MGT Power (estimated 21 + 44 = 65 mA)
=> MGT Termination (estimated 2 * 11 mA = 22 mA)



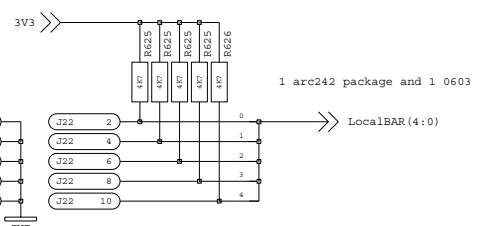
=> MGT RX Termination (estimated 8 * 11 mA = 88 mA)
Note: VT1V8_MGT is common to all MROD-Ins



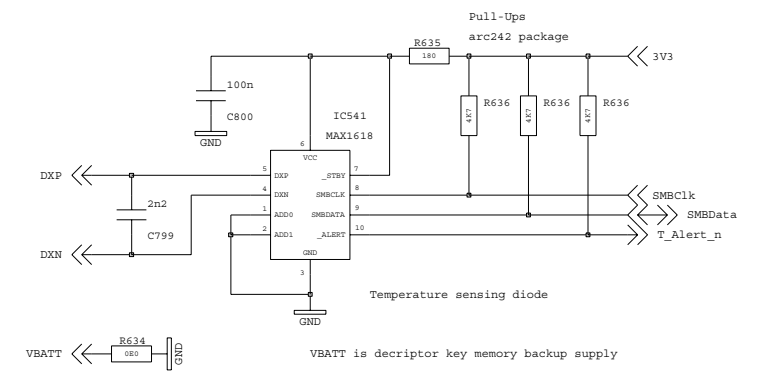
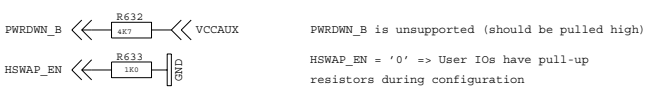
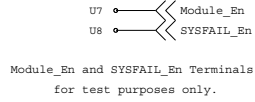
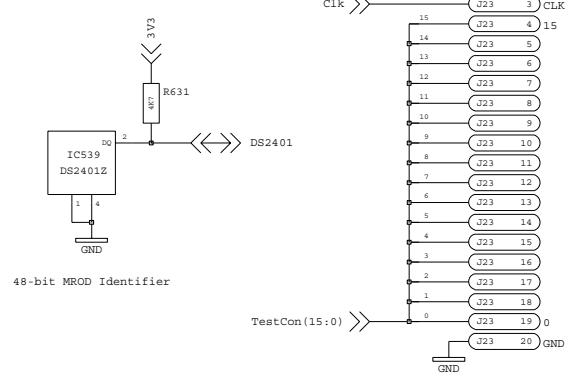
MROD-Out		Rev	V2	3
		Date	7 Feb 2006	
Outp FPGA MGT Pwr Decoupling, Termination		Time	1:29:37 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	9	of 19



GA_n(4:0) and GAP_n are either 'open' or 'ground' on the VME64x Back Plane.

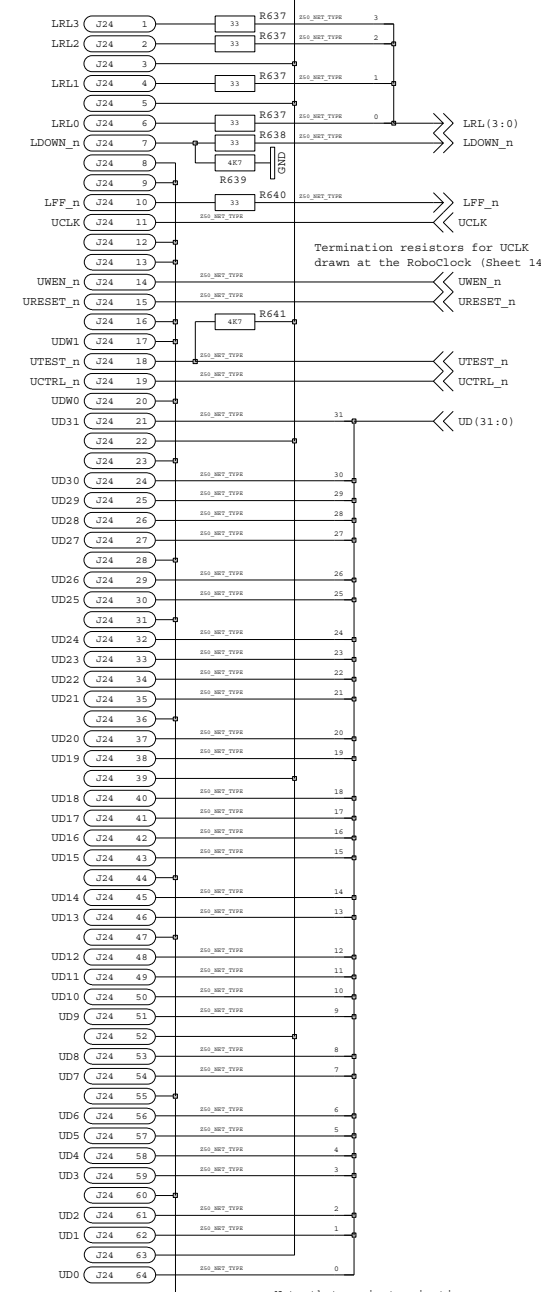


LocalBAR
These settings are used for BAR at power-up when this module is plugged into a non-VME64x backplane (without GA pins).



Other (Output) FPGA Control signals

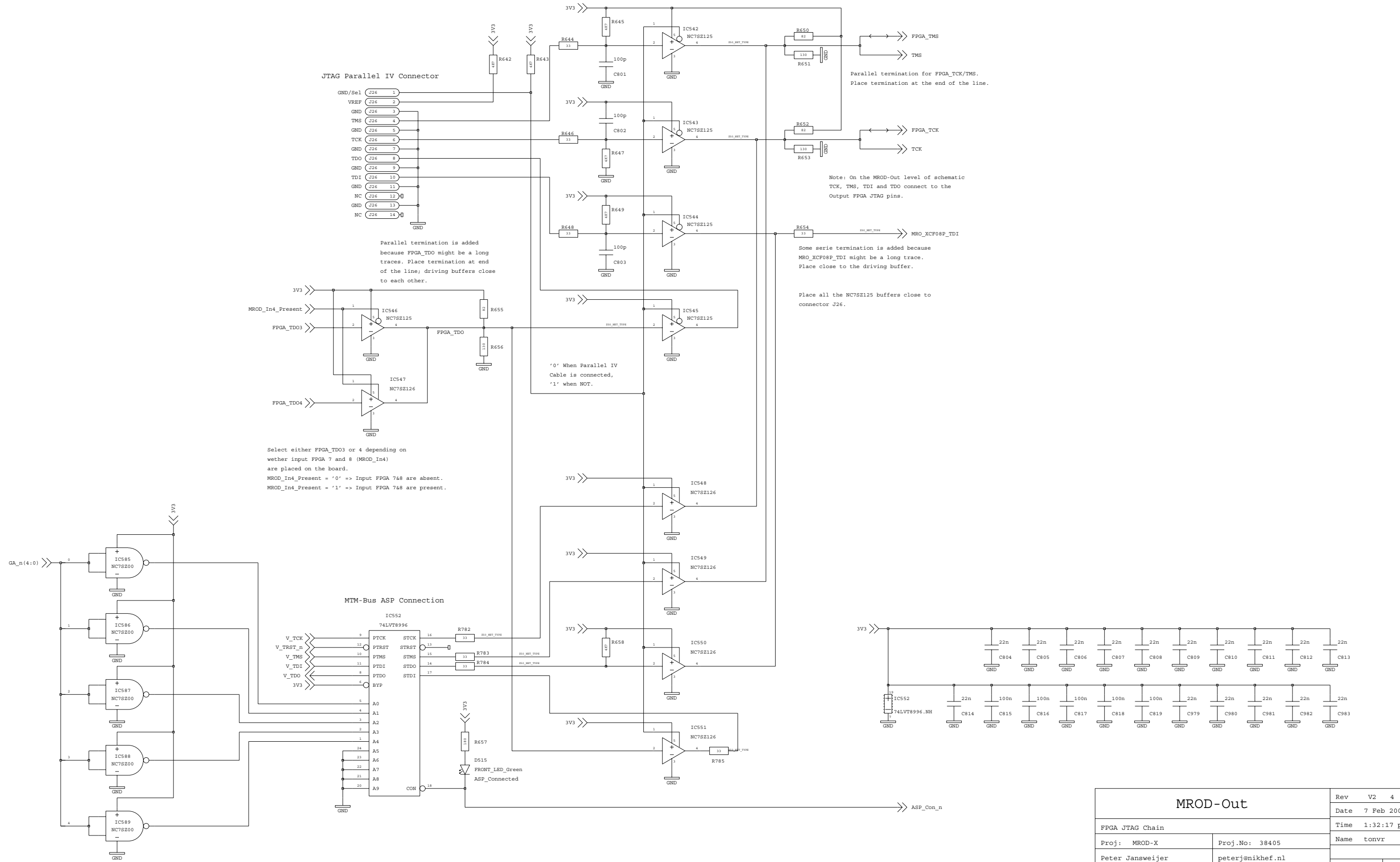
Note that the 33 ohm series termination resistors for the LRL, LDOWN_n and LFF_n signals should be placed near the S-Link connector.



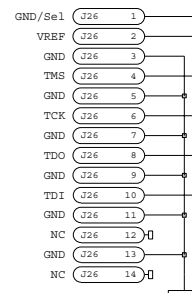
Note that series termination is incorporated by the Digital Contolled Impedance (DCI) feature of the Output FPGA.

S-LINK FEMB Connector Receptable

S-Link and Outp. FPGA Auxiliary Connections		Rev	V2	8
		Date	7 Feb 2006	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF NATIONAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	10 of 19	



JTAG Parallel IV Connector



Parallel termination is added because FPGA_TDO might be a long traces. Place termination at end of the line; driving buffers close to each other.

Parallel termination for FPGA_TCK/TMS. Place termination at the end of the line.

Note: On the MROD-Out level of schematic TCK, TMS, TDI and TDO connect to the Output FPGA JTAG pins.

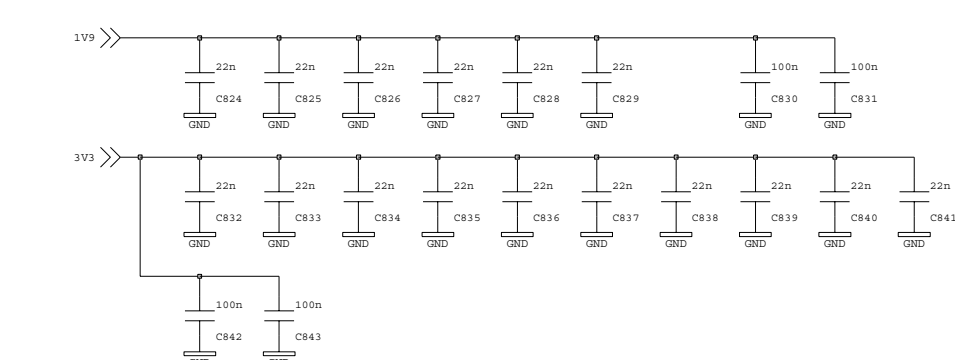
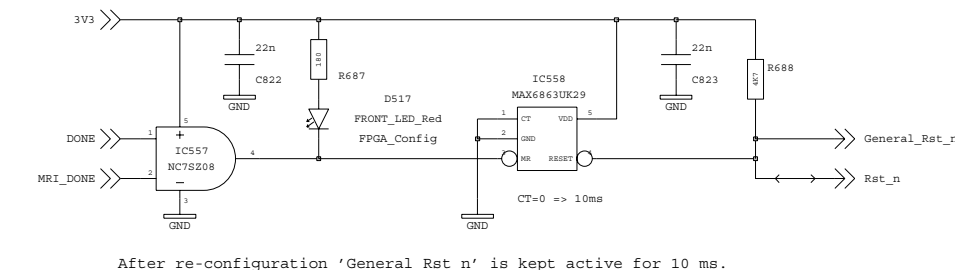
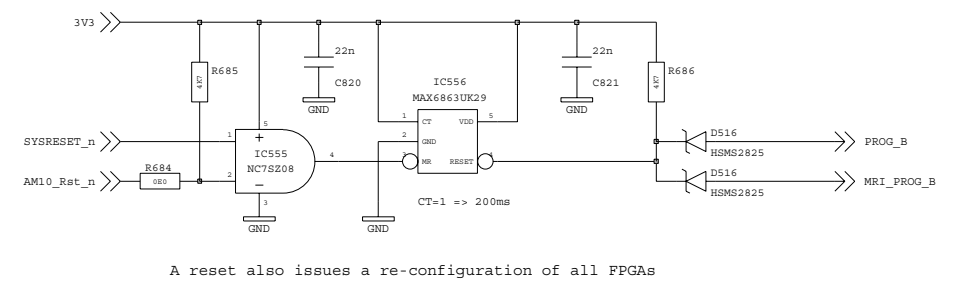
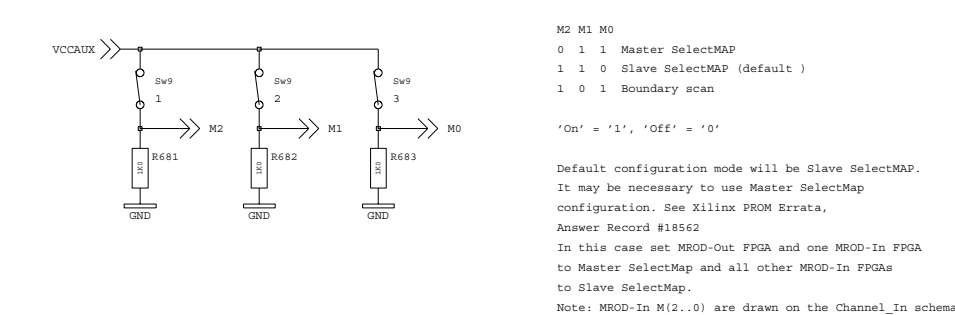
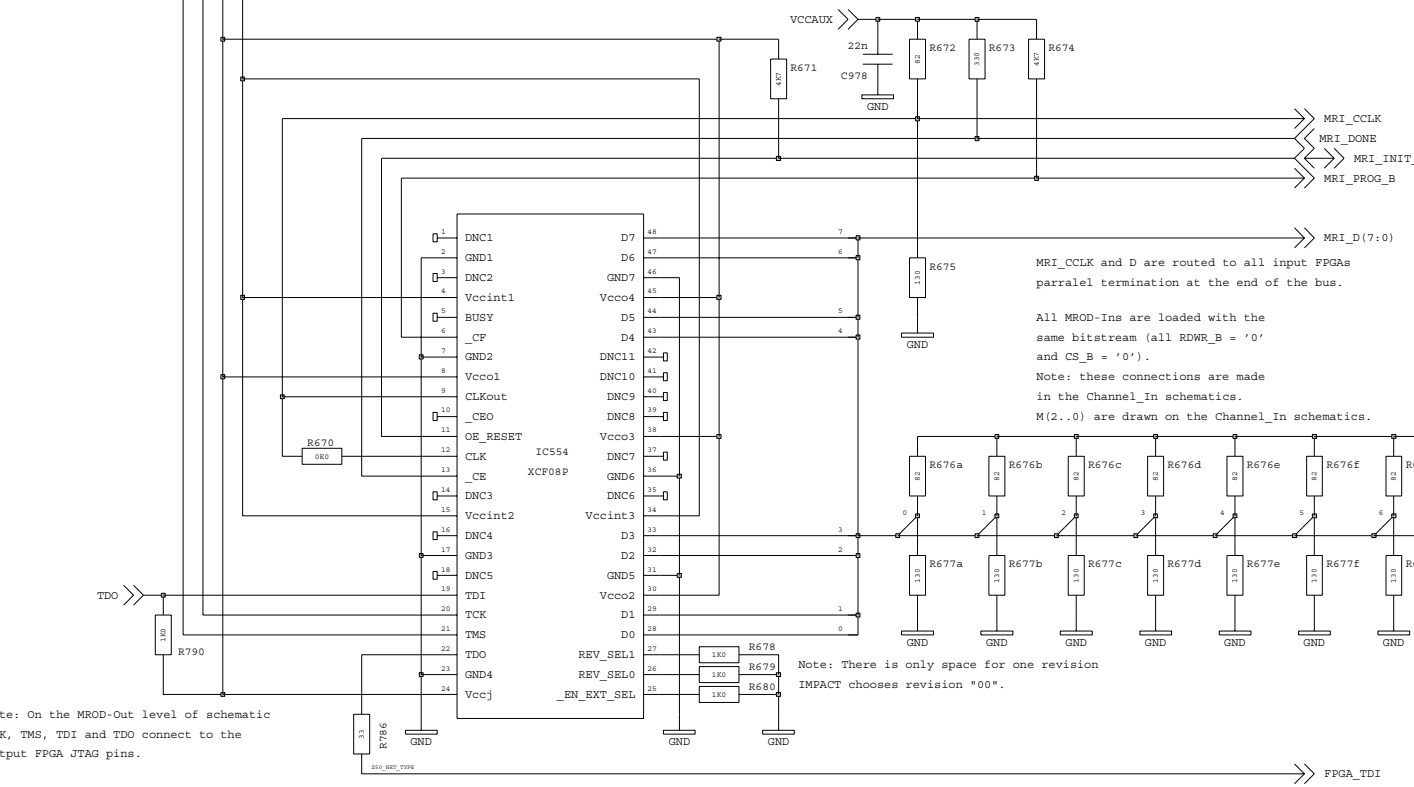
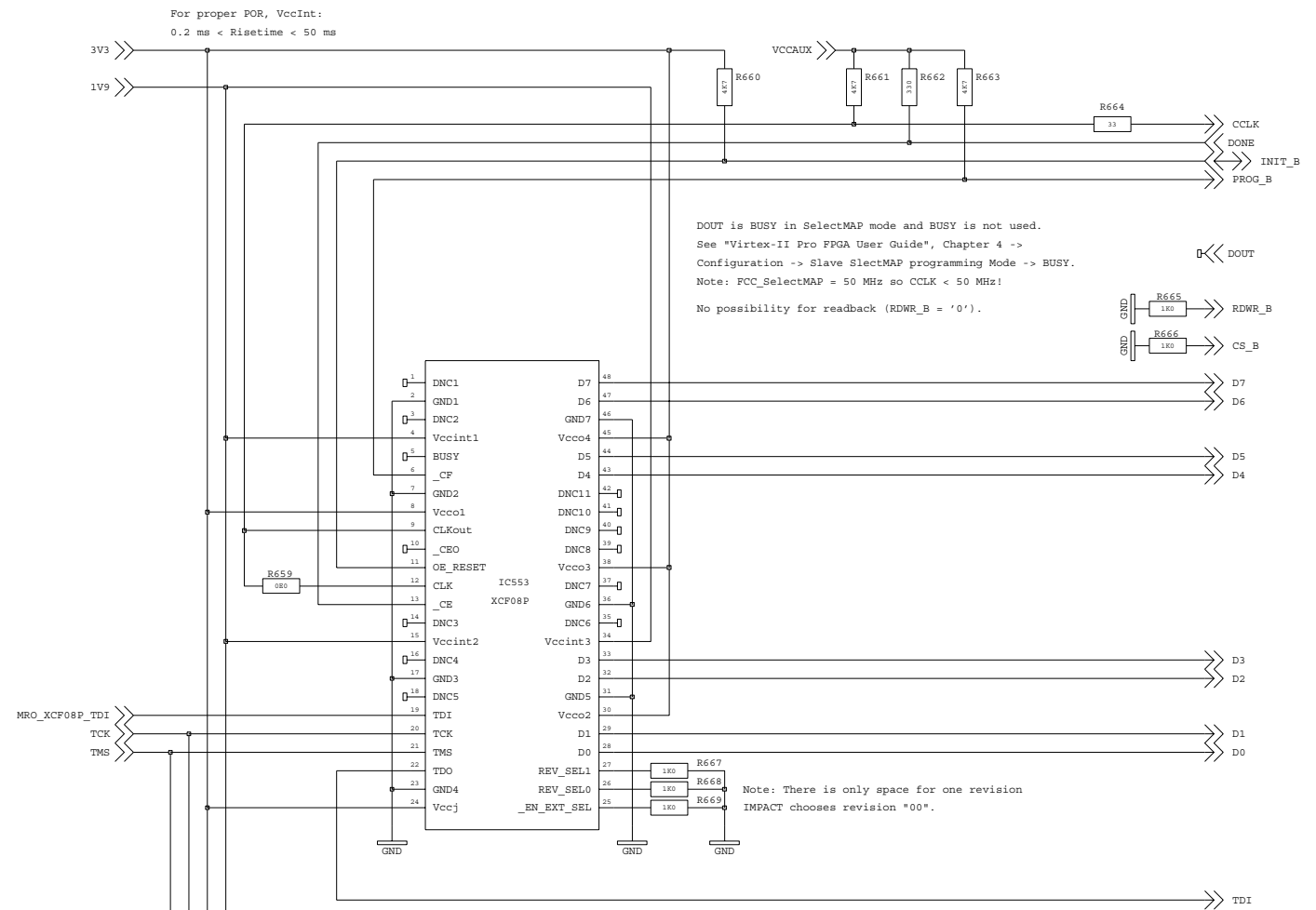
Some serie termination is added because MRO_XCF08P_TDI might be a long trace. Place close to the driving buffer.

Place all the NC7SZ125 buffers close to connector J26.

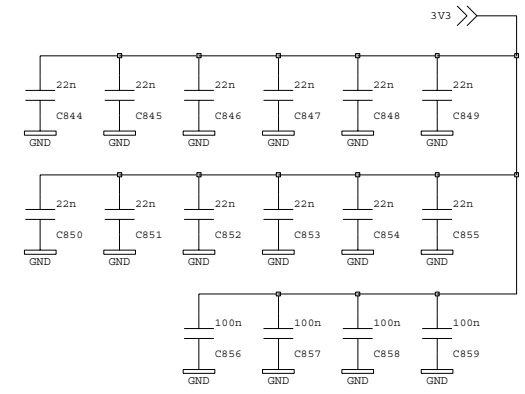
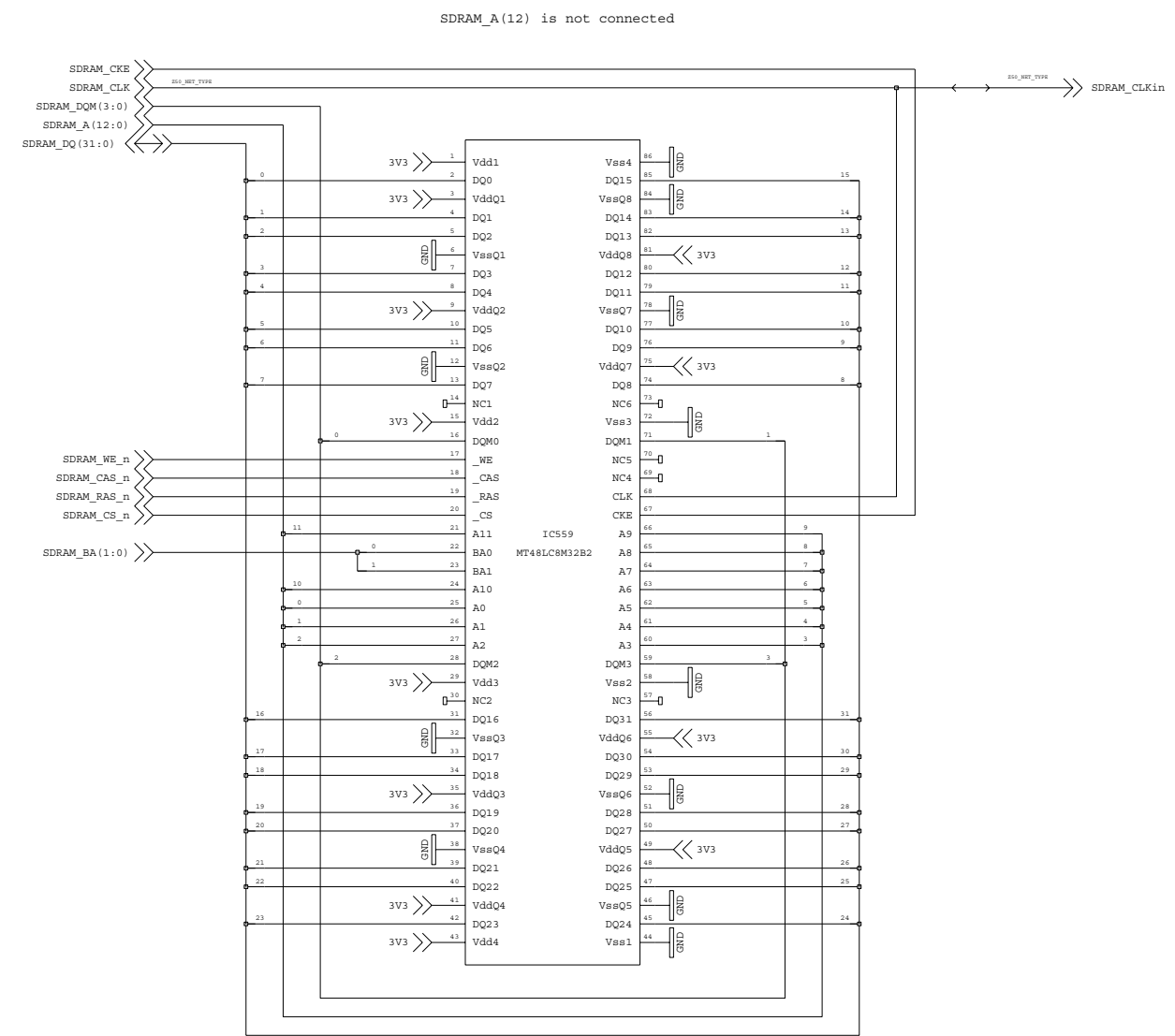
'0' When Parallel IV Cable is connected, '1' when NOT.

Select either FPGA_TDO3 or 4 depending on whether input FPGA 7 and 8 (MROD_In4) are placed on the board.
 MROD_In4_Present = '0' => Input FPGA 7&8 are absent.
 MROD_In4_Present = '1' => Input FPGA 7&8 are present.

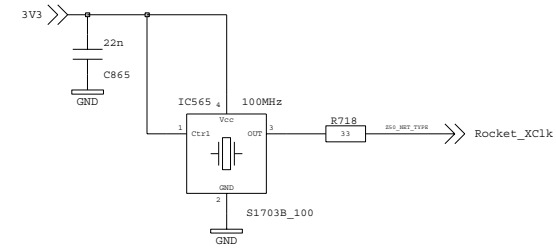
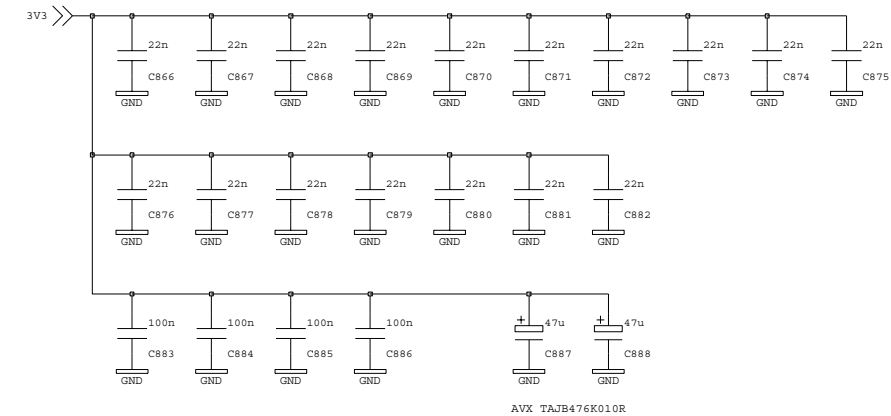
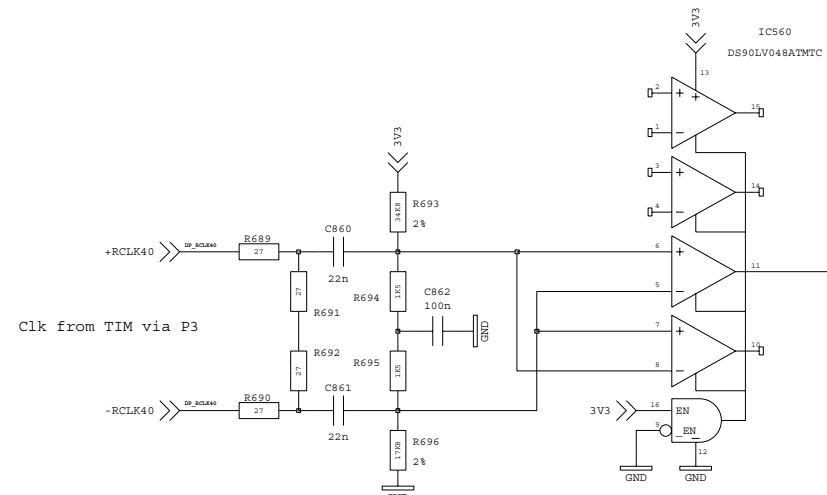
MROD-Out		Rev	V2	4
FPGA JTAG Chain		Date	7 Feb 2006	
Proj: MROD-X		Proj.No:	38405	
Peter Jansweijer		Name	tonvr	
peterj@nikhef.nl		Size	A3	4 1 4 A
NIKHEF		Dim	420 x 297 mm	
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Page	11 of 19	



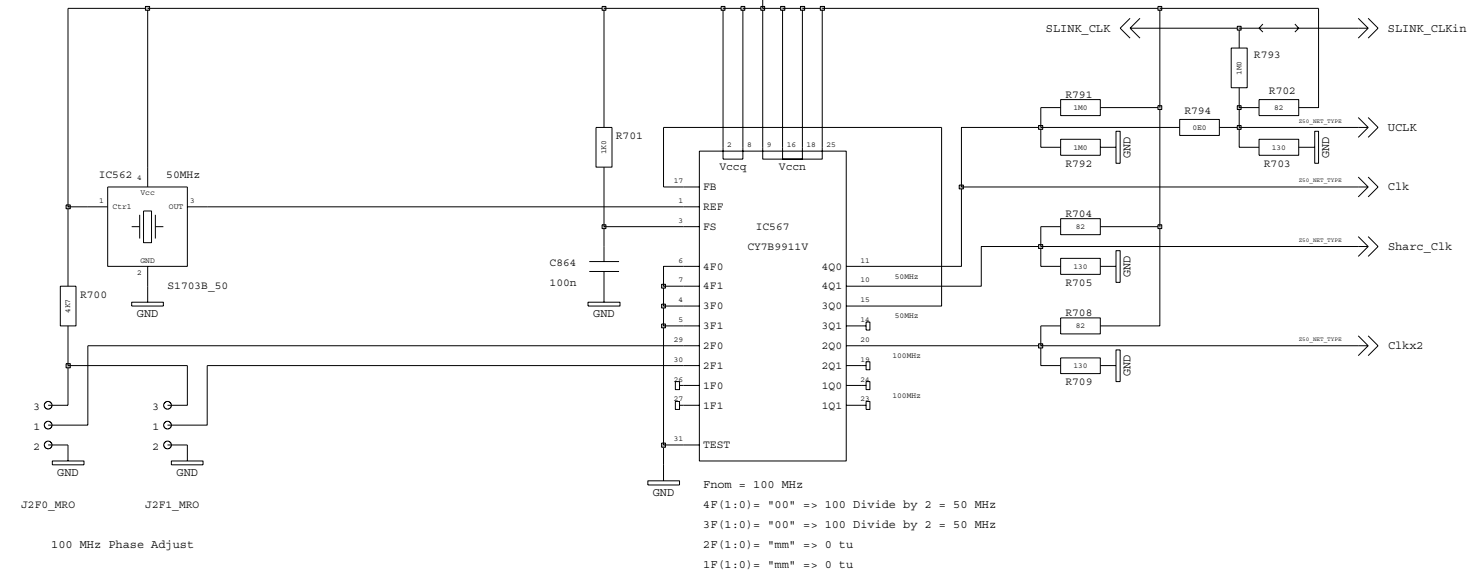
MROD-Out		Rev	V2	9
		Date	7 Feb 2006	
FPGA Configuration And Resets		Time	1:33:23 pm	
Proj: MROD-X	Proj.No: 38405	Name	Ton van Reen	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Dim	420 x 297 mm	
		Page	12 of 19	



MROD-Out		Rev	V2	3
		Date	7 Feb 2006	
SDRAM		Time	1:33:40 pm	
Proj:	MROD-X	Proj.No:	38405	
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		
		Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	13	of 19

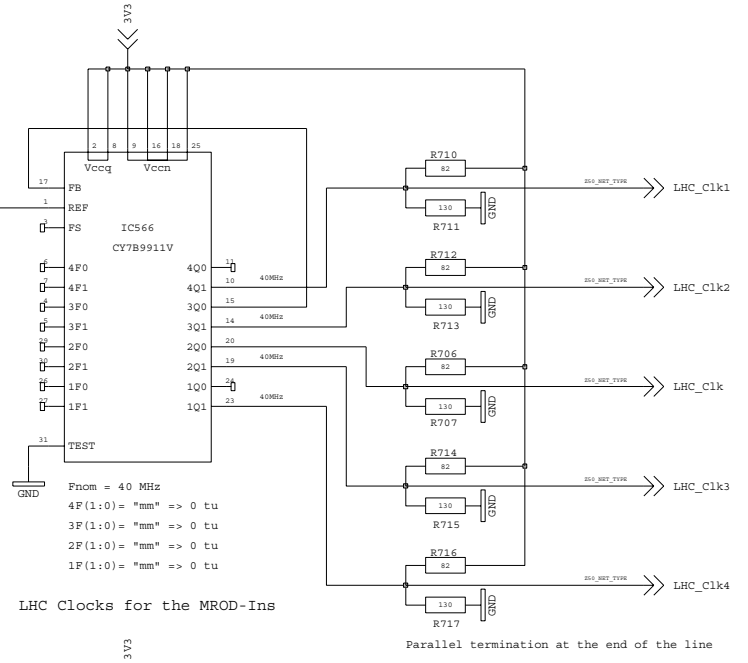


Rocket-IO Inter-FPGA Link Frequency
 100 MHz 16 bit = 50 MHz 32 bit
 = 200 MB/s



LHC Clocks for the MROD-Ins

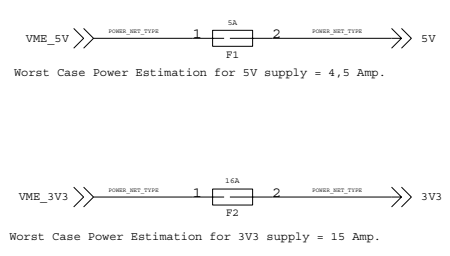
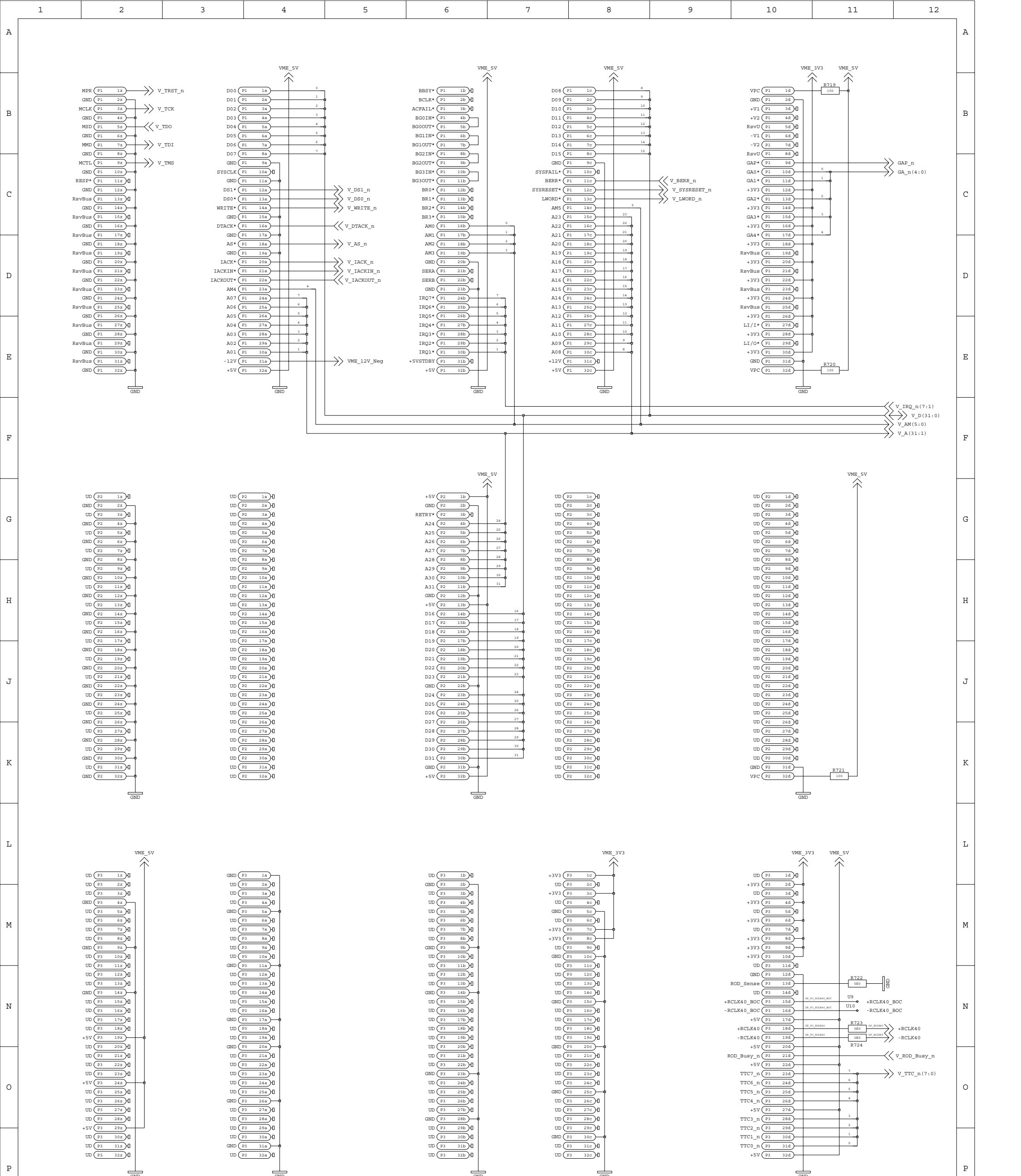
Clocks for the MROD-Out



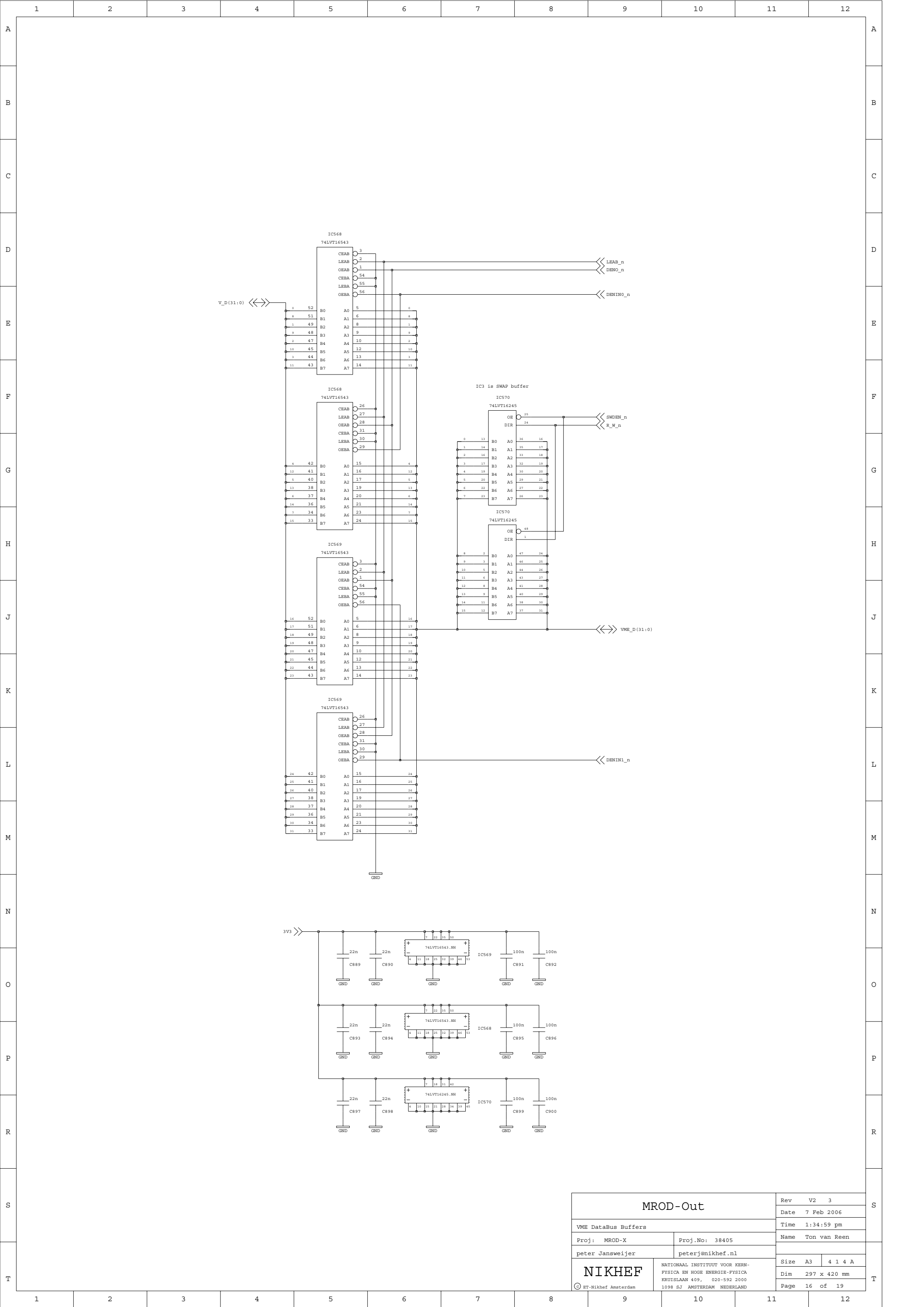
Parallel termination at the end of the line

Parallel termination at the end of the line

MROD-Out		Rev	V2	12	
		Date	7 Feb 2006		
Clocks		Time	1:34:07 pm		
Proj: MROD-X	Proj.No: 38405	Name	Ton van Reen		
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A	
NIKHEF © ET-Nikhef Amsterdam		NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Dim	420 x 297 mm
		Page	14 of 19		



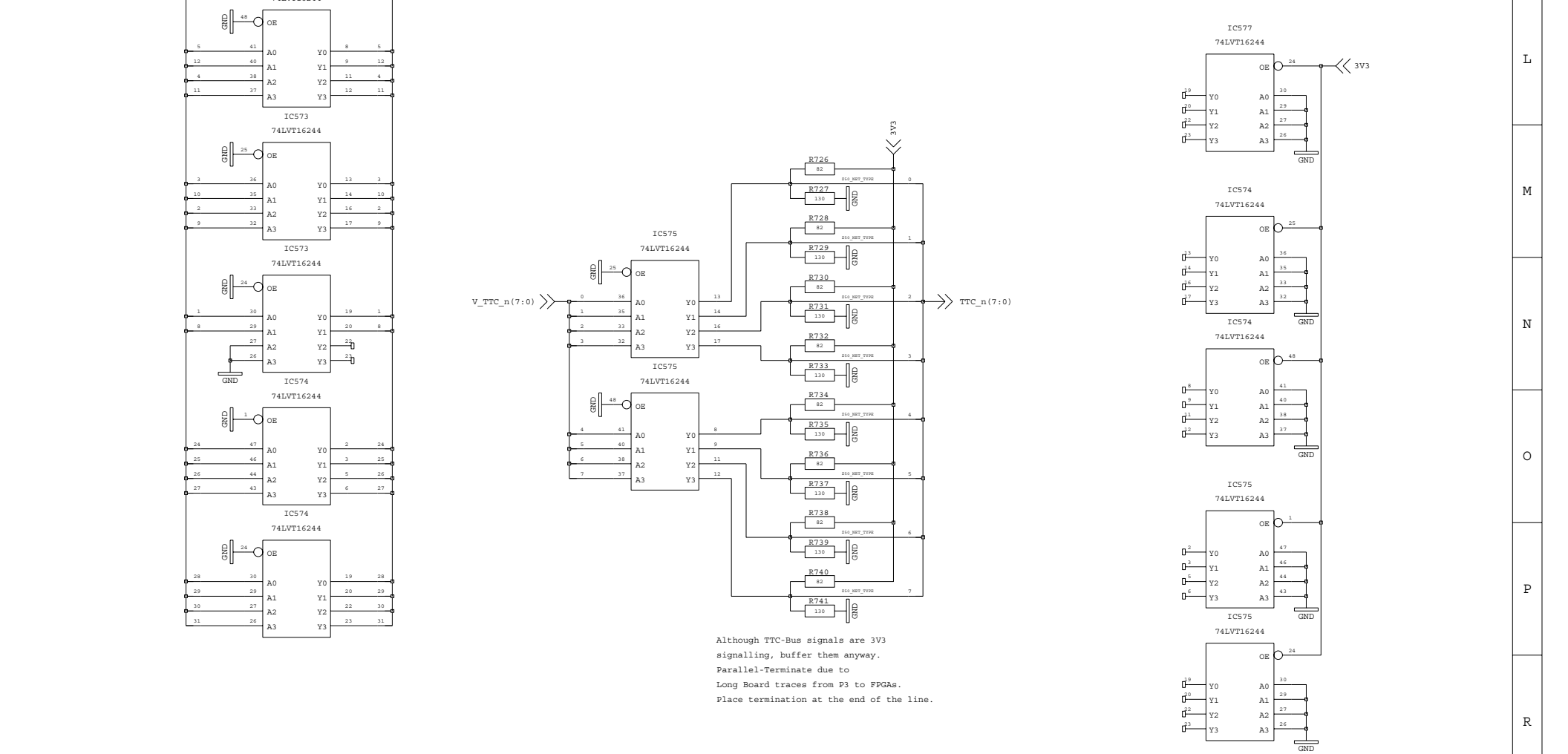
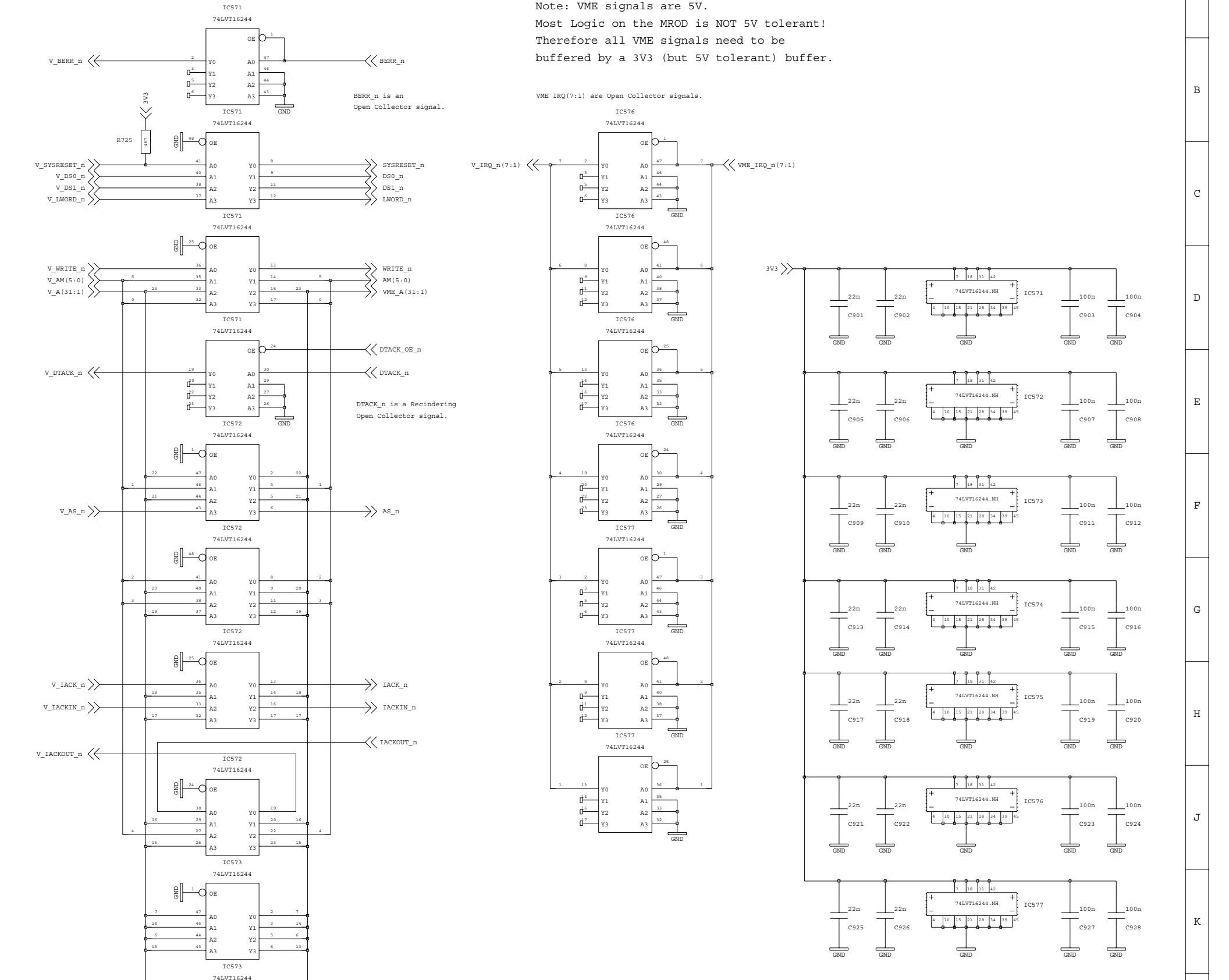
MROD-Out		Rev	V2 3
		Date	7 Feb 2006
VME Connectors		Time	1:34:31 pm
Proj:	MROD-X	Proj.No:	38405
Peter Janweijer		peterj@nikhef.nl	
NIKHEF NATIONAL INSTITUUT VOOR KERNFYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM, NEDERLAND		Size	A3 4 1 4 A
		Dim	297 x 420 mm
© ET-Nikhef Amsterdam		Page	15 of 19



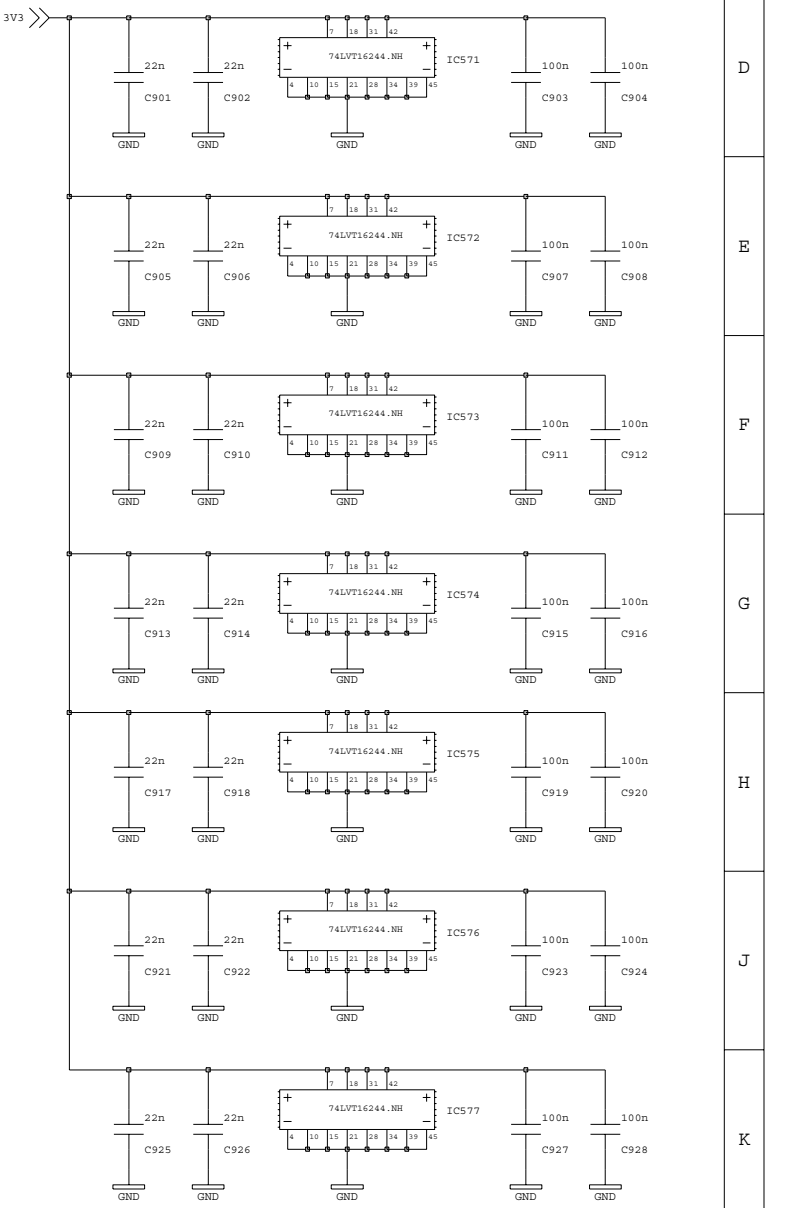
MROD-Out		Rev	V2	3
		Date	7 Feb 2006	
VME DataBus Buffers		Time	1:34:59 pm	
Proj:	MROD-X	Proj.No:	38405	
peter Jansweijer		peterj@nikhef.nl		
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>	Size	A3	4 1 4 A	
	Dim	297 x 420 mm		
	Page	16 of 19		

Note: VME signals are 5V.
Most Logic on the MROD is NOT 5V tolerant!
Therefore all VME signals need to be buffered by a 3V3 (but 5V tolerant) buffer.

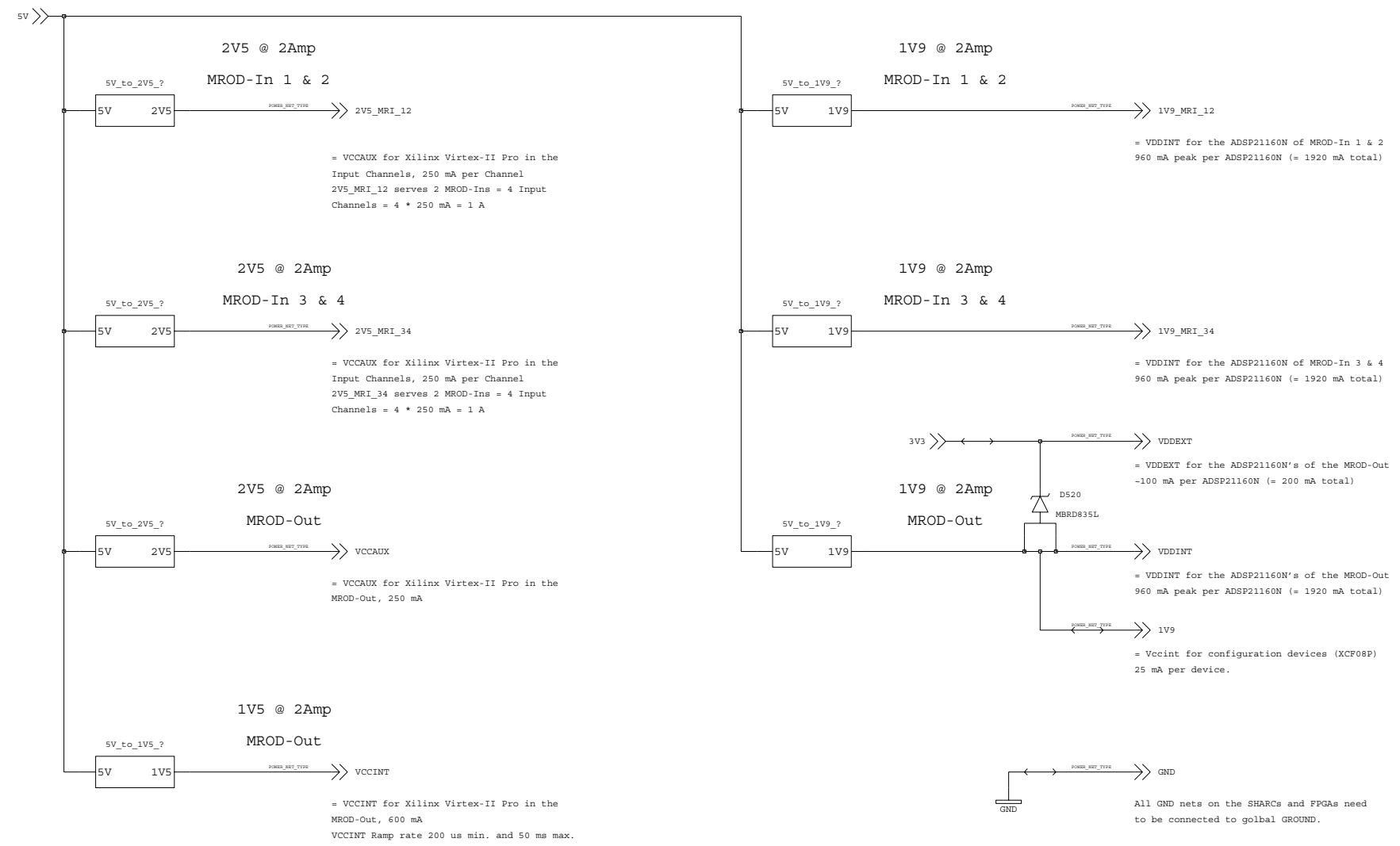
VME IRQ(7:1) are Open Collector signals.



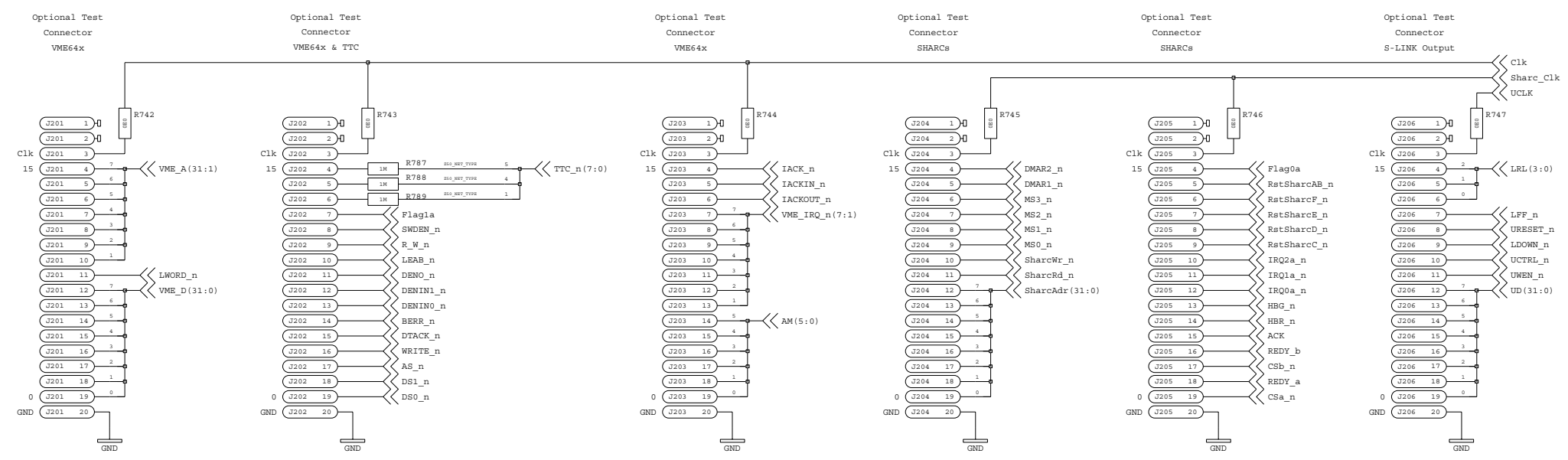
Although TTC-Bus signals are 3V3 signalling, buffer them anyway.
Parallel-Terminate due to Long Board traces from P3 to FPGAs.
Place termination at the end of the line.



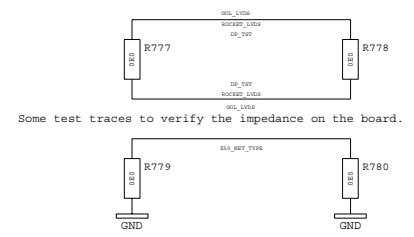
MROD-Out		Rev	V2	3
		Date	7 Feb 2006	
VME Bus Other Buffers		Time	1:35:25 pm	
Proj:	MROD-X	Proj.No:		
Peter Jansweijer		peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOOG ENERGIE-FYSICA		Size	A3 4 1 4 A
	KRUISLAAN 409, 020-592 2000		Dim	297 x 420 mm
© T-Nikhef Amsterdam		1098 SJ AMSTERDAM NEDERLAND		Page 17 of 19



MROD-Out		Rev	V2	3
Power Supplies		Date	7 Feb 2006	
Proj: MROD-X		Proj.No:	38405	
Peter Jansweijer		Name	tonvr	
peterj@nikhef.nl		Size	A3	4 1 4 A
NIKHEF <small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>		Dim	420 x 297 mm	
		Page	18 of 19	

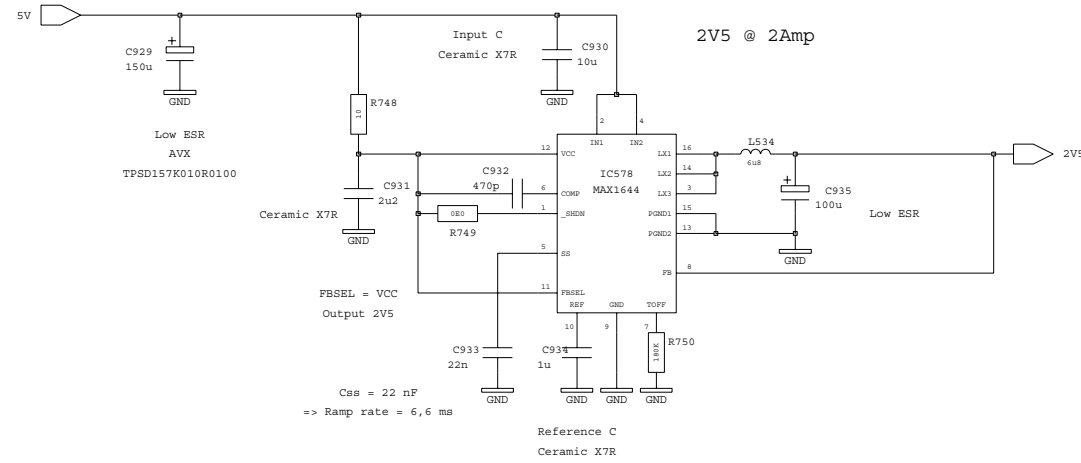


The 0 ohm resistors in the clock lines can be removed when the test connector is not used. This avoids long stubs on the clock lines. Note that the resistors should be placed near the clock source!

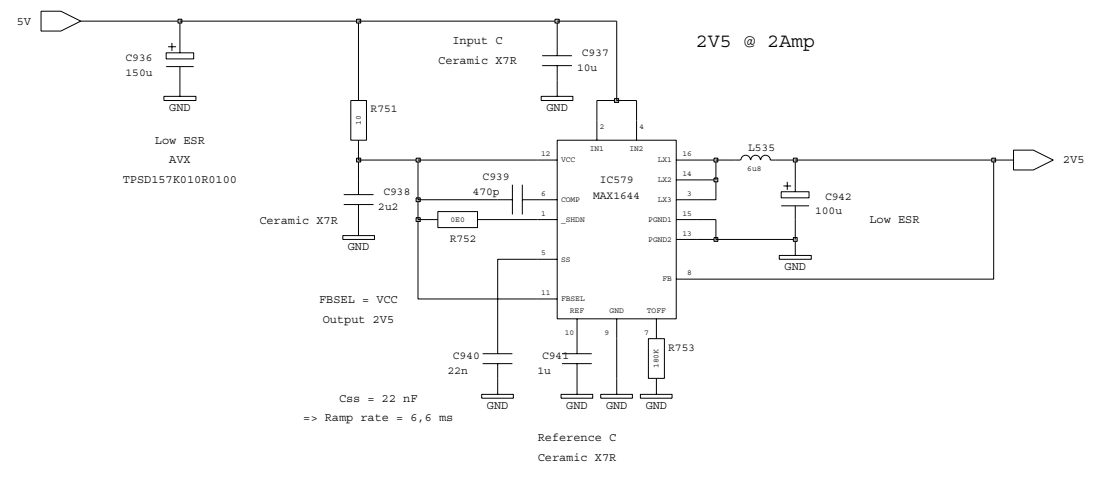


Some test traces to verify the impedance on the board.

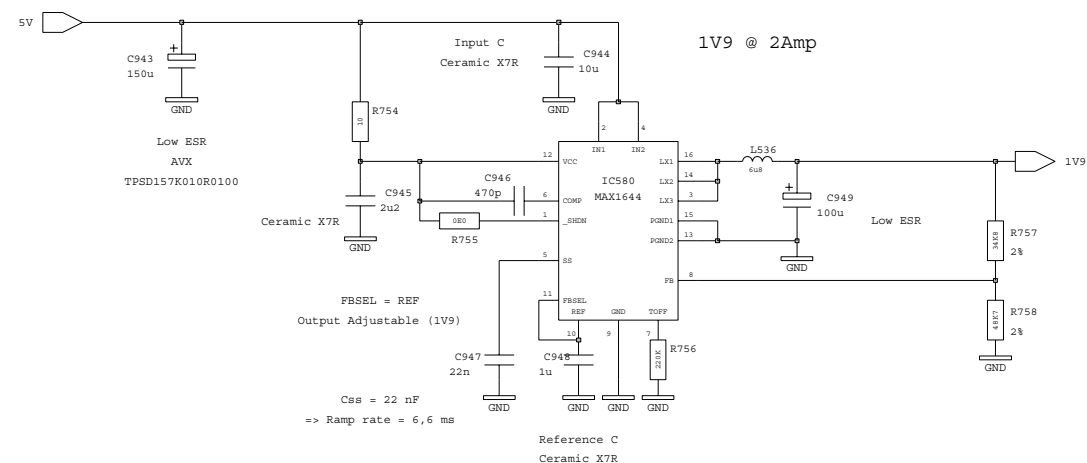
MROD-Out		Rev	V2	4
		Date	7 Feb 2006	
Test connectors		Time	1:36:13 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF © ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim	420 x 297 mm	
		Page	19 of 19	



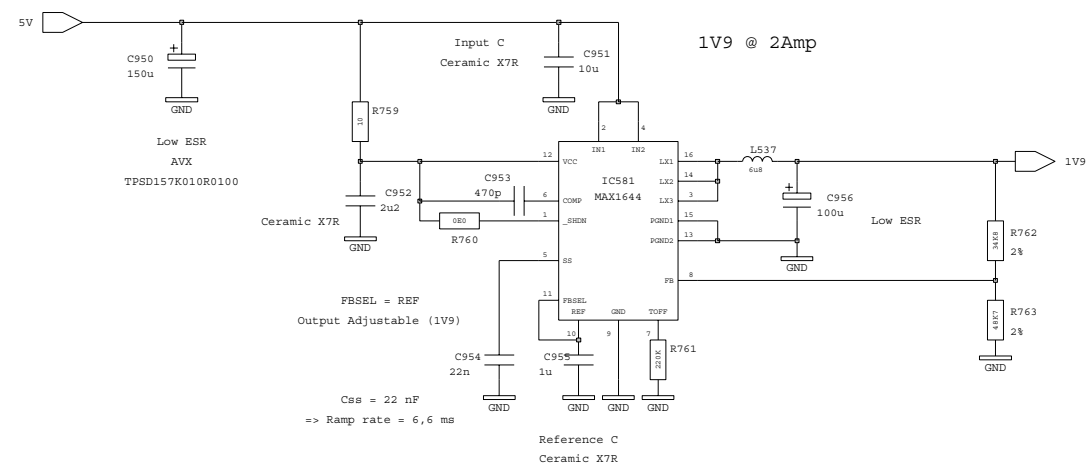
Power Supply		Rev	V2	2
		Date	7 Feb 2006	
5V -> 2V5 @ 2A		Time	1:36:58 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF	NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim	420 x 297 mm	
© ET-Nikhef Amsterdam		Page	1	of 1



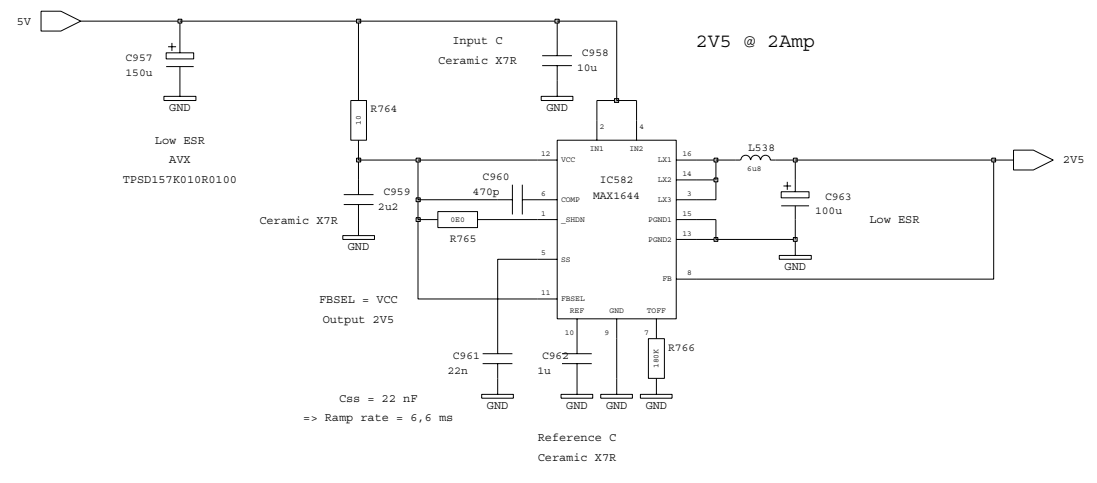
Power Supply		Rev	V2	2
		Date	7 Feb 2006	
5V -> 2V5 @ 2A		Time	1:36:58 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>© ET-Nikhef Amsterdam</small>	<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>	Dim	420 x 297 mm	
		Page	1	of



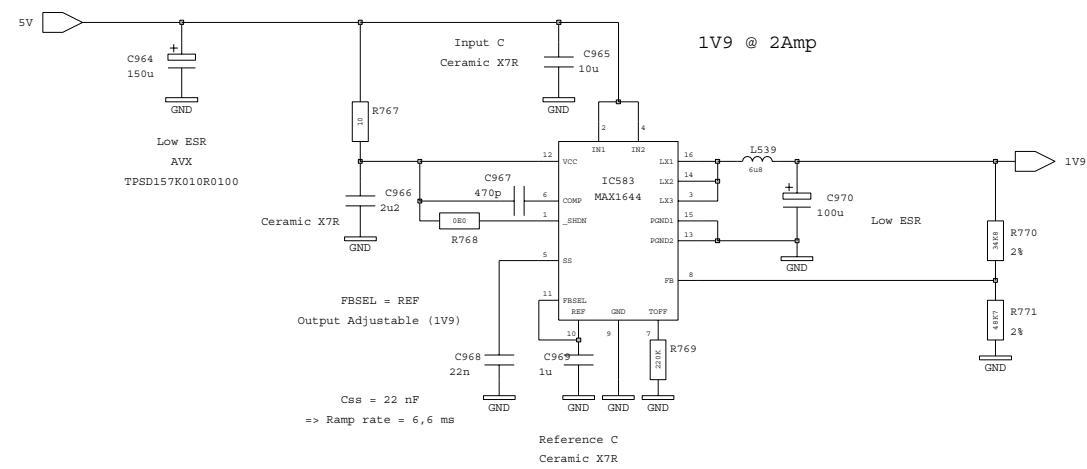
Power Supply		Rev	V2	2
		Date	7 Feb 2006	
5V -> 1V9 @ 2A		Time	1:39:18 pm	
Proj: MROD_X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>© ET-Nikhef Amsterdam</small>	<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>	Dim	420 x 297 mm	
		Page	1	of



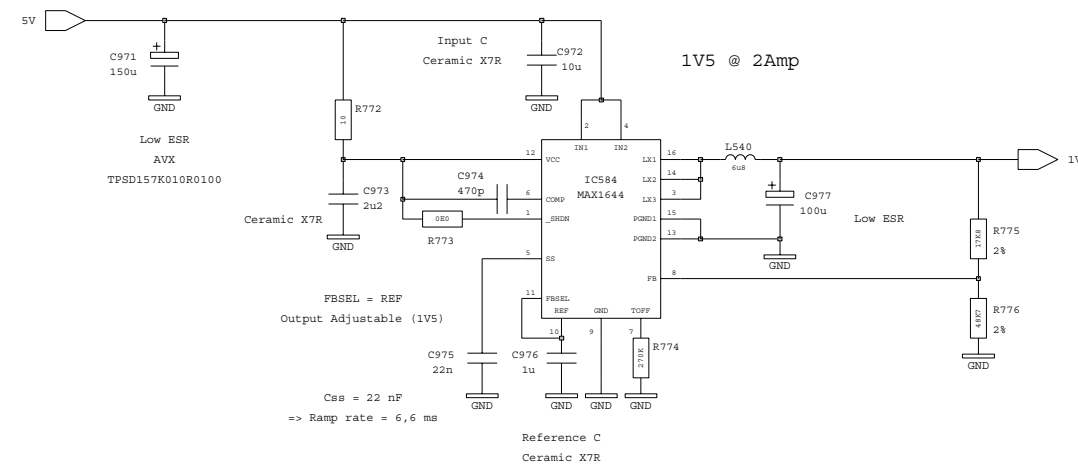
Power Supply		Rev	V2	2
		Date	7 Feb 2006	
5V -> 1V9 @ 2A		Time	1:39:18 pm	
Proj: MROD_X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>© ET-Nikhef Amsterdam</small>	<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>	Dim	420 x 297 mm	
		Page	1 of 1	



Power Supply		Rev	V2	2
		Date	7 Feb 2006	
5V -> 2V5 @ 2A		Time	1:36:58 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>© ET-Nikhef Amsterdam</small>	<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>	Dim	420 x 297 mm	
		Page	1	of



Power Supply		Rev	V2	2
		Date	7 Feb 2006	
5V -> 1V9 @ 2A		Time	1:39:18 pm	
Proj: MROD_X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl			
NIKHEF <small>© ET-Nikhef Amsterdam</small>	<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>	Size	A3	4 1 4 A
		Dim	420 x 297 mm	
		Page	1	of 1



Power Supply		Rev	V2	2
		Date	7 Feb 2006	
5V -> 1V5 @ 2A		Time	1:38:24 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>© ET-Nikhef Amsterdam</small>	<small>NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>	Dim	420 x 297 mm	
		Page	1 of 1	