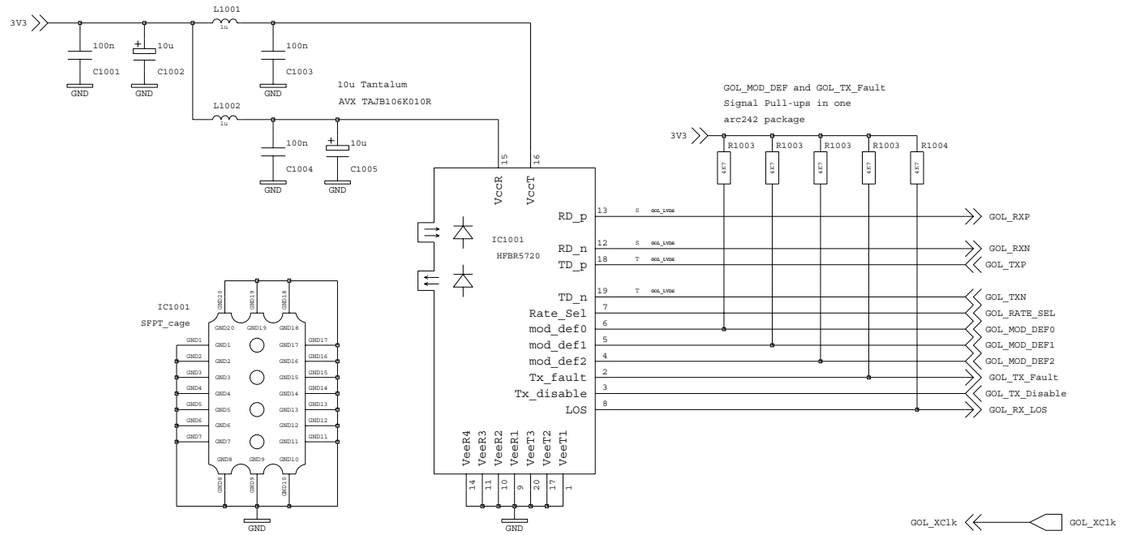
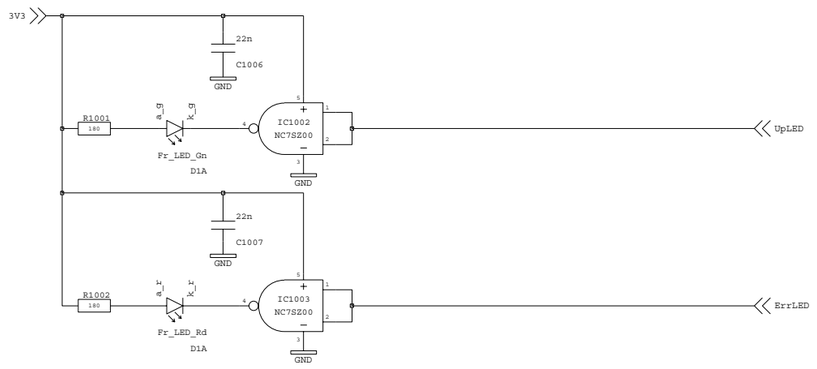




channel_in		Rev V2 2	
		Date 7 Feb 2006	
GOL Input		Time 1:50:33 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
ET-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 1 of 6	

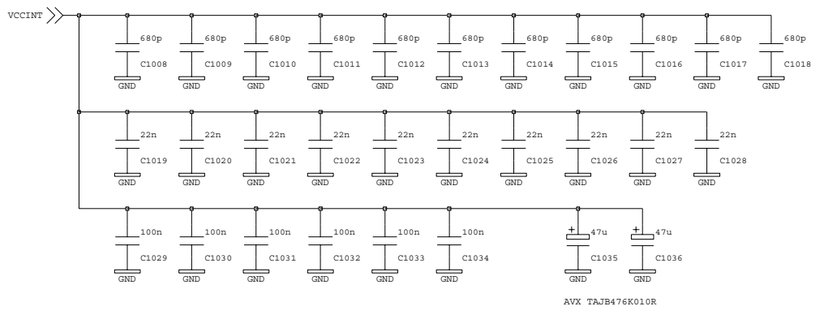
IC1004
XC2VP7FF896

	A2 VCCAUX	A3 VRP_2	A4	A5	A6	A7	A8	A9 GND	A10	A11	A12	A13	A14	A15 VCCAUX	A16 VCCAUX	A17 GOL_LVDS GOL_LVDS T DP_GOL_RX1A	A18 GOL_LVDS GOL_LVDS T DP_GOL_RX1A	A19 GOL_LVDS GOL_LVDS S DP_GOL_TX1A	A20 GOL_LVDS GOL_LVDS S DP_GOL_TX1A	A21	A22 GND	A23 LEDs(0)	A24	A25	A26	A27	A28 VRP_7	A29 VCCAUX	
B1 VCCAUX	B2 GND	B3 VRN_2	B4 AVCCAUXRX9	B5 VTRXPAD9	B6 AVCCAUXTX9	B7 VTTXPAD9	B8	B9	B10	B11 AVCCAUXRX7	B12 VTRXPAD7	B13 AVCCAUXTX7	B14 VTTXPAD7	B15	B16 GOL_XClk	B17 AVCCAUXRX6	B18 VTRXPAD6	B19 AVCCAUXTX6	B20 VTTXPAD6	B21	B22	B23 LEDs(1)	B24 AVCCAUXRX4	B25 VTRXPAD4	B26 AVCCAUXTX4	B27 VTTXPAD4	B28 VRN_7	B29 GND	B30 VCCAUX
C1	C2	C3 GND	C4	C5	C6 GNDA9	C7	C8	C9	C10	C11	C12 GNDA7	C13	C14 GND	C15	C16	C17 GND	C18 UpLED	C19 GNDA6	C20	C21	C22	C23 LEDs(2)	C24 LEDs(3)	C25 GNDA4	C26 BufA(6)	C27 BufA(7)	C28 GND	C29 BufCE_n	C30 BufA(19)
D1	D2	D3 GND	D4	D5	D6	D7	D8	D9 GND	D10	D11	D12 GND	D13	D14	D15	D16 GOL_RX_LOS	D17 GOL_TX_Disable	D18 ErrLED	D19 GND	D20 GOL_MOD_DEF1	D21 GOL_MOD_DEF0	D22 GND	D23 ChaID(1)	D24 ChaID(0)	D25 DXN	D26 BufD(16)	D27 GND	D28 BufD(33)	D29	D30
E1	E2	E3	E4 GND	E5	E6 VRN_1	E7 VRP_1	E8	E9	E10	E11	E12	E13	E14	E15	E16	R17 GOL_TX_Fault	E18	E19	E20 GOL_MOD_DEF2	E21 GOL_RATE_SEL	E22	E23 ChaID(2)	E24 VRN_0	E25 VRP_0	E26 GND	E27	E28	E29	E30
F1	F2	F3	F4	F5 TDO	F6 GND	F7	F8	F9	F10	F11	F12	F13 GND	F14	F15	F16	F17	F18 GND	F19	F20	F21 TestCon(1)	F22 TestCon(0)	F23	F24	F25 GND	F26 TDI	F27	F28	F29	F30
G1	G2	G3	G4	G5	G6	G7 TCK	G8	G9	G10	G11	G12	G13	G14	G15	G16 Rst_n	G17	G18	G19 TestCon(6)	G20 TestCon(5)	G21 TestCon(4)	G22 TestCon(3)	G23 TestCon(2)	G24 PROG_B	G25 BufD(18)	G26 BufD(17)	G27	G28	G29	G30
H1 GND	H2	H3	H4	H5	H6	H7 VBATT	H8 TMS	H9	H10	H11	H12 TestCon(15)	H13	H14	H15	H16	H17	H18	H19 TestCon(7)	H20 T_Alert_n	H21 SMBData	H22 SMBClk	H23 HSWAP_EN	H24 DXP	H25	H26	H27	H28	H29 BufD(19)	H30 GND
J1	J2	J3	J4	J5	J6	J7	J8 TestCon(14)	J9 VCCO_2	J10 VCCO_1	J11 VCCO_1	J12 VCCO_1	J13 VCCO_1	J14	J15	J16	J17	J18 VCCO_0	J19 VCCO_0	J20 VCCO_0	J21 VCCO_0	J22 VCCO_7	J23 BufD(25)	J24 BufD(24)	J25	J26	J27 BufD(23)	J28 BufD(22)	J29 BufD(21)	J30 BufD(20)
K1	K2	K3	K4	K5	K6	K7	K8	K9 VCCO_2	K10 VCCO_1	K11 VCCO_1	K12 VCCO_1	K13 VCCO_1	K14 VCCO_1	K15 VCCO_1	K16 VCCO_0	K17 VCCO_0	K18 VCCO_0	K19 VCCO_0	K20 VCCO_0	K21 VCCO_0	K22 VCCO_7	K23	K24	K25 BufD(31)	K26 BufD(30)	K27 BufD(29)	K28 BufD(28)	K29 BufD(27)	K30 BufD(26)
L1	L2	L3 GND	L4	L5	L6 GND	L7	L8	L9 VCCO_2	L10 VCCO_2	L11 GND	L12 VCCINT	L13 VCCINT	L14 VCCINT	L15 VCCINT	L16 VCCINT	L17 VCCINT	L18 VCCINT	L19 VCCINT	L20 GND	L21 VCCO_7	L22 VCCO_7	L23	L24	L25 GND	L26 BufA(3)	L27 BufA(4)	L28 GND	L29 BufA(5)	L30 BufD(32)
M1	M2	M3	M4	M5	M6	M7	M8	M9 VCCO_2	M10 VCCO_2	M11 VCCINT	M12 GND	M13 GND	M14 GND	M15 GND	M16 GND	M17 GND	M18 GND	M19 GND	M20 VCCINT	M21 VCCO_7	M22 VCCO_7	M23 BufA(14)	M24 BufA(13)	M25 BufA(12)	M26 BufA(11)	M27 BufA(10)	M28 BufA(0)	M29 BufA(1)	M30 BufA(2)
N1	N2	N3	N4	N5	N6	N7	N8	N9 VCCO_2	N10 VCCO_2	N11 VCCINT	N12 GND	N13 GND	N14 GND	N15 GND	N16 GND	N17 GND	N18 GND	N19 GND	N20 VCCINT	N21 VCCO_7	N22 VCCO_7	N23 BufD(4)	N24 BufD(3)	N25 BufD(2)	N26 BufD(1)	N27 BufD(0)	N28 BufD(35)	N29 BufA(16)	N30 BufA(15)
P1	P2	P3	P4	P5	P6 GND	P7	P8	P9	P10 VCCO_2	P11 VCCINT	P12 GND	P13 GND	P14 GND	P15 GND	P16 GND	P17 GND	P18 GND	P19 GND	P20 VCCINT	P21 VCCO_7	P22 BufD(12)	P23 BufD(11)	P24 BufD(10)	P25 GND	P26 BufD(9)	P27 BufD(8)	P28 BufD(7)	P29 BufD(6)	P30 BufD(5)
R1 VCCAUX	R2	R3	R4	R5	R6	R7	R8	R9	R10 VCCO_2	R11 VCCINT	R12 GND	R13 GND	R14 GND	R15 GND	R16 GND	R17 GND	R18 GND	R19 GND	R20 VCCINT	R21 VCCO_7	R22 BufA(18)	R23 BufA(17)	R24 BufA(8)	R25 BufA(9)	R26 BufD(34)	R27 BufD(15)	R28 BufD(14)	R29 BufD(13)	R30 VCCAUX
T1 VCCAUX	T2	T3	T4	T5 Spare(4)	T6 Spare(3)	T7 Spare(2)	T8 Spare(1)	T9 Spare(0)	T10 VCCO_3	T11 VCCINT	T12 GND	T13 GND	T14 GND	T15 GND	T16 GND	T17 GND	T18 GND	T19 GND	T20 VCCINT	T21 VCCO_6	T22 SDRAM_DQ(6)	T23 SDRAM_DQ(5)	T24 SDRAM_DQ(4)	T25 SDRAM_DQ(3)	T26 SDRAM_DQ(2)	T27 SDRAM_DQ(1)	T28 SDRAM_DQ(0)	T29 BufR_W_n	T30 VCCAUX
U1	U2	U3	U4	U5	U6 GND	U7	U8	U9	U10 VCCO_3	U11 VCCINT	U12 GND	U13 GND	U14 GND	U15 GND	U16 GND	U17 GND	U18 GND	U19 GND	U20 VCCINT	U21 VCCO_6	U22 SDRAM_BA(0)	U23 SDRAM_A(11)	U24 SDRAM_CS_n	U25 GND	U26 SDRAM_RAS_n	U27 SDRAM_CAS_n	U28 SDRAM_WE_n	U29 SDRAM_DQM(0)	U30 SDRAM_DQ(7)
V1 A21_Select	V2	V3	V4	V5	V6	V7	V8	V9 VCCO_3	V10 VCCO_3	V11 VCCINT	V12 GND	V13 GND	V14 GND	V15 GND	V16 GND	V17 GND	V18 GND	V19 GND	V20 VCCINT	V21 VCCO_6	V22 VCCO_6	V23 SDRAM_DQ(17)	V24 SDRAM_DQ(16)	V25 SDRAM_DQM(2)	V26 SDRAM_A(2)	V27 SDRAM_A(1)	V28 SDRAM_A(0)	V29 SDRAM_A(10)	V30 SDRAM_BA(1)
W1 Adr(21)	W2 MS0_n	W3 MS1_n	W4 MS2_n	W5 MS3_n	W6 DMAR_n	W7	W8	W9 VCCO_3	W10 VCCO_3	W11 VCCINT	W12 GND	W13 GND	W14 GND	W15 GND	W16 GND	W17 GND	W18 GND	W19 GND	W20 VCCINT	W21 VCCO_6	W22 VCCO_6	W23 SDRAM_DQ(25)	W24 SDRAM_DQ(24)	W25 SDRAM_DQ(23)	W26 SDRAM_DQ(22)	W27 SDRAM_DQ(21)	W28 SDRAM_DQ(20)	W29 SDRAM_DQ(19)	W30 SDRAM_DQ(18)
Y1 Adr(17)	Y2 Adr(18)	Y3 GND	Y4 Adr(19)	Y5 Adr(20)	Y6 GND	Y7	Y8	Y9 VCCO_3	Y10 VCCO_3	Y11 GND	Y12 VCCINT	Y13 VCCINT	Y14 VCCINT	Y15 VCCINT	Y16 VCCINT	Y17 VCCINT	Y18 VCCINT	Y19 VCCINT	Y20 GND	Y21 VCCO_6	Y22 VCCO_6	Y23	Y24	Y25 GND	Y26 SDRAM_DQ(29)	Y27 SDRAM_DQ(28)	Y28 GND	Y29 SDRAM_DQ(27)	Y30 SDRAM_DQ(26)
AA1 Adr(11)	AA2 Adr(12)	AA3 Adr(13)	AA4 Adr(14)	AA5 Adr(15)	AA6 Adr(16)	AA7	AA8	AA9 VCCO_3	AA10 VCCO_4	AA11 VCCO_4	AA12 VCCO_4	AA13 VCCO_4	AA14 VCCO_4	AA15 VCCO_4	AA16 VCCO_5	AA17 VCCO_5	AA18 VCCO_5	AA19 VCCO_5	AA20 VCCO_5	AA21 VCCO_5	AA22 VCCO_6	AA23	AA24	AA25 SDRAM_A(5)	AA26 SDRAM_A(4)	AA27 SDRAM_A(3)	AA28 SDRAM_DQM(3)	AA29 SDRAM_DQ(31)	AA30 SDRAM_DQ(30)
AB1 Adr(7)	AB2 Adr(8)	AB3 Adr(9)	AB4 Adr(10)	AB5	AB6	AB7	AB8	AB9 VCCO_3	AB10 VCCO_4	AB11 VCCO_4	AB12 VCCO_4	AB13 VCCO_4	AB14	AB15 Data(3)	AB16 IRQ2_n	AB17	AB18 VCCO_5	AB19 VCCO_5	AB20 VCCO_5	AB21 VCCO_5	AB22 VCCO_6	AB23	AB24	AB25	AB26	AB27 SDRAM_A(9)	AB28 SDRAM_A(8)	AB29 SDRAM_A(7)	AB30 SDRAM_A(6)
AC1 GND	AC2 Adr(4)	AC3 Adr(5)	AC4 Adr(6)	AC5	AC6	AC7 CCLK	AC8 DONE	AC9 D0	AC10 Data(16)	AC11 Data(11)	AC12 Data(9)	AC13	AC14	AC15 Data(2)	AC16 IRQ1_n	AC17	AC18	AC19 TestCon(8)	AC20 TestCon(9)	AC21 TestCon(10)	AC22 D7	AC23 M2	AC24 M1	AC25	AC26	AC27 SDRAM_DQM(1)	AC28 SDRAM_A(12)	AC29 SDRAM_CKE	AC30 GND
AD1	AD2	AD3	AD4	AD5 Adr(2)	AD6 Adr(3)	AD7 PWRDWN_B	AD8	AD9 D1	AD10 Data(15)	AD11 Data(10)	AD12 Data(8)	AD13	AD14 Data(7)	AD15 Data(1)	AD16 IRQ0_n	AD17	AD18	AD19 TestCon(11)	AD20 TestCon(12)	AD21 TestCon(13)	AD22 D6	AD23	AD24 M0	AD25 SDRAM_DQ(9)	AD26 SDRAM_DQ(8)	AD27	AD28	AD29	AD30
AE1	AE2	AE3	AE4	AE5	AE6 GND	AE7 Data(25)	AE8 Data(24)	AE9 Data(20)	AE10 Data(14)	AE11	AE12	AE13 GND	AE14 Data(6)	AE15 Data(0)	AE16 Empty	AE17	AE18 GND	AE19	AE20	AE21	AE22	AE23	AE24	AE25 GND	AE26	AE27	AE28	AE29	AE30
AF1	AF2	AF3	AF4	AF5 GND	AF6	AF7 INIT_B	AF8 Data(23)	AF9 Data(19)	AF10 Data(13)	AF11	AF12	AF13	AF14 Data(5)	AF15 SDRAM_CLKin	AF16 SDRAM_CLK	AF17	AF18	AF19	AF20	AF21 TTC_n(7)	AF22 TTC_n(6)	AF23 TTC_n(4)	AF24 RDWR_B	AF25	AF26 GND	AF27	AF28	AF29	AF30
AG1 Data(30)	AG2 Data(31)	AG3 Adr(0)	AG4 GND	AG5 Adr(1)	AG6 DOUT	AG7 D2	AG8 VRP_4	AG9 GND	AG10 Data(12)	AG11	AG12 GND	AG13	AG14 Data(4)	AG15 SharcWr_n	AG16 LHC_Clk	AG17 ChaBusy	AG18	AG19 GND	AG20	AG21 TTC_n(5)	AG22 GND	AG23 VRN_5	AG24 D5	AG25 CS_B	AG26 SDRAM_DQ(13)	AG27 GND	AG28 SDRAM_DQ(12)	AG29 SDRAM_DQ(11)	AG30 SDRAM_DQ(10)
AH1 Data(26)	AH2 Data(27)	AH3 GND	AH4 Data(28)	AH5 Data(29)	AH6 GNDA16	AH7 D3	AH8 VRN_4	AH9 Data(18)	AH10	AH11	AH12 GNDA18	AH13	AH14 GND	AH15 SharcRd_n	AH16 Clk	AH17 GND	AH18	AH19 GNDA19	AH20	AH21	AH22 TTC_n(3)	AH23 VRP_5	AH24 D4	AH25 GNDA21	AH26	AH27	AH28 GND	AH29 SDRAM_DQ(15)	AH30 SDRAM_DQ(14)
AJ1 VCCAUX	AJ2 GND	AJ3 VRP_3	AJ4 AVCCAUXRX16	AJ5 VTRXPAD16	AJ6 AVCCAUXTX16	AJ7 VTTXPAD16	AJ8 Data(22)	AJ9 Data(17)	AJ10	AJ11 AVCCAUXRX18	AJ12 VTRXPAD18	AJ13 AVCCAUXTX18	AJ14 VTTXPAD18	AJ15 Rocket_XC1k	AJ16 Clkx2	AJ17 AVCCAUXRX19	AJ18 VTRXPAD19	AJ19 AVCCAUXTX19	AJ20 VTTXPAD19	AJ21	AJ22 TTC_n(2)	AJ23 TTC_n(1)	AJ24 AVCCAUXRX21	AJ25 VTRXPAD21	AJ26 AVCCAUXTX21	AJ27 VTTXPAD21	AJ28 VRP_6	AJ29 GND	AJ30 VCCAUX
	AK2 VCCAUX	AK3 VRN_3	AK4	AK5	AK6	AK7	AK8 Data(21)	AK9 GND	AK10	AK11	AK12	AK13	AK14	AK15 VCCAUX	AK16 VCCAUX	AK17 ROCKET_LVDS ROCKET_LVDS T Rocket_RXN	AK18 ROCKET_LVDS ROCKET_LVDS T Rocket_RXP	AK19 ROCKET_LVDS ROCKET_LVDS S Rocket_TXP	AK20 ROCKET_LVDS ROCKET_LVDS S Rocket_TXN	AK21	AK22 GND	AK23 TTC_n(0)	AK24	AK25	AK26	AK27	AK28 VRN_6	AK29 VCCAUX	

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

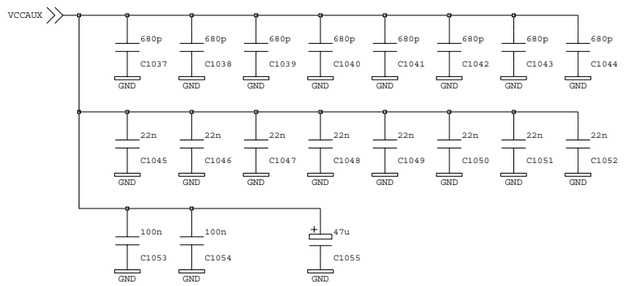
channel_in		Rev V2 2
		Date 7 Feb 2006
Input FPGA		Time 1:50:53 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
		Size A3 4 1 4 A
NIKHEF © ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
		Page 2 of 6

XC2VP7/20 VCCINT Decoupling Capacitors
Min. Power-On Current XC2VP20
IccINT = 600 mA



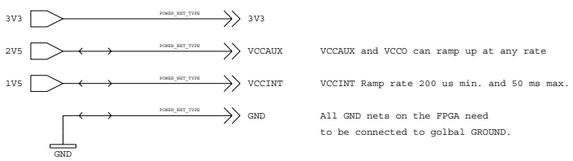
AVX TAJB476K010R

XC2VP7/20 VCCAUX Decoupling Capacitors
Min. Power-On Current XC2VP20
IccAUX = 250 mA (min)



AVX TAJB476K010R

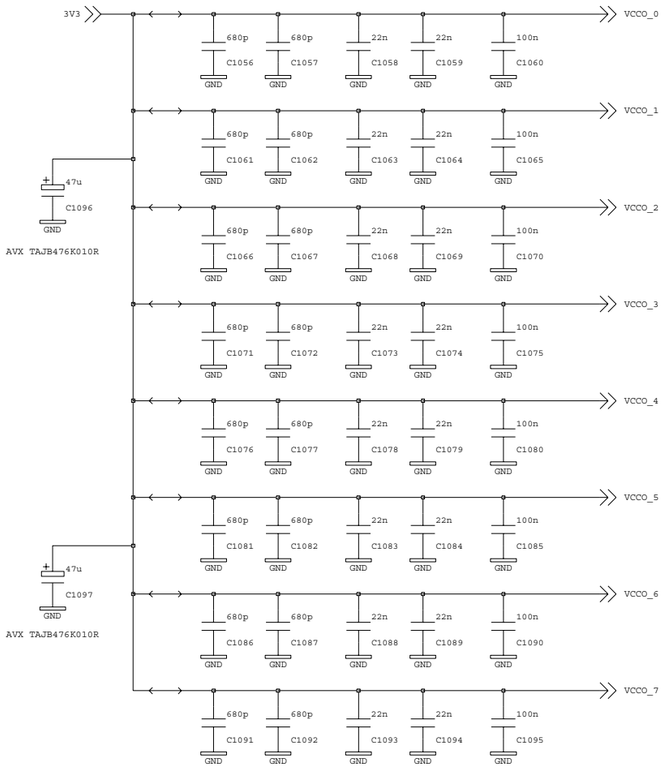
Power Inputs
For Xilinx Virtex-II Pro, power supplies
can be turned on in any sequence.



VCCAUX and VCCO can ramp up at any rate

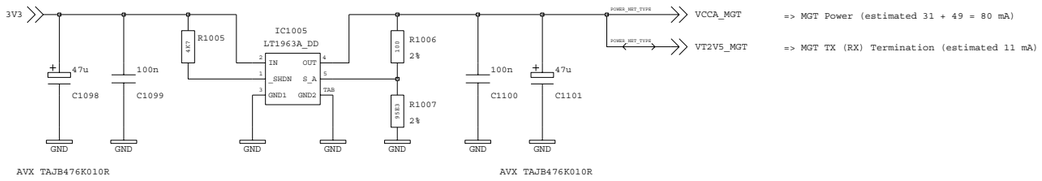
VCCINT Ramp rate 200 us min. and 50 ms max.

All GND nets on the FPGA need
to be connected to golbal GROUND.



channel_in		Rev V2 2
		Date 7 Feb 2006
Input FPGA Power Supply Decoupling		Time 1:51:34 pm
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
		Dim 420 x 297 mm
		Page 3 of 6

2V5 @ 1,5A

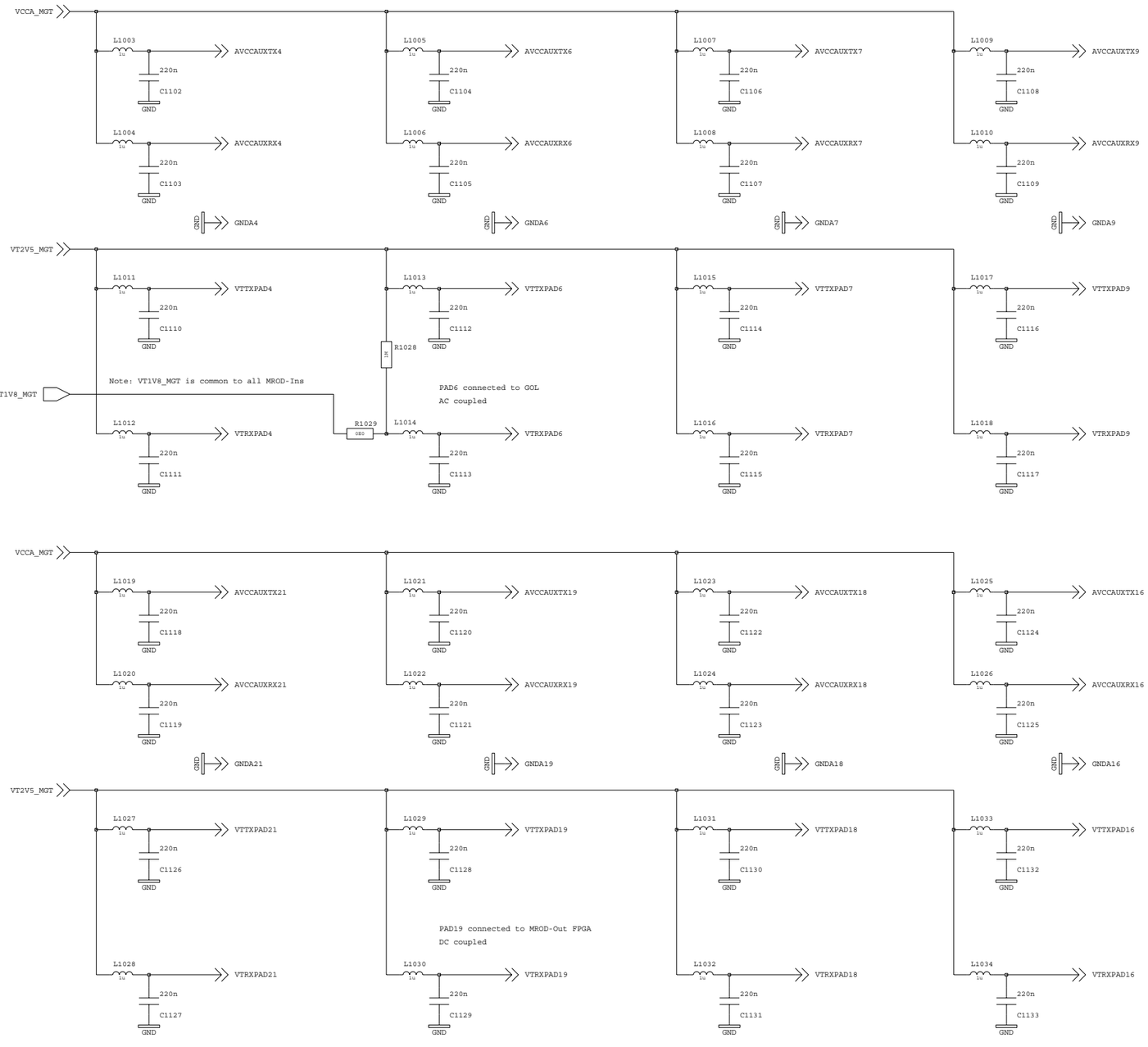


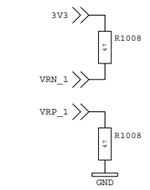
AVX TAJB476K010R

AVX TAJB476K010R

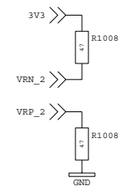
=> MGT Power (estimated 31 + 49 = 80 mA)

=> MGT TX (RX) Termination (estimated 11 mA)

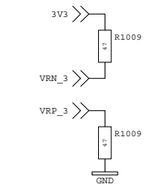




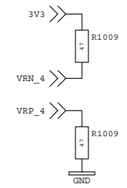
Series Termination for
Not (yet) used



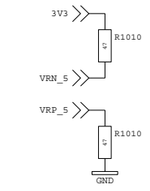
Series Termination for
Not (yet) used



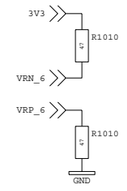
Series Termination for
Sharc Addressbus



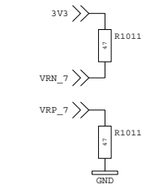
Series Termination for
Sharc Databus



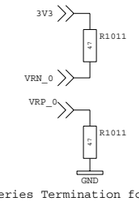
Series Termination for
General purpose



Series Termination for
SDRAM interface



Series Termination for
Buffer Memory interface



Series Termination for
General purpose

channel_in		Rev V2 2	
		Date 7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time 1:52:01 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
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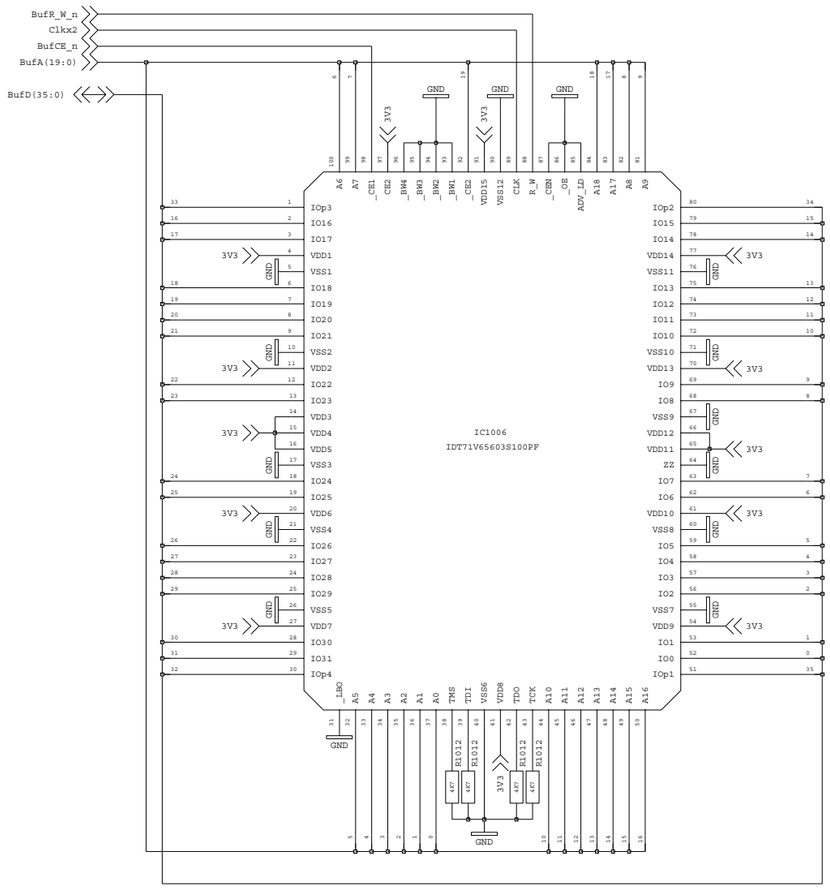
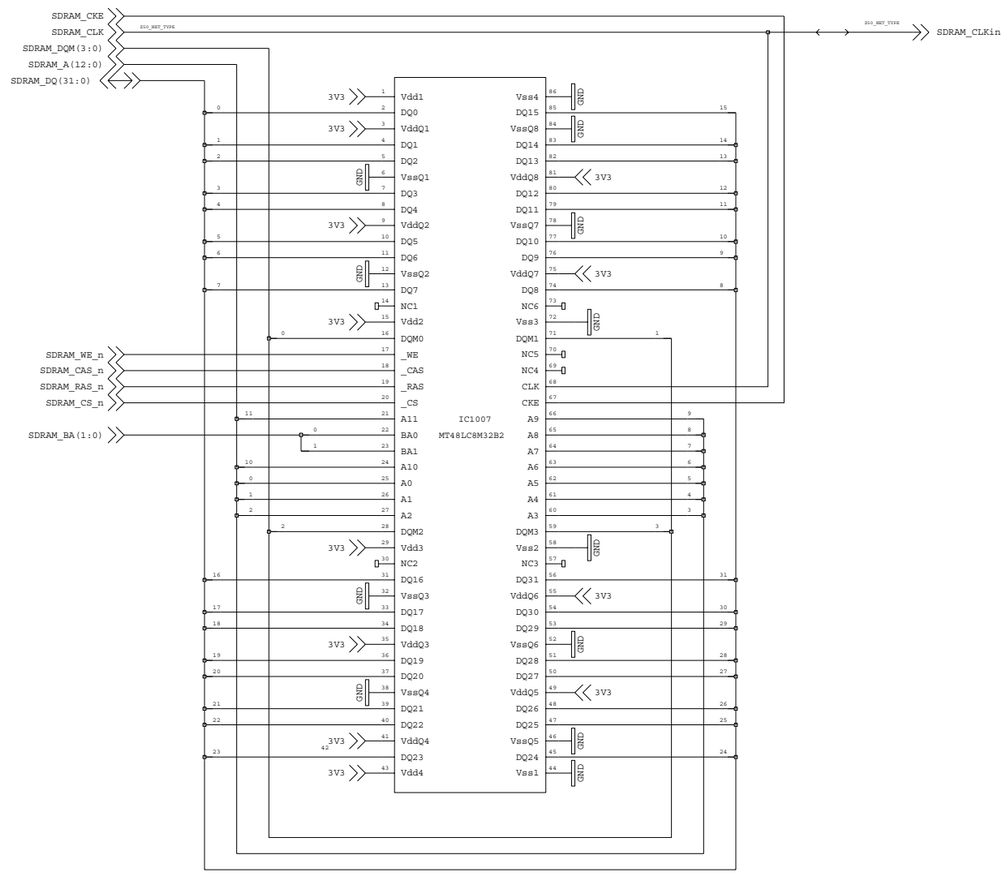
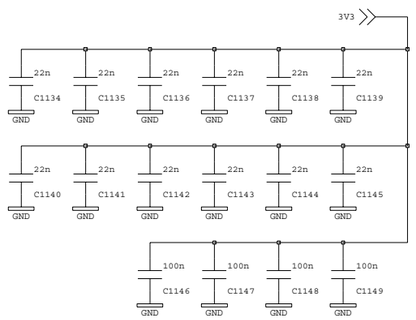
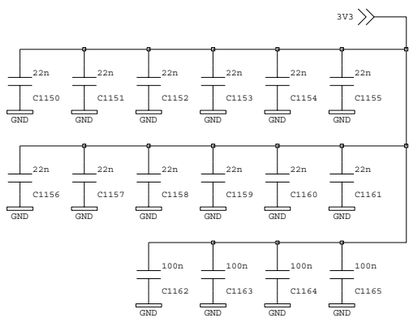
SDRAM_A(12) is not connected









channel_in		Rev V2 2	
		Date 7 Feb 2006	
Buffer Memory (ZBT and SDRAM)		Time 1:52:29 pm	
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
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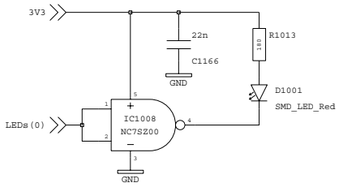
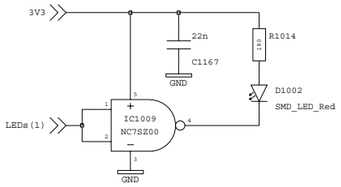
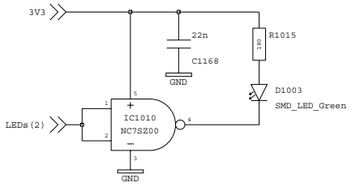
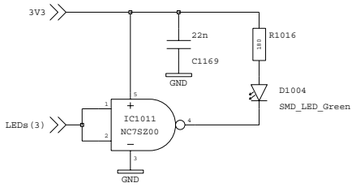
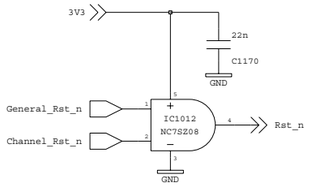


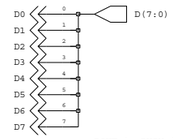




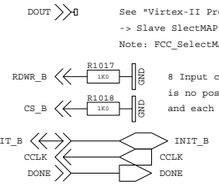




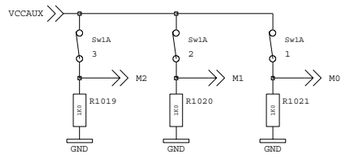
Fiducial1001 Fiducial1002



DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices.
See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SlectMAP programming Mode -> BUSY.
Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!



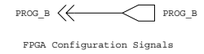
8 Input channels are loaded in parallel so there is no possibility for readback (RDWR_B = '0') and each CS_B = '0'



M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.



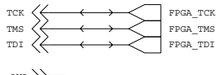
FPGA Configuration Signals

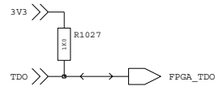
PWRDWN_B is unsupported (should be pulled high)

HSWAP_EN = '0' => User IOs have pull-up resistors during configuration

VBATT is decriptor key memory backup supply

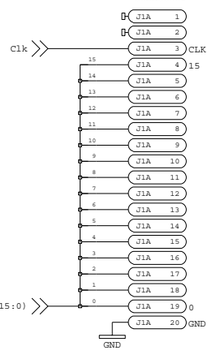
FPGA Control signals



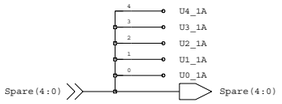


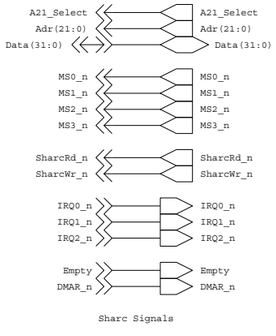
FPGA JTAG Signals

Optinal Test Connector



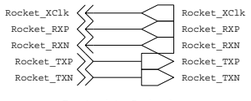
Testpoints force Spare lines to be accessible.





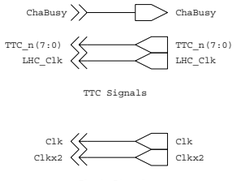
Sharc Signals

Input Channel ID bits



Frontend to Backend

Rocket IO Signals



TTC Signals

Clock Signals

channel_in	Rev V2 2
	Date 7 Feb 2006
	Time 1:53:04 pm
	Name Ton van Reen
Input FPGA Auxiliary Connections	
Proj: MROD-X	Proj.No: 38405
Peter Jansweijer	peterj@nikhef.nl
NIKHEF	Size A3 4 1 4 A
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
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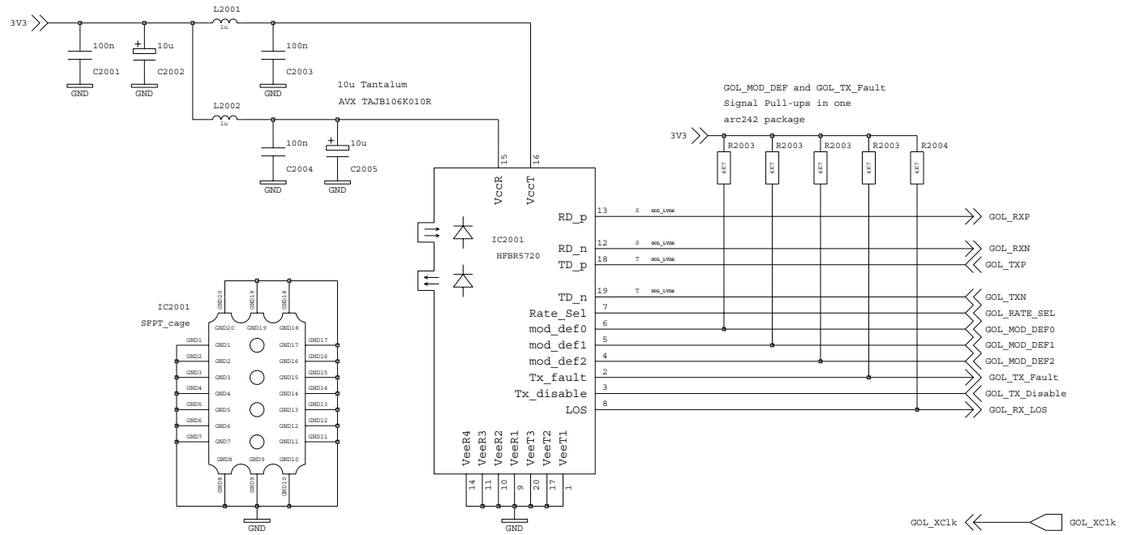

channel_in		Rev V2 2	
GOL Input		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:50:33 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 1 of 6	

IC2004
XC2VP7FF896

	A2 VCCAUX	A3 VRP_2	A4	A5	A6	A7	A8	A9 GND	A10	A11	A12	A13	A14	A15 VCCAUX	A16 VCCAUX	A17 GOL_LVDS gol_lvds T DP_GOL_RX1B	A18 GOL_LVDS gol_lvds T DP_GOL_RX1B	A19 GOL_LVDS gol_lvds S DP_GOL_TX1B	A20 GOL_LVDS gol_lvds S DP_GOL_TX1B	A21	A22 GND	A23 LEDs(0)	A24	A25	A26	A27	A28 VRP_7	A29 VCCAUX	
B1 VCCAUX	B2 GND	B3 VRN_2	B4 AVCCAUXRX9	B5 VTRXPAD9	B6 AVCCAUXTX9	B7 VTTXPAD9	B8	B9	B10	B11 AVCCAUXRX7	B12 VTRXPAD7	B13 AVCCAUXTX7	B14 VTTXPAD7	B15	B16 GOL_XClk	B17 AVCCAUXRX6	B18 VTRXPAD6	B19 AVCCAUXTX6	B20 VTTXPAD6	B21	B22	B23 LEDs(1)	B24 AVCCAUXRX4	B25 VTRXPAD4	B26 AVCCAUXTX4	B27 VTTXPAD4	B28 VRN_7	B29 GND	B30 VCCAUX
C1	C2	C3 GND	C4	C5	C6 GNDA9	C7	C8	C9	C10	C11	C12 GNDA7	C13	C14 GND	C15	C16	C17 GND	C18 UpLED	C19 GNDA6	C20	C21	C22	C23 LEDs(2)	C24 LEDs(3)	C25 GNDA4	C26 BufA(6)	C27 BufA(7)	C28 GND	C29 BufCE_n	C30 BufA(19)
D1	D2	D3 GND	D4	D5	D6	D7	D8	D9 GND	D10	D11	D12 GND	D13	D14	D15	D16 GOL_RX_LOS	D17 GOL_TX_Disable	D18 ErrLED	D19 GND	D20 GOL_MOD_DEF1	D21 GOL_MOD_DEF0	D22 GND	D23 ChaID(1)	D24 ChaID(0)	D25 DXN	D26 BufD(16)	D27 GND	D28 BufD(33)	D29	D30
E1	E2	E3	E4 GND	E5	E6 VRN_1	E7 VRP_1	E8	E9	E10	E11	E12	E13	E14	E15	E16	R17 GOL_TX_Fault	E18	E19	R20 GOL_MOD_DEF2	R21 GOL_RATE_SEL	E22	E23 ChaID(2)	E24 VRN_0	R25 VRP_0	E26 GND	E27	E28	E29	E30
F1	F2	F3	F4	F5 TDO	F6 GND	F7	F8	F9	F10	F11	F12	F13 GND	F14	F15	F16	F17	F18 GND	F19	F20	F21 TestCon(1)	F22 TestCon(0)	F23	F24	F25 GND	F26 TDI	F27	F28	F29	F30
G1	G2	G3	G4	G5	G6	G7 TCK	G8	G9	G10	G11	G12	G13	G14	G15	G16 Rst_n	G17	G18	G19 TestCon(6)	G20 TestCon(5)	G21 TestCon(4)	G22 TestCon(3)	G23 TestCon(2)	G24 PROG_B	G25 BufD(18)	G26 BufD(17)	G27	G28	G29	G30
H1 GND	H2	H3	H4	H5	H6	H7 VBATT	H8 TMS	H9	H10	H11	H12 TestCon(15)	H13	H14	H15	H16	H17	H18	H19 TestCon(7)	H20 T_Alert_n	H21 SMBData	H22 SMBClk	H23 HSWAP_EN	H24 DXP	H25	H26	H27	H28	H29 BufD(19)	H30 GND
J1	J2	J3	J4	J5	J6	J7	J8 TestCon(14)	J9 VCCO_2	J10 VCCO_1	J11 VCCO_1	J12 VCCO_1	J13 VCCO_1	J14	J15	J16	J17	J18 VCCO_0	J19 VCCO_0	J20 VCCO_0	J21 VCCO_0	J22 VCCO_7	J23 BufD(25)	J24 BufD(24)	J25	J26	J27 BufD(23)	J28 BufD(22)	J29 BufD(21)	J30 BufD(20)
K1	K2	K3	K4	K5	K6	K7	K8	K9 VCCO_2	K10 VCCO_1	K11 VCCO_1	K12 VCCO_1	K13 VCCO_1	K14 VCCO_1	K15 VCCO_1	K16 VCCO_0	K17 VCCO_0	K18 VCCO_0	K19 VCCO_0	K20 VCCO_0	K21 VCCO_0	K22 VCCO_7	K23	K24	K25 BufD(31)	K26 BufD(30)	K27 BufD(29)	K28 BufD(28)	K29 BufD(27)	K30 BufD(26)
L1	L2	L3 GND	L4	L5	L6 GND	L7	L8	L9 VCCO_2	L10 VCCO_2	L11 GND	L12 VCCINT	L13 VCCINT	L14 VCCINT	L15 VCCINT	L16 VCCINT	L17 VCCINT	L18 VCCINT	L19 VCCINT	L20 GND	L21 VCCO_7	L22 VCCO_7	L23	L24	L25 GND	L26 BufA(3)	L27 BufA(4)	L28 GND	L29 BufA(5)	L30 BufD(32)
M1	M2	M3	M4	M5	M6	M7	M8	M9 VCCO_2	M10 VCCO_2	M11 VCCINT	M12 GND	M13 GND	M14 GND	M15 GND	M16 GND	M17 GND	M18 GND	M19 GND	M20 VCCINT	M21 VCCO_7	M22 VCCO_7	M23 BufA(14)	M24 BufA(13)	M25 BufA(12)	M26 BufA(11)	M27 BufA(10)	M28 BufA(0)	M29 BufA(1)	M30 BufA(2)
N1	N2	N3	N4	N5	N6	N7	N8	N9 VCCO_2	N10 VCCO_2	N11 VCCINT	N12 GND	N13 GND	N14 GND	N15 GND	N16 GND	N17 GND	N18 GND	N19 GND	N20 VCCINT	N21 VCCO_7	N22 VCCO_7	N23 BufD(4)	N24 BufD(3)	N25 BufD(2)	N26 BufD(1)	N27 BufD(0)	N28 BufD(35)	N29 BufA(16)	N30 BufA(15)
P1	P2	P3	P4	P5	P6 GND	P7	P8	P9	P10 VCCO_2	P11 VCCINT	P12 GND	P13 GND	P14 GND	P15 GND	P16 GND	P17 GND	P18 GND	P19 GND	P20 VCCINT	P21 VCCO_7	P22 BufD(12)	P23 BufD(11)	P24 BufD(10)	P25 GND	P26 BufD(9)	P27 BufD(8)	P28 BufD(7)	P29 BufD(6)	P30 BufD(5)
R1 VCCAUX	R2	R3	R4	R5	R6	R7	R8	R9	R10 VCCO_2	R11 VCCINT	R12 GND	R13 GND	R14 GND	R15 GND	R16 GND	R17 GND	R18 GND	R19 GND	R20 VCCINT	R21 VCCO_7	R22 BufA(18)	R23 BufA(17)	R24 BufA(8)	R25 BufA(9)	R26 BufD(34)	R27 BufD(15)	R28 BufD(14)	R29 BufD(13)	R30 VCCAUX
T1 VCCAUX	T2	T3	T4	T5 Spare(4)	T6 Spare(3)	T7 Spare(2)	T8 Spare(1)	T9 Spare(0)	T10 VCCO_3	T11 VCCINT	T12 GND	T13 GND	T14 GND	T15 GND	T16 GND	T17 GND	T18 GND	T19 GND	T20 VCCINT	T21 VCCO_6	T22 SDRAM_DQ(6)	T23 SDRAM_DQ(5)	T24 SDRAM_DQ(4)	T25 SDRAM_DQ(3)	T26 SDRAM_DQ(2)	T27 SDRAM_DQ(1)	T28 SDRAM_DQ(0)	T29 BufR_W_n	T30 VCCAUX
U1	U2	U3	U4	U5	U6 GND	U7	U8	U9	U10 VCCO_3	U11 VCCINT	U12 GND	U13 GND	U14 GND	U15 GND	U16 GND	U17 GND	U18 GND	U19 GND	U20 VCCINT	U21 VCCO_6	U22 SDRAM_BA(0)	U23 SDRAM_A(11)	U24 SDRAM_CS_n	U25 GND	U26 SDRAM_RAS_n	U27 SDRAM_CAS_n	U28 SDRAM_WE_n	U29 SDRAM_DQM(0)	U30 SDRAM_DQ(7)
V1 A21_Select	V2	V3	V4	V5	V6	V7	V8	V9 VCCO_3	V10 VCCO_3	V11 VCCINT	V12 GND	V13 GND	V14 GND	V15 GND	V16 GND	V17 GND	V18 GND	V19 GND	V20 VCCINT	V21 VCCO_6	V22 VCCO_6	V23 SDRAM_DQ(17)	V24 SDRAM_DQ(16)	V25 SDRAM_DQM(2)	V26 SDRAM_A(2)	V27 SDRAM_A(1)	V28 SDRAM_A(0)	V29 SDRAM_A(10)	V30 SDRAM_BA(1)
W1 Adr(21)	W2 MS0_n	W3 MS1_n	W4 MS2_n	W5 MS3_n	W6 DMAR_n	W7	W8	W9 VCCO_3	W10 VCCO_3	W11 VCCINT	W12 GND	W13 GND	W14 GND	W15 GND	W16 GND	W17 GND	W18 GND	W19 GND	W20 VCCINT	W21 VCCO_6	W22 VCCO_6	W23 SDRAM_DQ(25)	W24 SDRAM_DQ(24)	W25 SDRAM_DQ(23)	W26 SDRAM_DQ(22)	W27 SDRAM_DQ(21)	W28 SDRAM_DQ(20)	W29 SDRAM_DQ(19)	W30 SDRAM_DQ(18)
Y1 Adr(17)	Y2 Adr(18)	Y3 GND	Y4 Adr(19)	Y5 Adr(20)	Y6 GND	Y7	Y8	Y9 VCCO_3	Y10 VCCO_3	Y11 GND	Y12 VCCINT	Y13 VCCINT	Y14 VCCINT	Y15 VCCINT	Y16 VCCINT	Y17 VCCINT	Y18 VCCINT	Y19 VCCINT	Y20 GND	Y21 VCCO_6	Y22 VCCO_6	Y23	Y24	Y25 GND	Y26 SDRAM_DQ(29)	Y27 SDRAM_DQ(28)	Y28 GND	Y29 SDRAM_DQ(27)	Y30 SDRAM_DQ(26)
AA1 Adr(11)	AA2 Adr(12)	AA3 Adr(13)	AA4 Adr(14)	AA5 Adr(15)	AA6 Adr(16)	AA7	AA8	AA9 VCCO_3	AA10 VCCO_4	AA11 VCCO_4	AA12 VCCO_4	AA13 VCCO_4	AA14 VCCO_4	AA15 VCCO_4	AA16 VCCO_5	AA17 VCCO_5	AA18 VCCO_5	AA19 VCCO_5	AA20 VCCO_5	AA21 VCCO_5	AA22 VCCO_6	AA23	AA24	AA25 SDRAM_A(5)	AA26 SDRAM_A(4)	AA27 SDRAM_A(3)	AA28 SDRAM_DQM(3)	AA29 SDRAM_DQ(31)	AA30 SDRAM_DQ(30)
AB1 Adr(7)	AB2 Adr(8)	AB3 Adr(9)	AB4 Adr(10)	AB5	AB6	AB7	AB8	AB9 VCCO_3	AB10 VCCO_4	AB11 VCCO_4	AB12 VCCO_4	AB13 VCCO_4	AB14	AB15 Data(3)	AB16 IRQ2_n	AB17	AB18 VCCO_5	AB19 VCCO_5	AB20 VCCO_5	AB21 VCCO_5	AB22 VCCO_6	AB23	AB24	AB25	AB26	AB27 SDRAM_A(9)	AB28 SDRAM_A(8)	AB29 SDRAM_A(7)	AB30 SDRAM_A(6)
AC1 GND	AC2 Adr(4)	AC3 Adr(5)	AC4 Adr(6)	AC5	AC6	AC7 CCLK	AC8 DONE	AC9 D0	AC10 Data(16)	AC11 Data(11)	AC12 Data(9)	AC13	AC14	AC15 Data(2)	AC16 IRQ1_n	AC17	AC18	AC19 TestCon(8)	AC20 TestCon(9)	AC21 TestCon(10)	AC22 D7	AC23 M2	AC24 M1	AC25	AC26	AC27 SDRAM_DQM(1)	AC28 SDRAM_A(12)	AC29 SDRAM_CKE	AC30 GND
AD1	AD2	AD3	AD4	AD5 Adr(2)	AD6 Adr(3)	AD7 PWRDWN_B	AD8	AD9 D1	AD10 Data(15)	AD11 Data(10)	AD12 Data(8)	AD13	AD14 Data(7)	AD15 Data(1)	AD16 IRQ0_n	AD17	AD18	AD19 TestCon(11)	AD20 TestCon(12)	AD21 TestCon(13)	AD22 D6	AD23	AD24 M0	AD25 SDRAM_DQ(9)	AD26 SDRAM_DQ(8)	AD27	AD28	AD29	AD30
AE1	AE2	AE3	AE4	AE5	AE6 GND	AE7 Data(25)	AE8 Data(24)	AE9 Data(20)	AE10 Data(14)	AE11	AE12	AE13 GND	AE14 Data(6)	AE15 Data(0)	AE16 Empty	AE17	AE18 GND	AE19	AE20	AE21	AE22	AE23	AE24	AE25 GND	AE26	AE27	AE28	AE29	AE30
AF1	AF2	AF3	AF4	AF5 GND	AF6	AF7 INIT_B	AF8 Data(23)	AF9 Data(19)	AF10 Data(13)	AF11	AF12	AF13	AF14 Data(5)	AF15 SDRAM_CLKin	AF16 SDRAM_CLK	AF17	AF18	AF19	AF20	AF21 TTC_n(7)	AF22 TTC_n(6)	AF23 TTC_n(4)	AF24 RDWR_B	AF25	AF26 GND	AF27	AF28	AF29	AF30
AG1 Data(30)	AG2 Data(31)	AG3 Adr(0)	AG4 GND	AG5 Adr(1)	AG6 DOUT	AG7 D2	AG8 VRP_4	AG9 GND	AG10 Data(12)	AG11	AG12 GND	AG13	AG14 Data(4)	AG15 SharcWr_n	AG16 LHC_Clk	AG17 ChaBusy	AG18	AG19 GND	AG20	AG21 TTC_n(5)	AG22 GND	AG23 VRN_5	AG24 D5	AG25 CS_B	AG26 SDRAM_DQ(13)	AG27 GND	AG28 SDRAM_DQ(12)	AG29 SDRAM_DQ(11)	AG30 SDRAM_DQ(10)
AH1 Data(26)	AH2 Data(27)	AH3 GND	AH4 Data(28)	AH5 Data(29)	AH6 GNDA16	AH7 D3	AH8 VRN_4	AH9 Data(18)	AH10	AH11	AH12 GNDA18	AH13	AH14 GND	AH15 SharcRd_n	AH16 Clk	AH17 GND	AH18	AH19 GNDA19	AH20	AH21	AH22 TTC_n(3)	AH23 VRP_5	AH24 D4	AH25 GNDA21	AH26	AH27	AH28 GND	AH29 SDRAM_DQ(15)	AH30 SDRAM_DQ(14)
AJ1 VCCAUX	AJ2 GND	AJ3 VRP_3	AJ4 AVCCAUXRX16	AJ5 VTRXPAD16	AJ6 AVCCAUXTX16	AJ7 VTTXPAD16	AJ8 Data(22)	AJ9 Data(17)	AJ10	AJ11 AVCCAUXRX18	AJ12 VTRXPAD18	AJ13 AVCCAUXTX18	AJ14 VTTXPAD18	AJ15 Rocket_XC1k	AJ16 Clkx2	AJ17 AVCCAUXRX19	AJ18 VTRXPAD19	AJ19 AVCCAUXTX19	AJ20 VTTXPAD19	AJ21	AJ22 TTC_n(2)	AJ23 TTC_n(1)	AJ24 AVCCAUXRX21	AJ25 VTRXPAD21	AJ26 AVCCAUXTX21	AJ27 VTTXPAD21	AJ28 VRP_6	AJ29 GND	AJ30 VCCAUX
	AK2 VCCAUX	AK3 VRN_3	AK4	AK5	AK6	AK7	AK8 Data(21)	AK9 GND	AK10	AK11	AK12	AK13	AK14	AK15 VCCAUX	AK16 VCCAUX	AK17 ROCKET_LVDS T Rocket_RXN	AK18 ROCKET_LVDS T Rocket_RXP	AK19 ROCKET_LVDS S Rocket_TXP	AK20 ROCKET_LVDS S Rocket_TXN	AK21	AK22 GND	AK23 TTC_n(0)	AK24	AK25	AK26	AK27	AK28 VRN_6	AK29 VCCAUX	

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

channel_in	Rev V2 2
	Date 7 Feb 2006
Input FPGA	Time 1:50:53 pm
Proj: MROD-X	Proj.No: 38405
	Name tonvr
Peter Jansweijer	peterj@nikhef.nl
	Size A3 4 1 4 A
NIKHEF	Dim 420 x 297 mm
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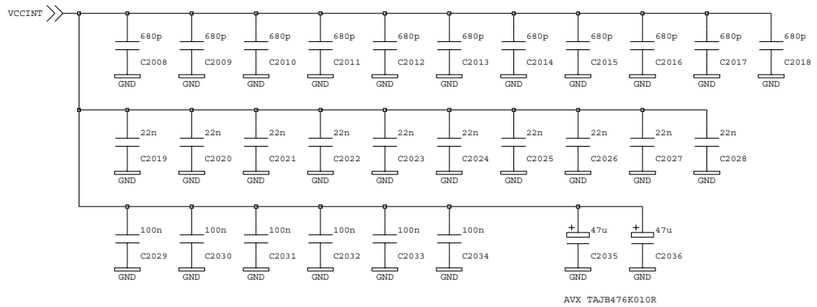
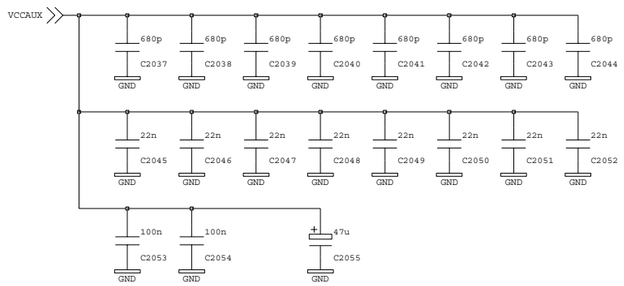
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND

XC2VP7/20 VCCINT Decoupling Capacitors
Min. Power-On Current XC2VP20
IccINT = 600 mA



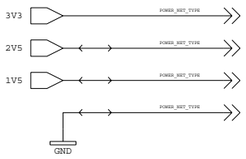
AVX TAJB476K010R

XC2VP7/20 VCCAUX Decoupling Capacitors
Min. Power-On Current XC2VP20
IccAUX = 250 mA (min)



AVX TAJB476K010R

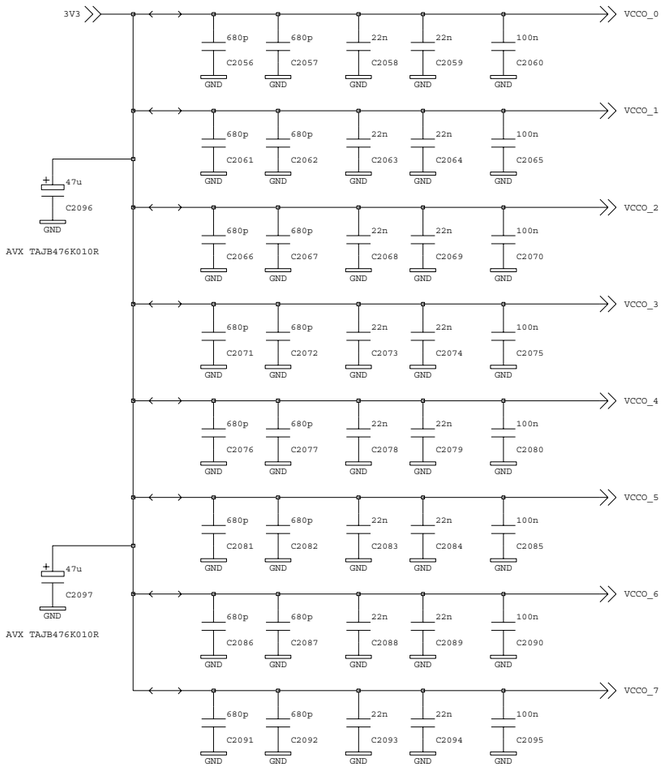
Power Inputs
For Xilinx Virtex-II Pro, power supplies
can be turned on in any sequence.



VCCAUX and VCCO can ramp up at any rate

VCCINT Ramp rate 200 us min. and 50 ms max.

All GND nets on the FPGA need
to be connected to golbal GROUND.

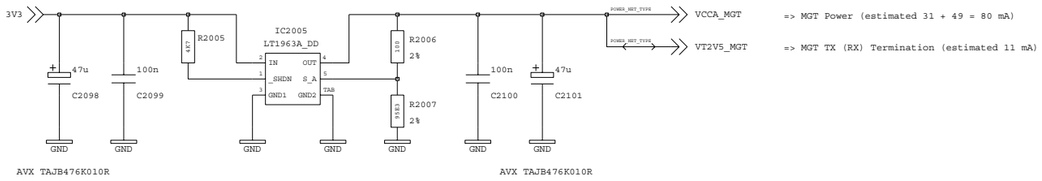


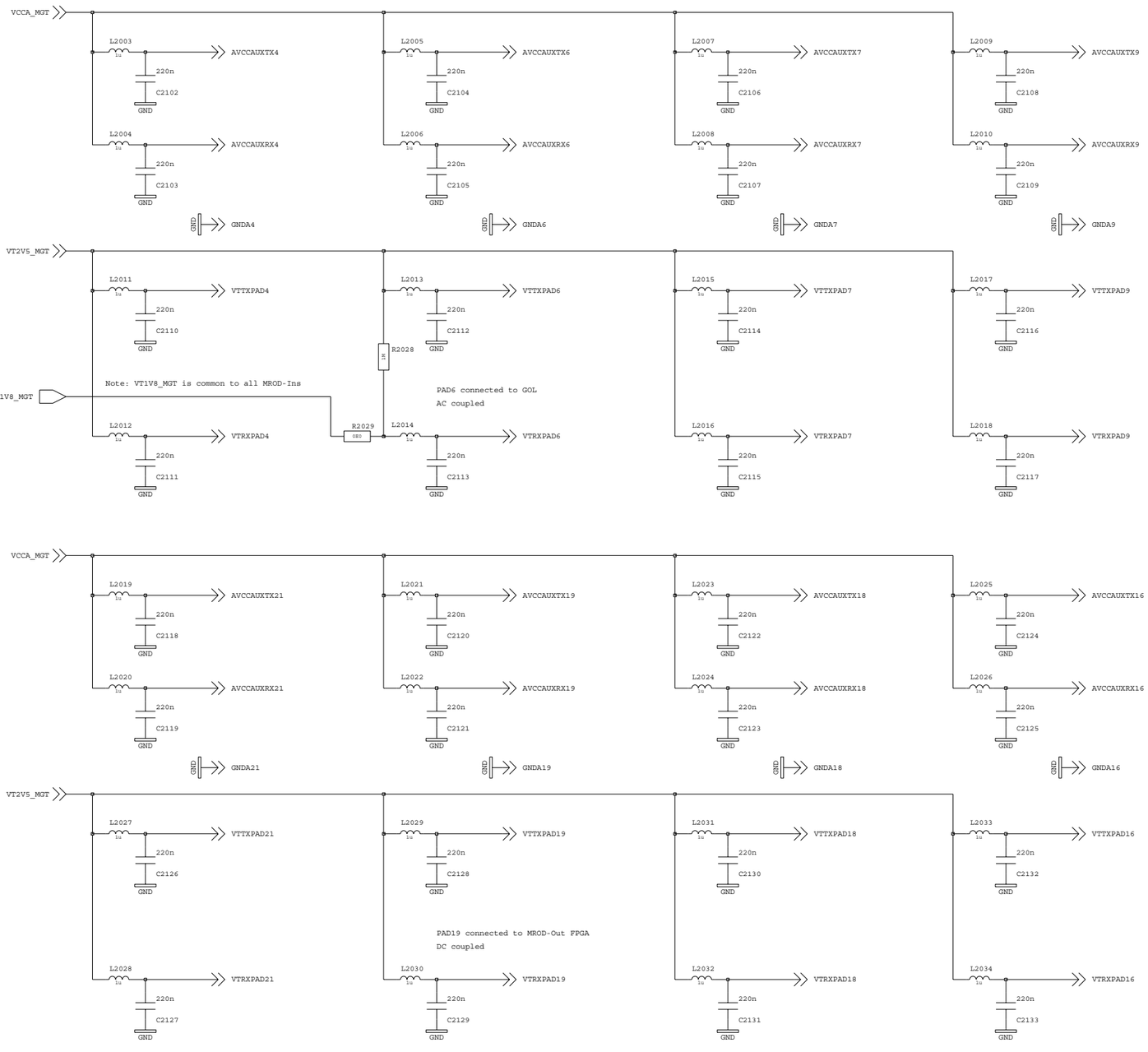
AVX TAJB476K010R

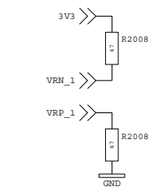
AVX TAJB476K010R

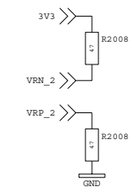
channel_in		Rev V2 2	
		Date 7 Feb 2006	
Input FPGA Power Supply Decoupling		Time 1:51:34 pm	
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
© RT-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 3 of 6	

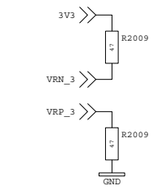
2V5 @ 1,5A

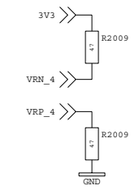


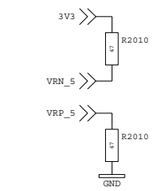


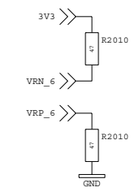


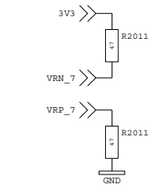


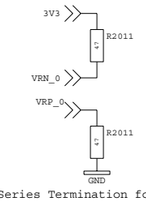






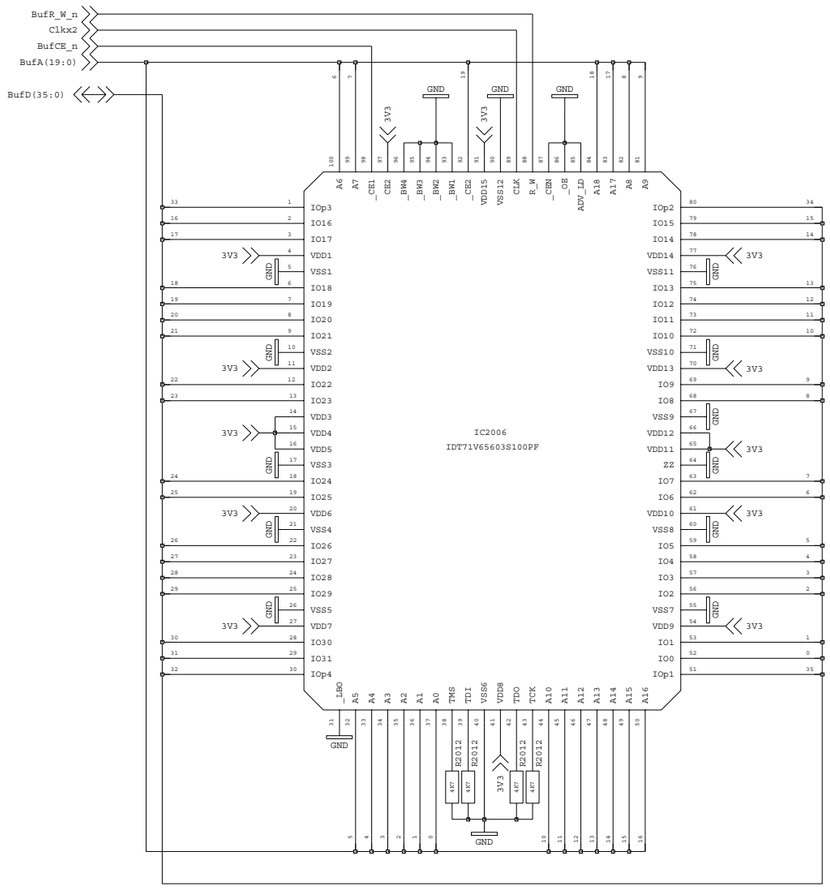


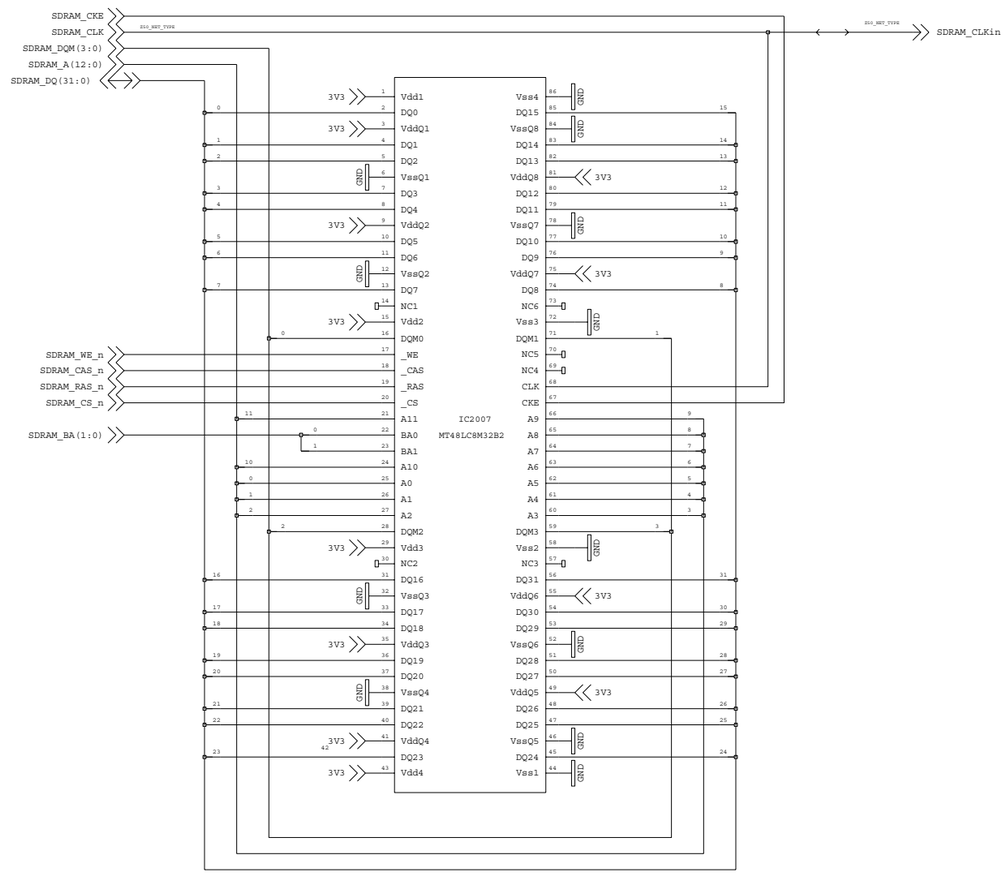


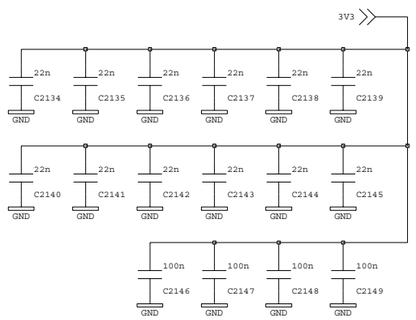


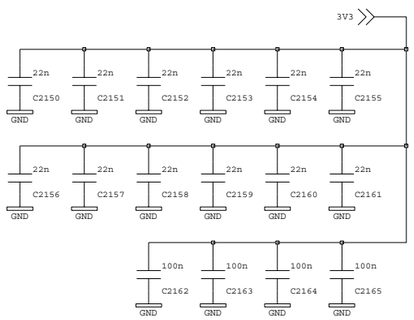
channel_in		Rev V2 2	
		Date 7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time 1:52:01 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
© ET-Nikhef Amsterdam		Page 4 of 6	

SDRAM_A(12) is not connected

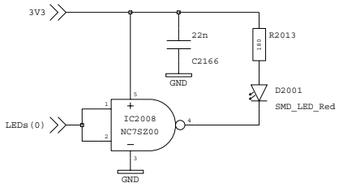


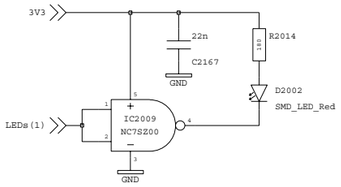


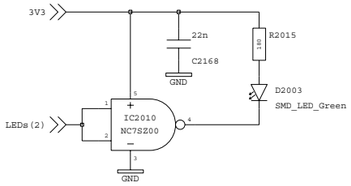


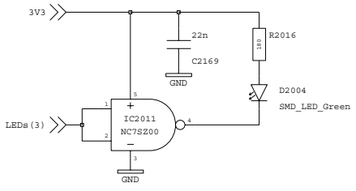


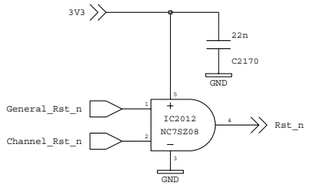
channel_in		Rev	V2 2
		Date	7 Feb 2006
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm
Proj: MROD-X	Proj.No: 38405	Name	Ton van Reen
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size	A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim	420 x 297 mm
		Page	5 of 6



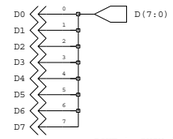




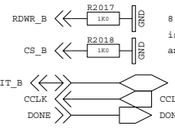




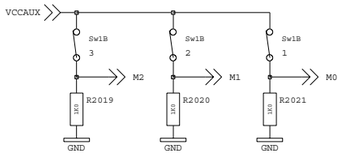
Fiducial2001 Fiducial2002



DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices.
See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SlectMAP programming Mode -> BUSY.
Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!



8 Input channels are loaded in parallel so there is no possibility for readback (RDWR_B = '0')
and each CS_B = '0'

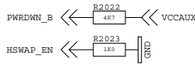


M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.

FPGA Configuration Signals



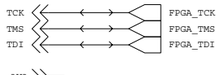
PWRDWN_B is unsupported (should be pulled high)

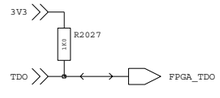
HSWAP_EN = '0' => User IOs have pull-up resistors during configuration

Temperature sensing diode

VBATT is decriptor key memory backup supply

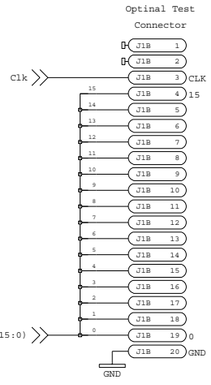
FPGA Control signals



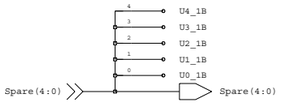


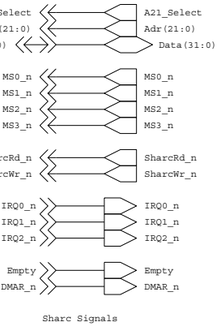
FPGA JTAG Signals

Optinal Test Connector



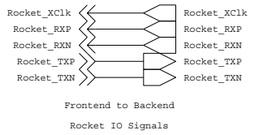
Testpoints force Spare lines to be accessible.





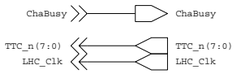
Sharc Signals

Input Channel ID bits

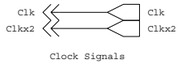


Frontend to Backend

Rocket IO Signals

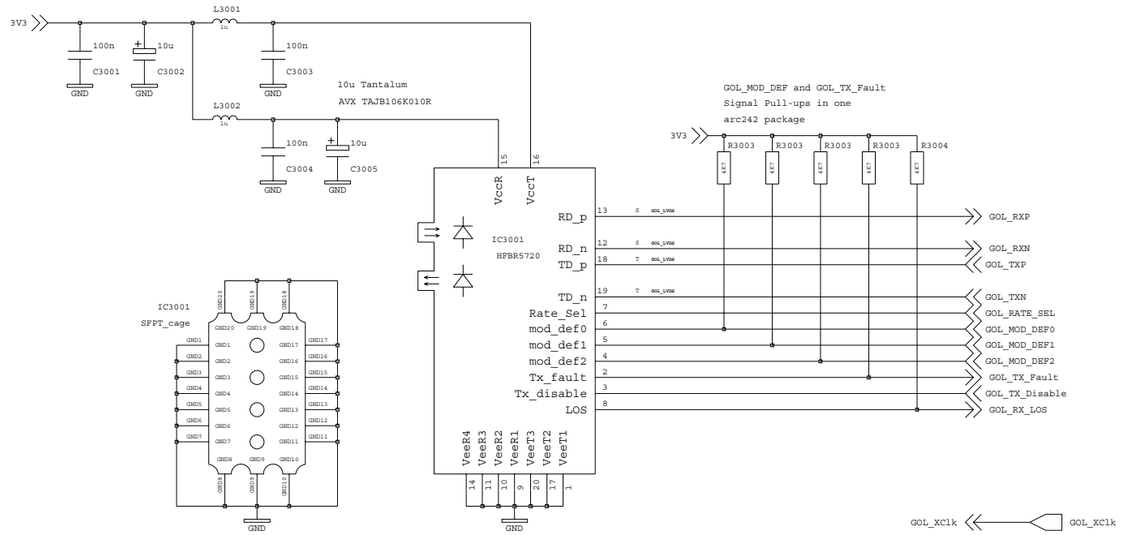


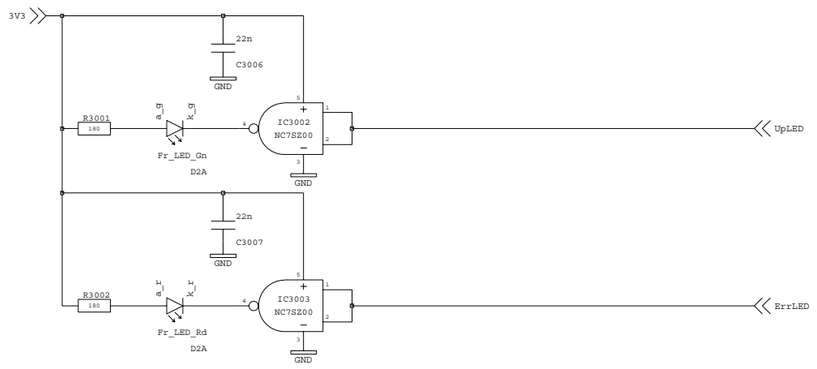
TTC Signals



Clock Signals

channel_in		Rev V2 2
		Date 7 Feb 2006
		Time 1:53:04 pm
Input FPGA Auxiliary Connections		Name Ton van Reen
Proj: MROD-X	Proj.No: 38405	
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 6 of 6





channel_in	Rev V2 2
	Date 7 Feb 2006
GOL Input	Time 1:50:33 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	
NIKHEF	Size A3 / 4 1 4 A
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
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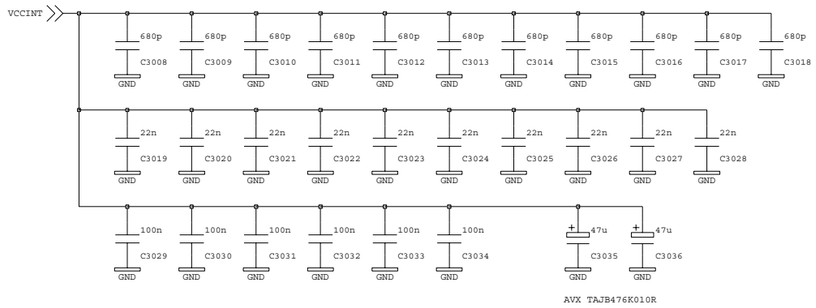
IC3004
XC2VP7FF896

	A2 VCCAUX	A3 VRP_2	A4	A5	A6	A7	A8	A9 GND	A10	A11	A12 VTRXPAD7	A13	A14	A15 VCCAUX	A16 VCCAUX	A17 GOL_LVDS GOL_LVDS T DP_GOL_RX2A	A18 GOL_LVDS GOL_LVDS T DP_GOL_RX2A	A19 GOL_LVDS GOL_LVDS S DP_GOL_TX2A	A20 GOL_LVDS GOL_LVDS S DP_GOL_TX2A	A21	A22 GND	A23 LEDs(0)	A24	A25	A26	A27	A28 VRP_7	A29 VCCAUX	
B1 VCCAUX	B2 GND	B3 VRN_2	B4 AVCCAUXRX9	B5 VTRXPAD9	B6 AVCCAUXTX9	B7 VTTXPAD9	B8	B9	B10	B11 AVCCAUXRX7	B12	B13 AVCCAUXTX7	B14 VTTXPAD7	B15	B16 GOL_XClk	B17 AVCCAUXRX6	B18 VTRXPAD6	B19 AVCCAUXTX6	B20 VTTXPAD6	B21	B22	B23 LEDs(1)	B24 AVCCAUXRX4	B25 VTRXPAD4	B26 AVCCAUXTX4	B27 VTTXPAD4	B28 VRN_7	B29 GND	B30 VCCAUX
C1	C2	C3 GND	C4	C5	C6 GNDA9	C7	C8	C9	C10	C11	C12 GNDA7	C13	C14 GND	C15	C16	C17 GND	C18 UpLED	C19 GNDA6	C20	C21	C22	C23 LEDs(2)	C24 LEDs(3)	C25 GNDA4	C26 BufA(6)	C27 BufA(7)	C28 GND	C29 BufCE_n	C30 BufA(19)
D1	D2	D3 GND	D4	D5	D6	D7	D8	D9 GND	D10	D11	D12 GND	D13	D14	D15	D16 GOL_RX_LOS	D17 GOL_TX_Disable	D18 ErrLED	D19 GND	D20 GOL_MOD_DEF1	D21 GOL_MOD_DEF0	D22 GND	D23 ChaID(1)	D24 ChaID(0)	D25 DXN	D26 BufD(16)	D27 GND	D28 BufD(33)	D29	D30
E1	E2	E3	E4 GND	E5 GND	E6 VRN_1	E7 VRP_1	E8	E9	E10	E11	E12	E13	E14	E15	E16	R17 GOL_TX_Fault	E18	E19	E20 GOL_MOD_DEF2	E21 GOL_RATE_SEL	E22	E23 ChaID(2)	E24 VRN_0	E25 VRP_0	E26 GND	E27	E28	E29	E30
F1	F2	F3	F4	F5 TDO	F6 GND	F7	F8	F9	F10	F11	F12	F13 GND	F14	F15	F16	F17	F18 GND	F19	F20	F21 TestCon(1)	F22 TestCon(0)	F23	F24	F25 GND	F26 TDI	F27	F28	F29	F30
G1	G2	G3	G4	G5	G6	G7 TCK	G8	G9	G10	G11	G12	G13	G14	G15	G16 Rst_n	G17	G18	G19 TestCon(6)	G20 TestCon(5)	G21 TestCon(4)	G22 TestCon(3)	G23 TestCon(2)	G24 PROG_B	G25 BufD(18)	G26 BufD(17)	G27	G28	G29	G30
H1 GND	H2	H3	H4	H5	H6	H7 VBATT	H8 TMS	H9	H10	H11	H12 TestCon(15)	H13	H14	H15	H16	H17	H18	H19 TestCon(7)	H20 T_Alert_n	H21 SMBData	H22 SMBClk	H23 HSWAP_EN	H24 DXP	H25	H26	H27	H28	H29 BufD(19)	H30 GND
J1	J2	J3	J4	J5	J6	J7	J8 TestCon(14)	J9 VCCO_2	J10 VCCO_1	J11 VCCO_1	J12 VCCO_1	J13 VCCO_1	J14	J15	J16	J17	J18 VCCO_0	J19 VCCO_0	J20 VCCO_0	J21 VCCO_0	J22 VCCO_7	J23 BufD(25)	J24 BufD(24)	J25	J26	J27 BufD(23)	J28 BufD(22)	J29 BufD(21)	J30 BufD(20)
K1	K2	K3	K4	K5	K6	K7	K8	K9 VCCO_2	K10 VCCO_1	K11 VCCO_1	K12 VCCO_1	K13 VCCO_1	K14 VCCO_1	K15 VCCO_1	K16 VCCO_0	K17 VCCO_0	K18 VCCO_0	K19 VCCO_0	K20 VCCO_0	K21 VCCO_0	K22 VCCO_7	K23	K24	K25 BufD(31)	K26 BufD(30)	K27 BufD(29)	K28 BufD(28)	K29 BufD(27)	K30 BufD(26)
L1	L2	L3 GND	L4	L5	L6 GND	L7	L8	L9 VCCO_2	L10 VCCO_2	L11 GND	L12 VCCINT	L13 VCCINT	L14 VCCINT	L15 VCCINT	L16 VCCINT	L17 VCCINT	L18 VCCINT	L19 VCCINT	L20 GND	L21 VCCO_7	L22 VCCO_7	L23	L24	L25 GND	L26 BufA(3)	L27 BufA(4)	L28 GND	L29 BufA(5)	L30 BufD(32)
M1	M2	M3	M4	M5	M6	M7	M8	M9 VCCO_2	M10 VCCO_2	M11 VCCINT	M12 GND	M13 GND	M14 GND	M15 GND	M16 GND	M17 GND	M18 GND	M19 GND	M20 VCCINT	M21 VCCO_7	M22 VCCO_7	M23 BufA(14)	M24 BufA(13)	M25 BufA(12)	M26 BufA(11)	M27 BufA(10)	M28 BufA(0)	M29 BufA(1)	M30 BufA(2)
N1	N2	N3	N4	N5	N6	N7	N8	N9 VCCO_2	N10 VCCO_2	N11 VCCINT	N12 GND	N13 GND	N14 GND	N15 GND	N16 GND	N17 GND	N18 GND	N19 GND	N20 VCCINT	N21 VCCO_7	N22 VCCO_7	N23 BufD(4)	N24 BufD(3)	N25 BufD(2)	N26 BufD(1)	N27 BufD(0)	N28 BufD(35)	N29 BufA(16)	N30 BufA(15)
P1	P2	P3	P4	P5	P6 GND	P7	P8	P9	P10 VCCO_2	P11 VCCINT	P12 GND	P13 GND	P14 GND	P15 GND	P16 GND	P17 GND	P18 GND	P19 GND	P20 VCCINT	P21 VCCO_7	P22 BufD(12)	P23 BufD(11)	P24 BufD(10)	P25 GND	P26 BufD(9)	P27 BufD(8)	P28 BufD(7)	P29 BufD(6)	P30 BufD(5)
R1 VCCAUX	R2	R3	R4	R5	R6	R7	R8	R9	R10 VCCO_2	R11 VCCINT	R12 GND	R13 GND	R14 GND	R15 GND	R16 GND	R17 GND	R18 GND	R19 GND	R20 VCCINT	R21 VCCO_7	R22 BufA(18)	R23 BufA(17)	R24 BufA(8)	R25 BufA(9)	R26 BufD(34)	R27 BufD(15)	R28 BufD(14)	R29 BufD(13)	R30 VCCAUX
T1 VCCAUX	T2	T3	T4	T5 Spare(4)	T6 Spare(3)	T7 Spare(2)	T8 Spare(1)	T9 Spare(0)	T10 VCCO_3	T11 VCCINT	T12 GND	T13 GND	T14 GND	T15 GND	T16 GND	T17 GND	T18 GND	T19 GND	T20 VCCINT	T21 VCCO_6	T22 SDRAM_DQ(6)	T23 SDRAM_DQ(5)	T24 SDRAM_DQ(4)	T25 SDRAM_DQ(3)	T26 SDRAM_DQ(2)	T27 SDRAM_DQ(1)	T28 SDRAM_DQ(0)	T29 BufR_W_n	T30 VCCAUX
U1	U2	U3	U4	U5	U6 GND	U7	U8	U9	U10 VCCO_3	U11 VCCINT	U12 GND	U13 GND	U14 GND	U15 GND	U16 GND	U17 GND	U18 GND	U19 GND	U20 VCCINT	U21 VCCO_6	U22 SDRAM_BA(0)	U23 SDRAM_A(11)	U24 SDRAM_CS_n	U25 GND	U26 SDRAM_RAS_n	U27 SDRAM_CAS_n	U28 SDRAM_WE_n	U29 SDRAM_DQM(0)	U30 SDRAM_DQ(7)
V1 A21_Select	V2	V3	V4	V5	V6	V7	V8	V9 VCCO_3	V10 VCCO_3	V11 VCCINT	V12 GND	V13 GND	V14 GND	V15 GND	V16 GND	V17 GND	V18 GND	V19 GND	V20 VCCINT	V21 VCCO_6	V22 VCCO_6	V23 SDRAM_DQ(17)	V24 SDRAM_DQ(16)	V25 SDRAM_DQM(2)	V26 SDRAM_A(2)	V27 SDRAM_A(1)	V28 SDRAM_A(0)	V29 SDRAM_A(10)	V30 SDRAM_BA(1)
W1 Adr(21)	W2 MS0_n	W3 MS1_n	W4 MS2_n	W5 MS3_n	W6 DMAR_n	W7	W8	W9 VCCO_3	W10 VCCO_3	W11 VCCINT	W12 GND	W13 GND	W14 GND	W15 GND	W16 GND	W17 GND	W18 GND	W19 GND	W20 VCCINT	W21 VCCO_6	W22 VCCO_6	W23 SDRAM_DQ(25)	W24 SDRAM_DQ(24)	W25 SDRAM_DQ(23)	W26 SDRAM_DQ(22)	W27 SDRAM_DQ(21)	W28 SDRAM_DQ(20)	W29 SDRAM_DQ(19)	W30 SDRAM_DQ(18)
Y1 Adr(17)	Y2 Adr(18)	Y3 GND	Y4 Adr(19)	Y5 Adr(20)	Y6 GND	Y7	Y8	Y9 VCCO_3	Y10 VCCO_3	Y11 GND	Y12 VCCINT	Y13 VCCINT	Y14 VCCINT	Y15 VCCINT	Y16 VCCINT	Y17 VCCINT	Y18 VCCINT	Y19 VCCINT	Y20 GND	Y21 VCCO_6	Y22 VCCO_6	Y23	Y24	Y25 GND	Y26 SDRAM_DQ(29)	Y27 SDRAM_DQ(28)	Y28 GND	Y29 SDRAM_DQ(27)	Y30 SDRAM_DQ(26)
AA1 Adr(11)	AA2 Adr(12)	AA3 Adr(13)	AA4 Adr(14)	AA5 Adr(15)	AA6 Adr(16)	AA7	AA8	AA9 VCCO_3	AA10 VCCO_4	AA11 VCCO_4	AA12 VCCO_4	AA13 VCCO_4	AA14 VCCO_4	AA15 VCCO_4	AA16 VCCO_5	AA17 VCCO_5	AA18 VCCO_5	AA19 VCCO_5	AA20 VCCO_5	AA21 VCCO_5	AA22 VCCO_6	AA23	AA24	AA25 SDRAM_A(5)	AA26 SDRAM_A(4)	AA27 SDRAM_A(3)	AA28 SDRAM_DQM(3)	AA29 SDRAM_DQ(31)	AA30 SDRAM_DQ(30)
AB1 Adr(7)	AB2 Adr(8)	AB3 Adr(9)	AB4 Adr(10)	AB5	AB6	AB7	AB8	AB9 VCCO_3	AB10 VCCO_4	AB11 VCCO_4	AB12 VCCO_4	AB13 VCCO_4	AB14	AB15 Data(3)	AB16 IRQ2_n	AB17	AB18 VCCO_5	AB19 VCCO_5	AB20 VCCO_5	AB21 VCCO_5	AB22 VCCO_6	AB23	AB24	AB25	AB26	AB27 SDRAM_A(9)	AB28 SDRAM_A(8)	AB29 SDRAM_A(7)	AB30 SDRAM_A(6)
AC1 GND	AC2 Adr(4)	AC3 Adr(5)	AC4 Adr(6)	AC5	AC6	AC7 CCLK	AC8 DONE	AC9 D0	AC10 Data(16)	AC11 Data(11)	AC12 Data(9)	AC13	AC14	AC15 Data(2)	AC16 IRQ1_n	AC17	AC18	AC19 TestCon(8)	AC20 TestCon(9)	AC21 TestCon(10)	AC22 D7	AC23 M2	AC24 M1	AC25	AC26	AC27 SDRAM_DQM(1)	AC28 SDRAM_A(12)	AC29 SDRAM_CKE	AC30 GND
AD1	AD2	AD3	AD4	AD5 Adr(2)	AD6 Adr(3)	AD7 PWRDWN_B	AD8	AD9 D1	AD10 Data(15)	AD11 Data(10)	AD12 Data(8)	AD13	AD14 Data(7)	AD15 Data(1)	AD16 IRQ0_n	AD17	AD18	AD19 TestCon(11)	AD20 TestCon(12)	AD21 TestCon(13)	AD22 D6	AD23	AD24 M0	AD25 SDRAM_DQ(9)	AD26 SDRAM_DQ(8)	AD27	AD28	AD29	AD30
AE1	AE2	AE3	AE4	AE5	AE6 GND	AE7 Data(25)	AE8 Data(24)	AE9 Data(20)	AE10 Data(14)	AE11	AE12	AE13 GND	AE14 Data(6)	AE15 Data(0)	AE16 Empty	AE17	AE18 GND	AE19	AE20	AE21	AE22	AE23	AE24	AE25 GND	AE26	AE27	AE28	AE29	AE30
AF1	AF2	AF3	AF4	AF5 GND	AF6	AF7 INIT_B	AF8 Data(23)	AF9 Data(19)	AF10 Data(13)	AF11	AF12	AF13	AF14 Data(5)	AF15 SDRAM_CLKin	AF16 SDRAM_CLK	AF17	AF18	AF19	AF20	AF21 TTC_n(7)	AF22 TTC_n(6)	AF23 TTC_n(4)	AF24 RDWR_B	AF25	AF26 GND	AF27	AF28	AF29	AF30
AG1 Data(30)	AG2 Data(31)	AG3 Adr(0)	AG4 GND	AG5 Adr(1)	AG6 DOUT	AG7 D2	AG8 VRP_4	AG9 GND	AG10 Data(12)	AG11	AG12 GND	AG13	AG14 Data(4)	AG15 SharcWr_n	AG16 LHC_Clk	AG17 ChaBusy	AG18	AG19 GND	AG20	AG21 TTC_n(5)	AG22 GND	AG23 VRN_5	AG24 D5	AG25 CS_B	AG26 SDRAM_DQ(13)	AG27 GND	AG28 SDRAM_DQ(12)	AG29 SDRAM_DQ(11)	AG30 SDRAM_DQ(10)
AH1 Data(26)	AH2 Data(27)	AH3 GND	AH4 Data(28)	AH5 Data(29)	AH6 GNDA16	AH7 D3	AH8 VRN_4	AH9 Data(18)	AH10	AH11	AH12 GNDA18	AH13	AH14 GND	AH15 SharcRd_n	AH16 Clk	AH17 GND	AH18	AH19 GNDA19	AH20	AH21	AH22 TTC_n(3)	AH23 VRP_5	AH24 D4	AH25 GNDA21	AH26	AH27	AH28 GND	AH29 SDRAM_DQ(15)	AH30 SDRAM_DQ(14)
AJ1 VCCAUX	AJ2 GND	AJ3 VRP_3	AJ4 AVCCAUXRX16	AJ5 VTRXPAD16	AJ6 AVCCAUXTX16	AJ7 VTTXPAD16	AJ8 Data(22)	AJ9 Data(17)	AJ10	AJ11 AVCCAUXRX18	AJ12 VTRXPAD18	AJ13 AVCCAUXTX18	AJ14 VTTXPAD18	AJ15 Rocket_XC1k	AJ16 Clkx2	AJ17 AVCCAUXRX19	AJ18 VTRXPAD19	AJ19 AVCCAUXTX19	AJ20 VTTXPAD19	AJ21	AJ22 TTC_n(2)	AJ23 TTC_n(1)	AJ24 AVCCAUXRX21	AJ25 VTRXPAD21	AJ26 AVCCAUXTX21	AJ27 VTTXPAD21	AJ28 VRP_6	AJ29 GND	AJ30 VCCAUX
	AK2 VCCAUX	AK3 VRN_3	AK4	AK5	AK6	AK7	AK8 Data(21)	AK9 GND	AK10	AK11	AK12	AK13	AK14	AK15 VCCAUX	AK16 VCCAUX	AK17 Rocket_RXN ROCKET_LVDS T	AK18 Rocket_RXP ROCKET_LVDS T	AK19 Rocket_TXP ROCKET_LVDS S	AK20 Rocket_TXN ROCKET_LVDS S	AK21	AK22 GND	AK23 TTC_n(0)	AK24	AK25	AK26	AK27	AK28 VRN_6	AK29 VCCAUX	

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

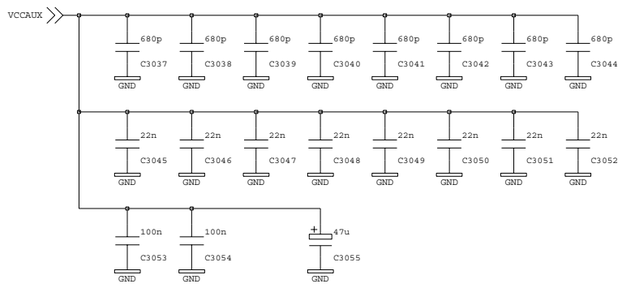
channel_in	Rev V2 2
Input FPGA	Date 7 Feb 2006
Proj: MROD-X	Time 1:50:53 pm
Peter Jansweijer	Name tonvr
peterj@nikhef.nl	Proj.No: 38405
NIKHEF ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND
	Size A3 4 1 4 A
	Dim 420 x 297 mm
	Page 2 of 6

XC2VP7/20 VCCINT Decoupling Capacitors
Min. Power-On Current XC2VP20
IccINT = 600 mA



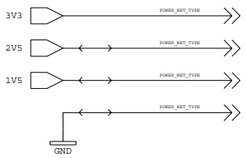
AVX TAJB476K010R

XC2VP7/20 VCCAUX Decoupling Capacitors
Min. Power-On Current XC2VP20
IccAUX = 250 mA (min)



AVX TAJB476K010R

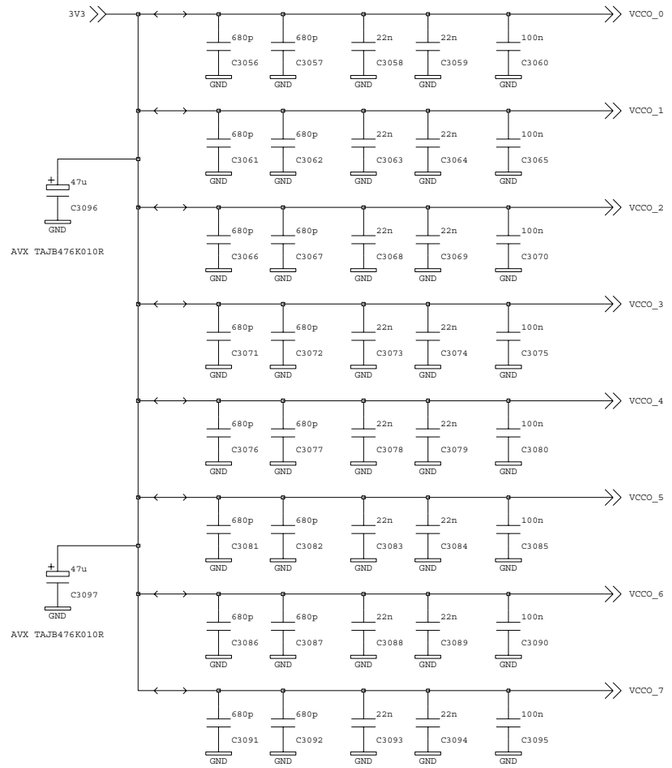
Power Inputs
For Xilinx Virtex-II Pro, power supplies
can be turned on in any sequence.



VCCAUX and VCCO can ramp up at any rate

VCCINT Ramp rate 200 us min. and 50 ms max.

All GND nets on the FPGA need
to be connected to golbal GROUND.

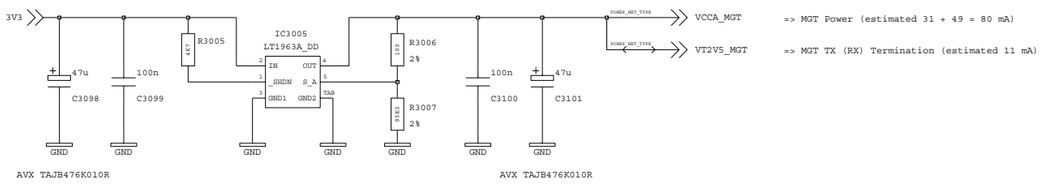


AVX TAJB476K010R

AVX TAJB476K010R

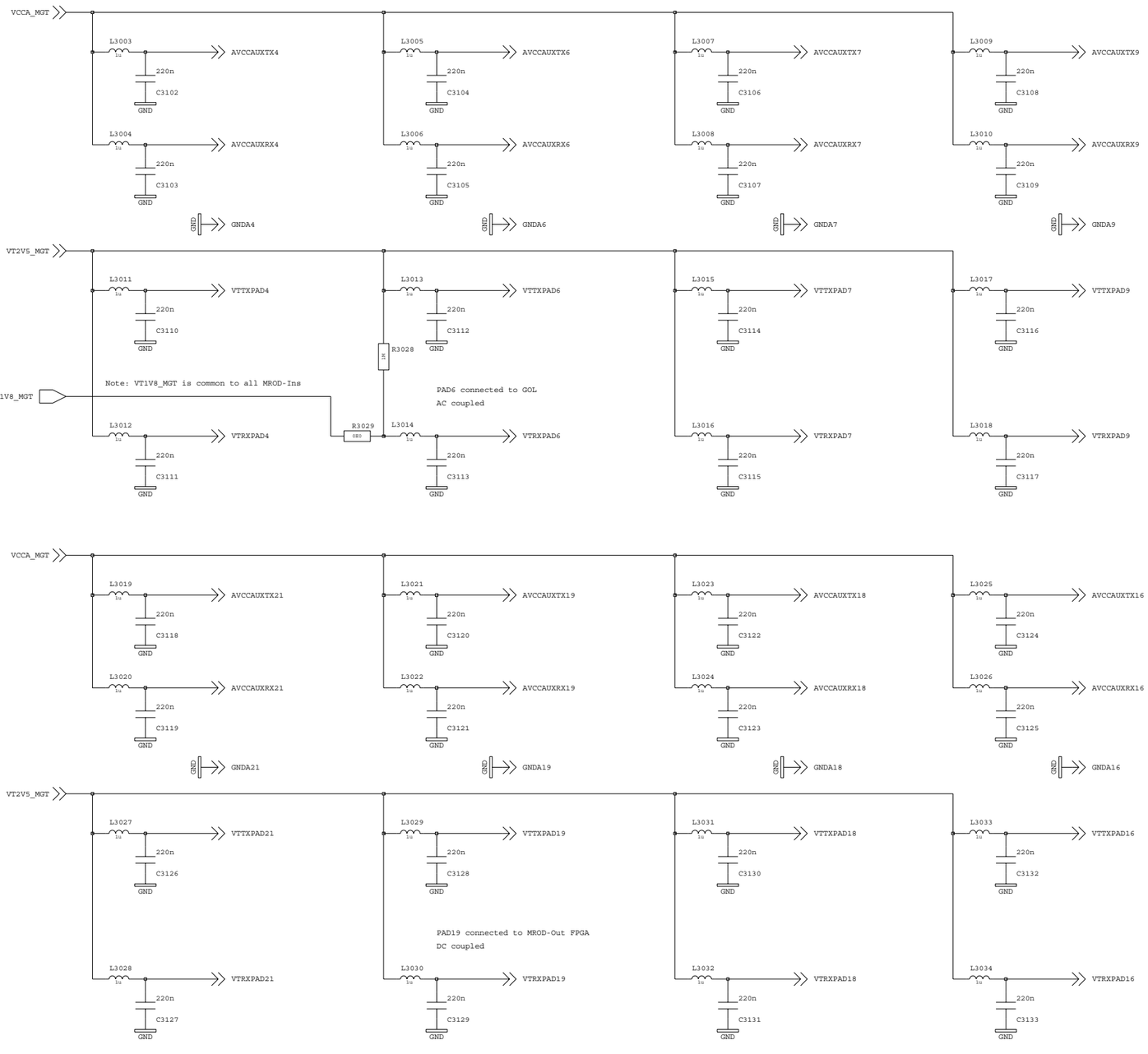
channel_in		Rev V2 2	
		Date 7 Feb 2006	
Input FPGA Power Supply Decoupling		Time 1:51:34 pm	
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
© RT-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 3 of 6	

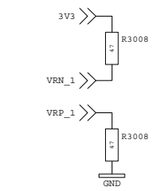
2V5 @ 1,5A



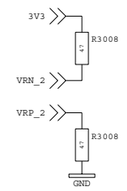
=> MGT Power (estimated 31 + 49 = 80 mA)

=> MGT TX (RX) Termination (estimated 11 mA)

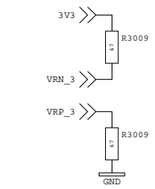




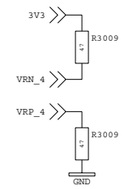
Series Termination for
Not (yet) used



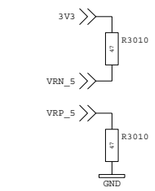
Series Termination for
Not (yet) used



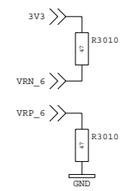
Series Termination for
Sharc Addressbus



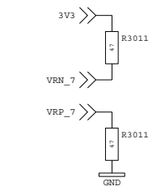
Series Termination for
Sharc Databus



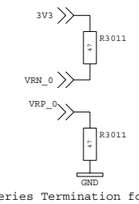
Series Termination for
General purpose



Series Termination for
SDRAM interface



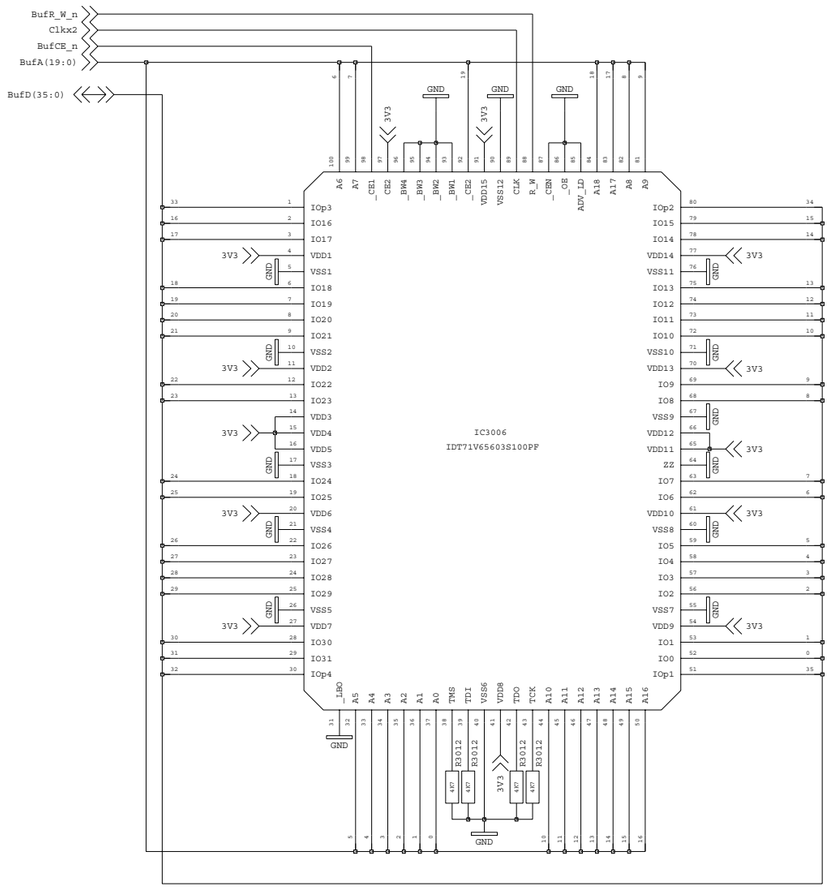
Series Termination for
Buffer Memory interface

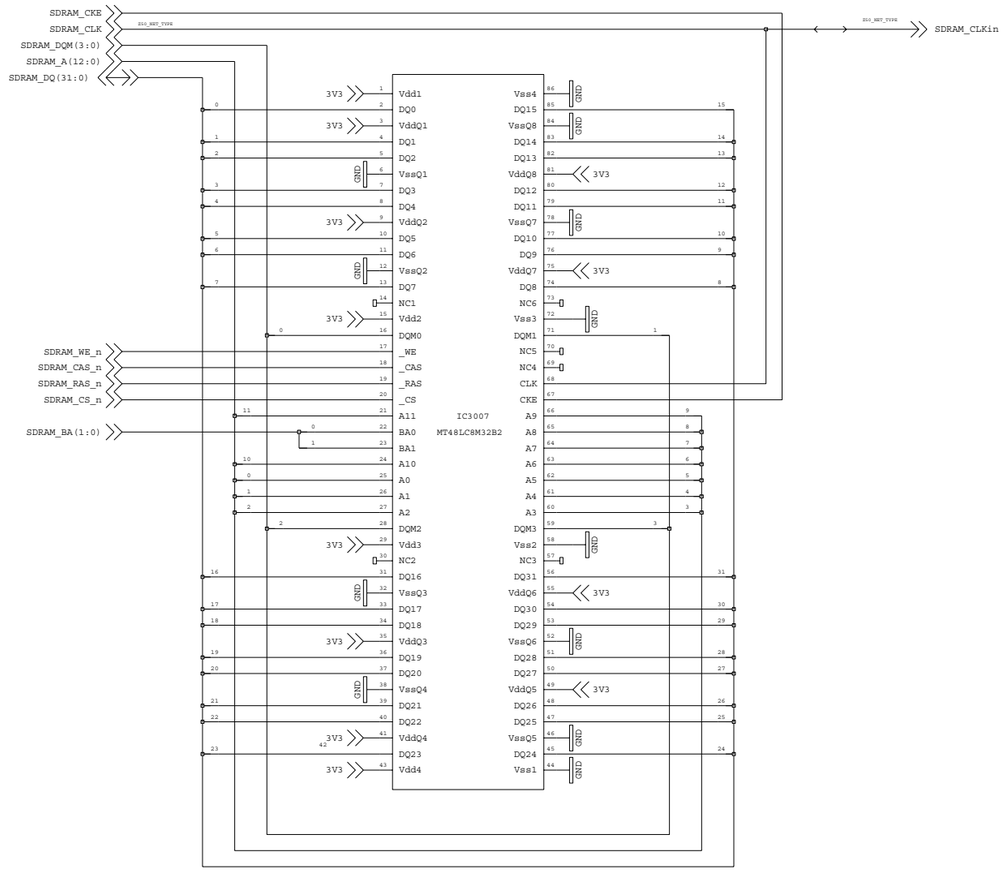


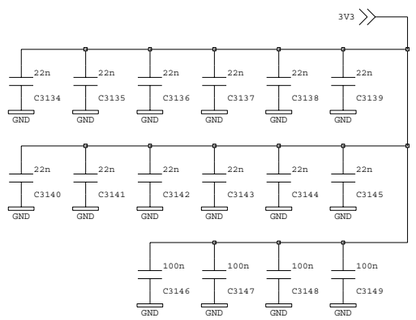
Series Termination for
General purpose

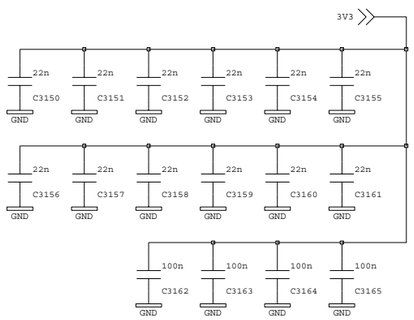
channel_in		Rev V2 2	
		Date 7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time 1:52:01 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
© ET-Nikhef Amsterdam		Page 4 of 6	

SDRAM_A(12) is not connected

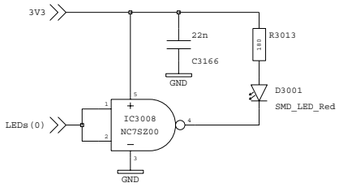


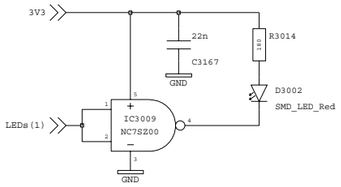


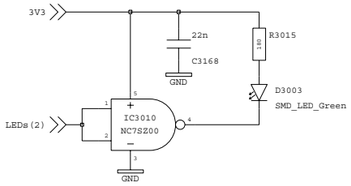


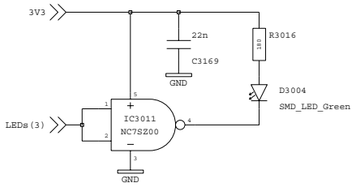


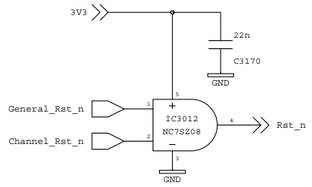
channel_in		Rev V2 2	
		Date 7 Feb 2006	
Buffer Memory (ZBT and SDRAM)		Time 1:52:29 pm	
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
ET-Nikhef Amsterdam		Page 5 of 6	



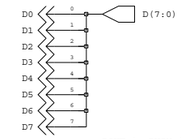




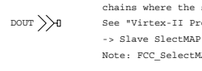




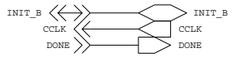
Fiducial3001 Fiducial3002

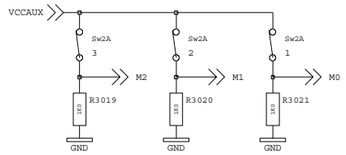


DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices.
See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SlectMAP programming Mode -> BUSY.
Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!



8 Input channels are loaded in parallel so there is no possibility for readback (RDWR_B = '0')
and each CS_B = '0'





M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

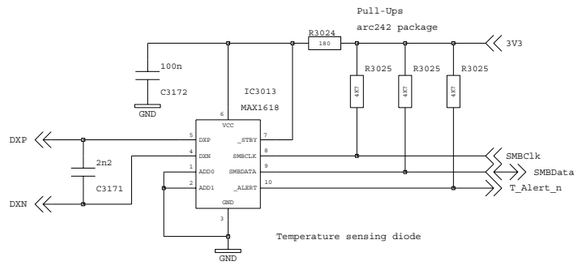
'On' = '1', 'Off' = '0'

Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.

FPGA Configuration Signals

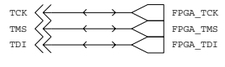
PWRDWN_B is unsupported (should be pulled high)

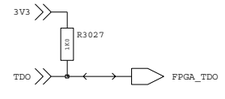
HSWAP_EN = '0' => User IOs have pull-up resistors during configuration



VBATT is decriptor key memory backup supply

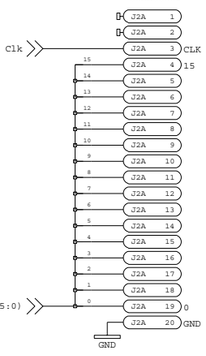
FPGA Control signals



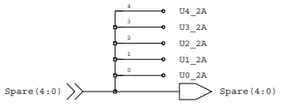


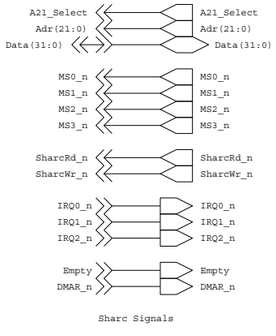
FPGA JTAG Signals

Optinal Test Connector



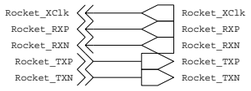
Testpoints force Spare lines to be accessible.



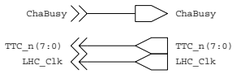


Sharc Signals

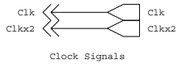
Input Channel ID bits



Frontend to Backend
Rocket IO Signals

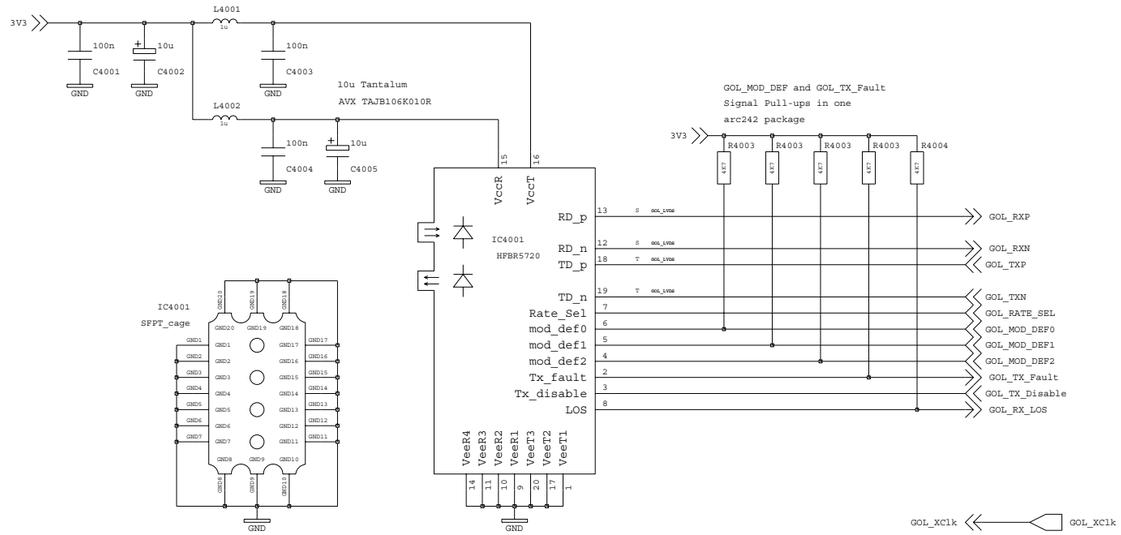


TTC Signals



Clock Signals

channel_in		Rev V2 2
		Date 7 Feb 2006
		Time 1:53:04 pm
		Name Ton van Reen
Input FPGA Auxiliary Connections		
Proj: MROD-X	Proj.No: 38405	Size A3 4 1 4 A
Peter Jansweijer	peterj@nikhef.nl	Dim 420 x 297 mm
NIKHEF © ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Page 6 of 6



channel_in		Rev V2 2	
GOL Input		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:50:33 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
ET-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 1 of 6	

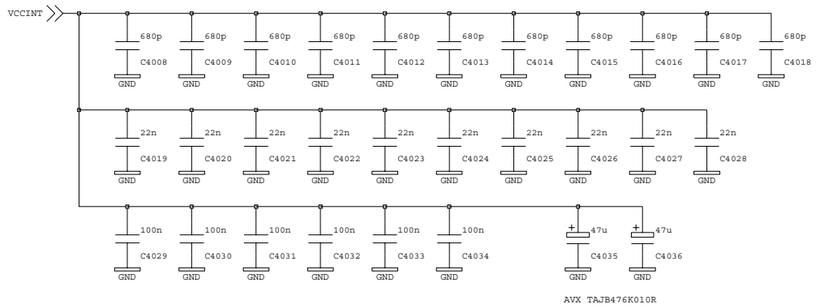
IC4004
XC2VP7FF896

	A2 VCCAUX	A3 VRP_2	A4	A5	A6	A7	A8	A9 GND	A10	A11	A12 VTRXPAD7	A13	A14 VTTXPAD7	A15 VCCAUX	A16 VCCAUX	A17 GOL_LVDS GOL_LVDS T DP_GOL_RX2B	A18 GOL_LVDS GOL_LVDS T DP_GOL_RX2B	A19 GOL_LVDS GOL_LVDS S DP_GOL_TX2B	A20 GOL_LVDS GOL_LVDS S DP_GOL_TX2B	A21	A22 GND	A23 LEDs(0)	A24	A25	A26	A27	A28 VRP_7	A29 VCCAUX	
B1 VCCAUX	B2 GND	B3 VRN_2	B4 AVCCAUXRX9	B5 VTRXPAD9	B6 AVCCAUXTX9	B7 VTTXPAD9	B8	B9	B10	B11 AVCCAUXRX7	B12	B13 AVCCAUXTX7	B14 VTTXPAD7	B15	B16 GOL_XClk	B17 AVCCAUXRX6	B18 VTRXPAD6	B19 AVCCAUXTX6	B20 VTTXPAD6	B21	B22 GND	B23 LEDs(1)	B24 AVCCAUXRX4	B25 VTRXPAD4	B26 AVCCAUXTX4	B27 VTTXPAD4	B28 VRN_7	B29 GND	B30 VCCAUX
C1	C2	C3 GND	C4	C5	C6 GNDA9	C7	C8	C9	C10	C11	C12 GNDA7	C13	C14 GND	C15	C16	C17 GND	C18 UpLED	C19 GNDA6	C20	C21	C22	C23 LEDs(2)	C24 LEDs(3)	C25 GNDA4	C26 BufA(6)	C27 BufA(7)	C28 GND	C29 BufCE_n	C30 BufA(19)
D1	D2	D3 GND	D4	D5 TDO	D6 GND	D7	D8	D9 GND	D10	D11	D12 GND	D13	D14	D15	D16 GOL_RX_LOS	D17 GOL_TX_Disable	D18 ErrLED	D19 GND	D20 GOL_MOD_DEF1	D21 GOL_MOD_DEF0	D22 GND	D23 ChaID(1)	D24 ChaID(0)	D25 DXN	D26 BufD(16)	D27 GND	D28 BufD(33)	D29	D30
E1	E2	E3	E4 GND	E5	E6 VRN_1	E7 VRP_1	E8	E9	E10	E11	E12	E13	E14	E15	E16	R17 GOL_TX_Fault	E18	E19	R20 GOL_MOD_DEF2	R21 GOL_RATE_SEL	E22	E23 ChaID(2)	E24 VRN_0	R25 VRP_0	E26 GND	E27	E28	E29	E30
F1	F2	F3	F4	F5 TDO	F6 GND	F7	F8	F9	F10	F11	F12	F13 GND	F14	F15	F16	F17	F18 GND	F19	F20	F21 TestCon(1)	F22 TestCon(0)	F23	F24	F25 GND	F26 TDI	F27	F28	F29	F30
G1	G2	G3	G4	G5	G6	G7 TCK	G8	G9	G10	G11	G12	G13	G14	G15	G16 Rst_n	G17	G18	G19 TestCon(6)	G20 TestCon(5)	G21 TestCon(4)	G22 TestCon(3)	G23 TestCon(2)	G24 PROG_B	G25 BufD(18)	G26 BufD(17)	G27	G28	G29	G30
H1 GND	H2	H3	H4	H5	H6	H7 VBATT	H8 TMS	H9	H10	H11	H12 TestCon(15)	H13	H14	H15	H16	H17	H18	H19 TestCon(7)	H20 T_Alert_n	H21 SMBData	H22 SMBClk	H23 HSWAP_EN	H24 DXP	H25	H26	H27	H28	H29 BufD(19)	H30 GND
J1	J2	J3	J4	J5	J6	J7	J8 TestCon(14)	J9 VCCO_2	J10 VCCO_1	J11 VCCO_1	J12 VCCO_1	J13 VCCO_1	J14	J15	J16	J17	J18 VCCO_0	J19 VCCO_0	J20 VCCO_0	J21 VCCO_0	J22 VCCO_7	J23 BufD(25)	J24 BufD(24)	J25	J26	J27 BufD(23)	J28 BufD(22)	J29 BufD(21)	J30 BufD(20)
K1	K2	K3	K4	K5	K6	K7	K8	K9 VCCO_2	K10 VCCO_1	K11 VCCO_1	K12 VCCO_1	K13 VCCO_1	K14 VCCO_1	K15 VCCO_1	K16 VCCO_0	K17 VCCO_0	K18 VCCO_0	K19 VCCO_0	K20 VCCO_0	K21 VCCO_0	K22 VCCO_7	K23	K24	K25 BufD(31)	K26 BufD(30)	K27 BufD(29)	K28 BufD(28)	K29 BufD(27)	K30 BufD(26)
L1	L2	L3 GND	L4	L5	L6 GND	L7	L8	L9 VCCO_2	L10 VCCO_2	L11 GND	L12 VCCINT	L13 VCCINT	L14 VCCINT	L15 VCCINT	L16 VCCINT	L17 VCCINT	L18 VCCINT	L19 VCCINT	L20 GND	L21 VCCO_7	L22 VCCO_7	L23	L24	L25 GND	L26 BufA(3)	L27 BufA(4)	L28 GND	L29 BufA(5)	L30 BufD(32)
M1	M2	M3	M4	M5	M6	M7	M8	M9 VCCO_2	M10 VCCO_2	M11 VCCINT	M12 GND	M13 GND	M14 GND	M15 GND	M16 GND	M17 GND	M18 GND	M19 GND	M20 VCCINT	M21 VCCO_7	M22 VCCO_7	M23 BufA(14)	M24 BufA(13)	M25 BufA(12)	M26 BufA(11)	M27 BufA(10)	M28 BufA(0)	M29 BufA(1)	M30 BufA(2)
N1	N2	N3	N4	N5	N6	N7	N8	N9 VCCO_2	N10 VCCO_2	N11 VCCINT	N12 GND	N13 GND	N14 GND	N15 GND	N16 GND	N17 GND	N18 GND	N19 GND	N20 VCCINT	N21 VCCO_7	N22 VCCO_7	N23 BufD(4)	N24 BufD(3)	N25 BufD(2)	N26 BufD(1)	N27 BufD(0)	N28 BufD(35)	N29 BufA(16)	N30 BufA(15)
P1	P2	P3	P4	P5	P6 GND	P7	P8	P9	P10 VCCO_2	P11 VCCINT	P12 GND	P13 GND	P14 GND	P15 GND	P16 GND	P17 GND	P18 GND	P19 GND	P20 VCCINT	P21 VCCO_7	P22 BufD(12)	P23 BufD(11)	P24 BufD(10)	P25 GND	P26 BufD(9)	P27 BufD(8)	P28 BufD(7)	P29 BufD(6)	P30 BufD(5)
R1 VCCAUX	R2	R3	R4	R5	R6	R7	R8	R9	R10 VCCO_2	R11 VCCINT	R12 GND	R13 GND	R14 GND	R15 GND	R16 GND	R17 GND	R18 GND	R19 GND	R20 VCCINT	R21 VCCO_7	R22 BufA(18)	R23 BufA(17)	R24 BufA(8)	R25 BufA(9)	R26 BufD(34)	R27 BufD(15)	R28 BufD(14)	R29 BufD(13)	R30 VCCAUX
T1 VCCAUX	T2	T3	T4	T5 Spare(4)	T6 Spare(3)	T7 Spare(2)	T8 Spare(1)	T9 Spare(0)	T10 VCCO_3	T11 VCCINT	T12 GND	T13 GND	T14 GND	T15 GND	T16 GND	T17 GND	T18 GND	T19 GND	T20 VCCINT	T21 VCCO_6	T22 SDRAM_DQ(6)	T23 SDRAM_DQ(5)	T24 SDRAM_DQ(4)	T25 SDRAM_DQ(3)	T26 SDRAM_DQ(2)	T27 SDRAM_DQ(1)	T28 SDRAM_DQ(0)	T29 BufR_W_n	T30 VCCAUX
U1	U2	U3	U4	U5	U6 GND	U7	U8	U9	U10 VCCO_3	U11 VCCINT	U12 GND	U13 GND	U14 GND	U15 GND	U16 GND	U17 GND	U18 GND	U19 GND	U20 VCCINT	U21 VCCO_6	U22 SDRAM_BA(0)	U23 SDRAM_A(11)	U24 SDRAM_CS_n	U25 GND	U26 SDRAM_RAS_n	U27 SDRAM_CAS_n	U28 SDRAM_WE_n	U29 SDRAM_DQM(0)	U30 SDRAM_DQ(7)
V1 A21_Select	V2	V3	V4	V5	V6	V7	V8	V9 VCCO_3	V10 VCCO_3	V11 VCCINT	V12 GND	V13 GND	V14 GND	V15 GND	V16 GND	V17 GND	V18 GND	V19 GND	V20 VCCINT	V21 VCCO_6	V22 VCCO_6	V23 SDRAM_DQ(17)	V24 SDRAM_DQ(16)	V25 SDRAM_DQM(2)	V26 SDRAM_A(2)	V27 SDRAM_A(1)	V28 SDRAM_A(0)	V29 SDRAM_A(10)	V30 SDRAM_BA(1)
W1 Adr(21)	W2 MS0_n	W3 MS1_n	W4 MS2_n	W5 MS3_n	W6 DMAR_n	W7	W8	W9 VCCO_3	W10 VCCO_3	W11 VCCINT	W12 GND	W13 GND	W14 GND	W15 GND	W16 GND	W17 GND	W18 GND	W19 GND	W20 VCCINT	W21 VCCO_6	W22 VCCO_6	W23 SDRAM_DQ(25)	W24 SDRAM_DQ(24)	W25 SDRAM_DQ(23)	W26 SDRAM_DQ(22)	W27 SDRAM_DQ(21)	W28 SDRAM_DQ(20)	W29 SDRAM_DQ(19)	W30 SDRAM_DQ(18)
Y1 Adr(17)	Y2 Adr(18)	Y3 GND	Y4 Adr(19)	Y5 Adr(20)	Y6 GND	Y7	Y8	Y9 VCCO_3	Y10 VCCO_3	Y11 GND	Y12 VCCINT	Y13 VCCINT	Y14 VCCINT	Y15 VCCINT	Y16 VCCINT	Y17 VCCINT	Y18 VCCINT	Y19 VCCINT	Y20 GND	Y21 VCCO_6	Y22 VCCO_6	Y23	Y24	Y25 GND	Y26 SDRAM_DQ(29)	Y27 SDRAM_DQ(28)	Y28 GND	Y29 SDRAM_DQ(27)	Y30 SDRAM_DQ(26)
AA1 Adr(11)	AA2 Adr(12)	AA3 Adr(13)	AA4 Adr(14)	AA5 Adr(15)	AA6 Adr(16)	AA7	AA8	AA9 VCCO_3	AA10 VCCO_4	AA11 VCCO_4	AA12 VCCO_4	AA13 VCCO_4	AA14 VCCO_4	AA15 VCCO_4	AA16 VCCO_5	AA17 VCCO_5	AA18 VCCO_5	AA19 VCCO_5	AA20 VCCO_5	AA21 VCCO_5	AA22 VCCO_6	AA23	AA24	AA25 SDRAM_A(5)	AA26 SDRAM_A(4)	AA27 SDRAM_A(3)	AA28 SDRAM_DQM(3)	AA29 SDRAM_DQ(31)	AA30 SDRAM_DQ(30)
AB1 Adr(7)	AB2 Adr(8)	AB3 Adr(9)	AB4 Adr(10)	AB5	AB6	AB7	AB8	AB9 VCCO_3	AB10 VCCO_4	AB11 VCCO_4	AB12 VCCO_4	AB13 VCCO_4	AB14	AB15 Data(3)	AB16 IRQ2_n	AB17	AB18 VCCO_5	AB19 VCCO_5	AB20 VCCO_5	AB21 VCCO_5	AB22 VCCO_6	AB23	AB24	AB25	AB26	AB27 SDRAM_A(9)	AB28 SDRAM_A(8)	AB29 SDRAM_A(7)	AB30 SDRAM_A(6)
AC1 GND	AC2 Adr(4)	AC3 Adr(5)	AC4 Adr(6)	AC5	AC6	AC7 CCLK	AC8 DONE	AC9 D0	AC10 Data(16)	AC11 Data(11)	AC12 Data(9)	AC13	AC14	AC15 Data(2)	AC16 IRQ1_n	AC17	AC18	AC19 TestCon(8)	AC20 TestCon(9)	AC21 TestCon(10)	AC22 D7	AC23 M2	AC24 M1	AC25	AC26	AC27 SDRAM_DQM(1)	AC28 SDRAM_A(12)	AC29 SDRAM_CKE	AC30 GND
AD1	AD2	AD3	AD4	AD5 Adr(2)	AD6 Adr(3)	AD7 PWRDWN_B	AD8	AD9 D1	AD10 Data(15)	AD11 Data(10)	AD12 Data(8)	AD13	AD14 Data(7)	AD15 Data(1)	AD16 IRQ0_n	AD17	AD18	AD19 TestCon(11)	AD20 TestCon(12)	AD21 TestCon(13)	AD22 D6	AD23	AD24 M0	AD25 SDRAM_DQ(9)	AD26 SDRAM_DQ(8)	AD27	AD28	AD29	AD30
AE1	AE2	AE3	AE4	AE5	AE6 GND	AE7 Data(25)	AE8 Data(24)	AE9 Data(20)	AE10 Data(14)	AE11	AE12	AE13 GND	AE14 Data(6)	AE15 Data(0)	AE16 Empty	AE17	AE18 GND	AE19	AE20	AE21	AE22	AE23	AE24	AE25 GND	AE26	AE27	AE28	AE29	AE30
AF1	AF2	AF3	AF4	AF5 GND	AF6	AF7 INIT_B	AF8 Data(23)	AF9 Data(19)	AF10 Data(13)	AF11	AF12	AF13	AF14 Data(5)	AF15 SDRAM_CLKin	AF16 SDRAM_CLK	AF17	AF18	AF19	AF20	AF21 TTC_n(7)	AF22 TTC_n(6)	AF23 TTC_n(4)	AF24 RDWR_B	AF25	AF26 GND	AF27	AF28	AF29	AF30
AG1 Data(30)	AG2 Data(31)	AG3 Adr(0)	AG4 GND	AG5 Adr(1)	AG6 DOUT	AG7 D2	AG8 VRP_4	AG9 GND	AG10 Data(12)	AG11	AG12 GND	AG13	AG14 Data(4)	AG15 SharcWr_n	AG16 LHC_Clk	AG17 ChaBusy	AG18	AG19 GND	AG20	AG21 TTC_n(5)	AG22 GND	AG23 VRN_5	AG24 D5	AG25 CS_B	AG26 SDRAM_DQ(13)	AG27 GND	AG28 SDRAM_DQ(12)	AG29 SDRAM_DQ(11)	AG30 SDRAM_DQ(10)
AH1 Data(26)	AH2 Data(27)	AH3 GND	AH4 Data(28)	AH5 Data(29)	AH6 GNDA16	AH7 D3	AH8 VRN_4	AH9 Data(18)	AH10	AH11	AH12 GNDA18	AH13	AH14 GND	AH15 SharcRd_n	AH16 Clk	AH17 GND	AH18	AH19 GNDA19	AH20	AH21	AH22 TTC_n(3)	AH23 VRP_5	AH24 D4	AH25 GNDA21	AH26	AH27	AH28 GND	AH29 SDRAM_DQ(15)	AH30 SDRAM_DQ(14)
AJ1 VCCAUX	AJ2 GND	AJ3 VRP_3	AJ4 AVCCAUXRX16	AJ5 VTRXPAD16	AJ6 AVCCAUXTX16	AJ7 VTTXPAD16	AJ8 Data(22)	AJ9 Data(17)	AJ10	AJ11 AVCCAUXRX18	AJ12 VTRXPAD18	AJ13 AVCCAUXTX18	AJ14 VTTXPAD18	AJ15 Rocket_XC1k	AJ16 Clkx2	AJ17 AVCCAUXRX19	AJ18 VTRXPAD19	AJ19 AVCCAUXTX19	AJ20 VTTXPAD19	AJ21	AJ22 TTC_n(2)	AJ23 TTC_n(1)	AJ24 AVCCAUXRX21	AJ25 VTRXPAD21	AJ26 AVCCAUXTX21	AJ27 VTTXPAD21	AJ28 VRP_6	AJ29 GND	AJ30 VCCAUX
	AK2 VCCAUX	AK3 VRN_3	AK4	AK5	AK6	AK7	AK8 Data(21)	AK9 GND	AK10	AK11	AK12	AK13	AK14	AK15 VCCAUX	AK16 VCCAUX	AK17 ROCKET_LVDS T Rocket_RXN	AK18 ROCKET_LVDS T Rocket_RXP	AK19 ROCKET_LVDS S Rocket_TXP	AK20 ROCKET_LVDS S Rocket_TXN	AK21	AK22 GND	AK23 TTC_n(0)	AK24	AK25	AK26	AK27	AK28 VRN_6	AK29 VCCAUX	

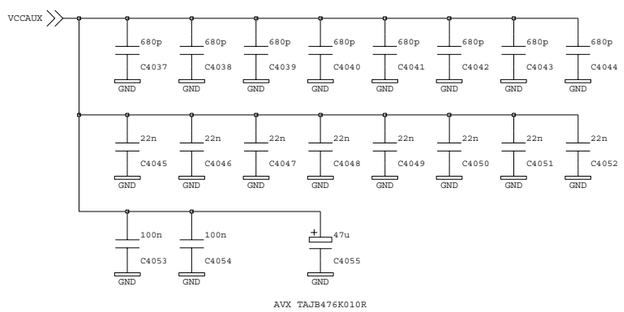
Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

channel_in	Rev V2 2
Input FPGA	Date 7 Feb 2006
Proj: MROD-X	Time 1:50:53 pm
Peter Jansweijer	Proj.No: 38405
NIKHEF	Name tonvr
ET-Nikhef Amsterdam	Size A3 4 1 4 A
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
peterj@nikhef.nl	Page 2 of 6

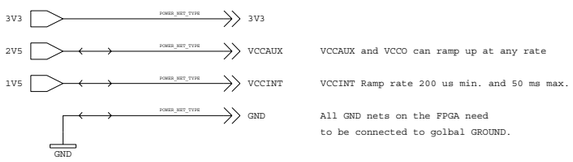
XC2VP7/20 VCCINT Decoupling Capacitors
Min. Power-On Current XC2VP20
IccINT = 600 mA



XC2VP7/20 VCCAUX Decoupling Capacitors
Min. Power-On Current XC2VP20
IccAUX = 250 mA (min)



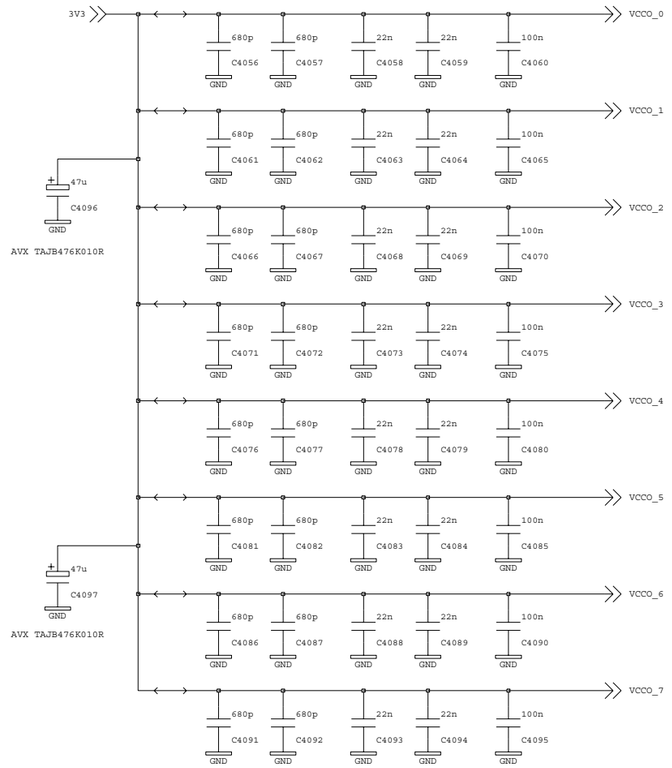
Power Inputs
For Xilinx Virtex-II Pro, power supplies
can be turned on in any sequence.



VCCAUX and VCCO can ramp up at any rate

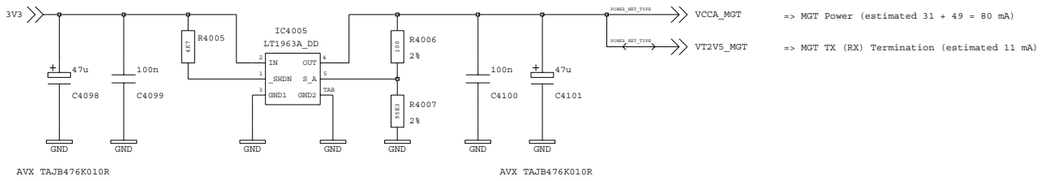
VCCINT Ramp rate 200 us min. and 50 ms max.

All GND nets on the FPGA need
to be connected to golbal GROUND.



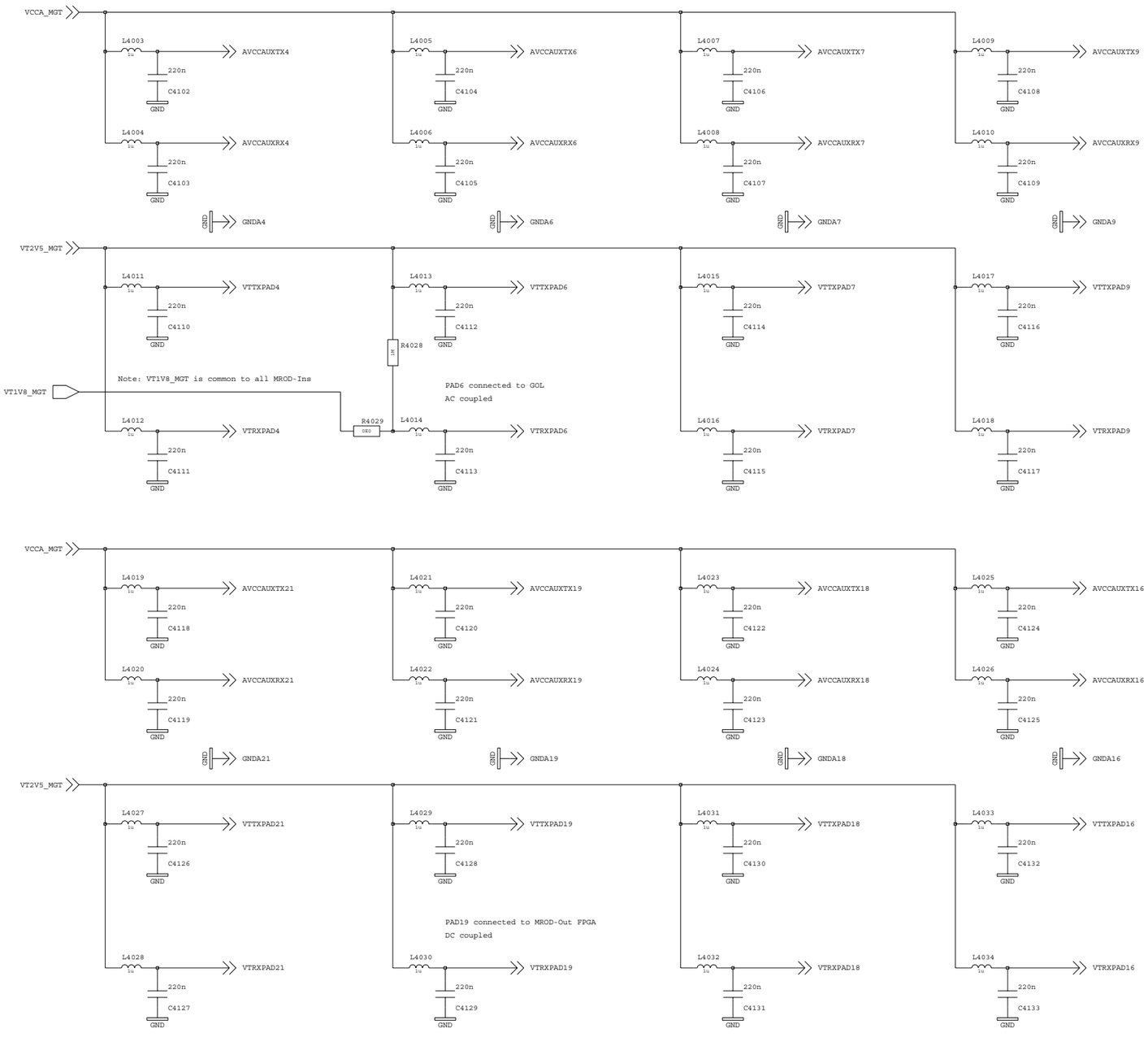
channel_in		Rev V2 2	
		Date 7 Feb 2006	
Input FPGA Power Supply Decoupling		Time 1:51:34 pm	
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
		Page 3 of 6	

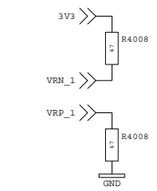
2V5 @ 1,5A



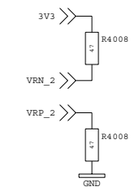
=> MGT Power (estimated 31 + 49 = 80 mA)

=> MGT TX (RX) Termination (estimated 11 mA)

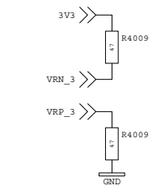




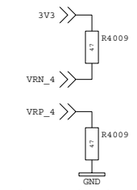
Series Termination for
Not (yet) used



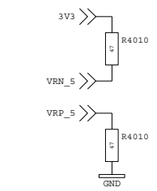
Series Termination for
Not (yet) used



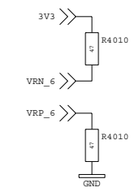
Series Termination for
Sharc Addressbus



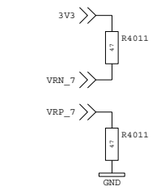
Series Termination for
Sharc Databus



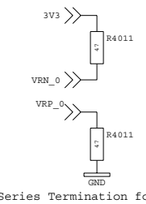
Series Termination for
General purpose



Series Termination for
SDRAM interface



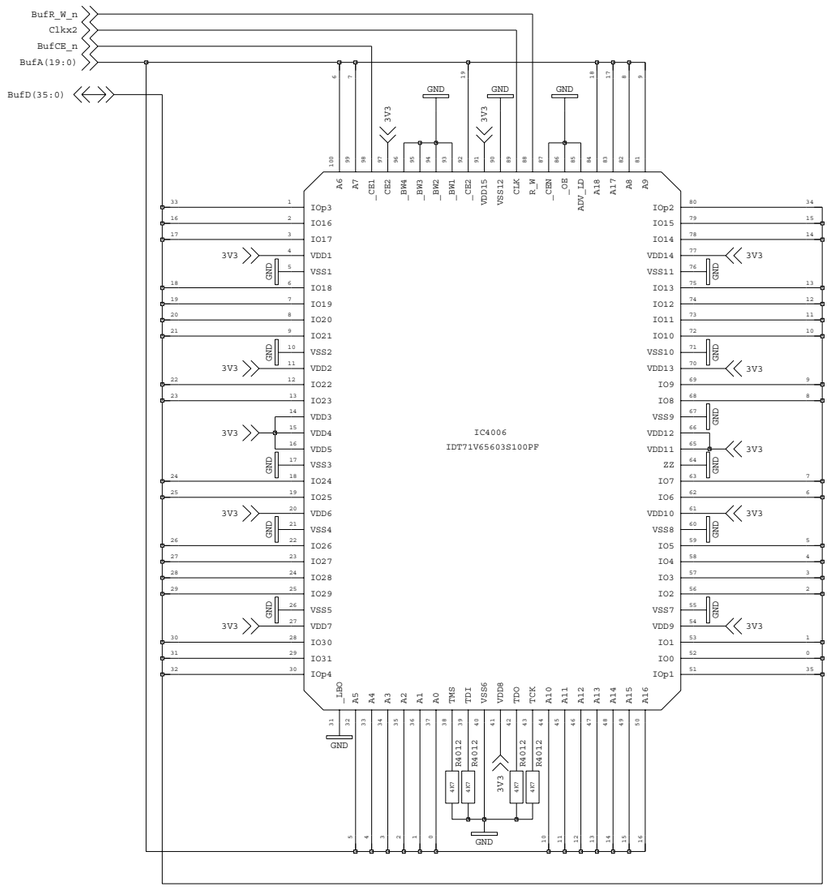
Series Termination for
Buffer Memory interface

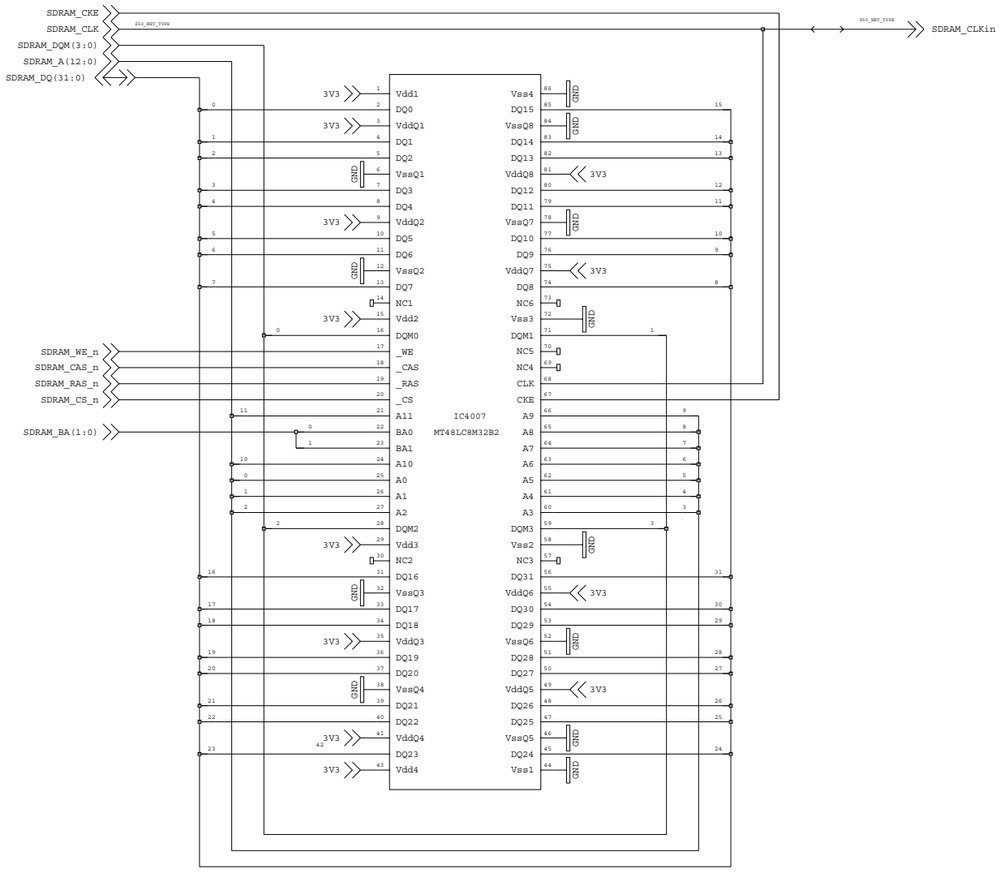


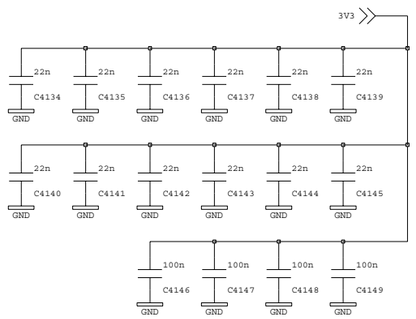
Series Termination for
General purpose

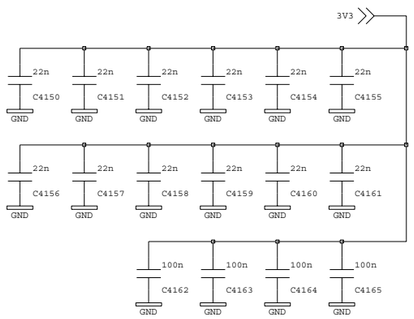
channel_in		Rev V2 2	
		Date 7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time 1:52:01 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
		Page 4 of 6	

SDRAM_A(12) is not connected

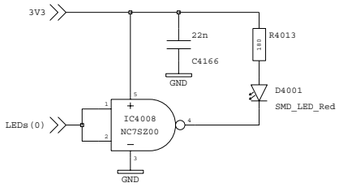


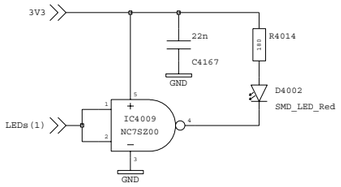


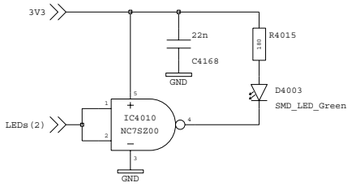


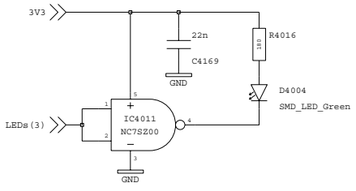


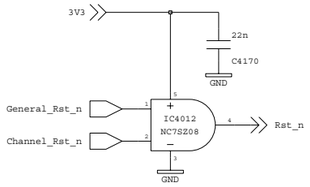
channel_in		Rev	V2 2
		Date	7 Feb 2006
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm
Proj: MROD-X	Proj.No: 38405	Name	Ton van Reen
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size	A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim	420 x 297 mm
		Page	5 of 6



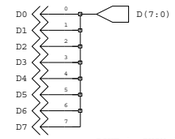




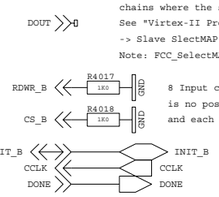




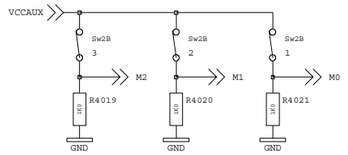
Fiducial4001 Fiducial4002



DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices.
See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SlectMAP programming Mode -> BUSY.
Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!



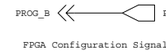
8 Input channels are loaded in parallel so there is no possibility for readback (RDWR_B = '0') and each CS_B = '0'



M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.



FPGA Configuration Signals

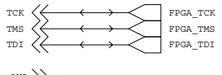
PWRDWN_B is unsupported (should be pulled high)

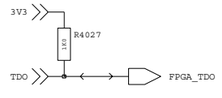
HSWAP_EN = '0' => User IOs have pull-up resistors during configuration

Temperature sensing diode

VBATT is decriptor key memory backup supply

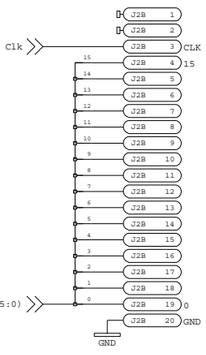
FPGA Control signals



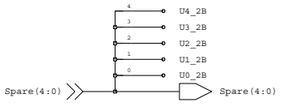


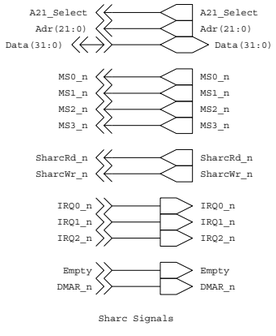
FPGA JTAG Signals

Optinal Test Connector



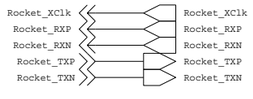
Testpoints force Spare lines to be accessible.





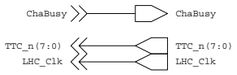
Sharc Signals

Input Channel ID bits

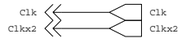


Frontend to Backend

Rocket IO Signals



TTC Signals



Clock Signals

channel_in

Input FPGA Auxiliary Connections

Proj: MROD-X	Proj.No: 38405
Peter Jansweijer	peterj@nikhef.nl

NIKHEF
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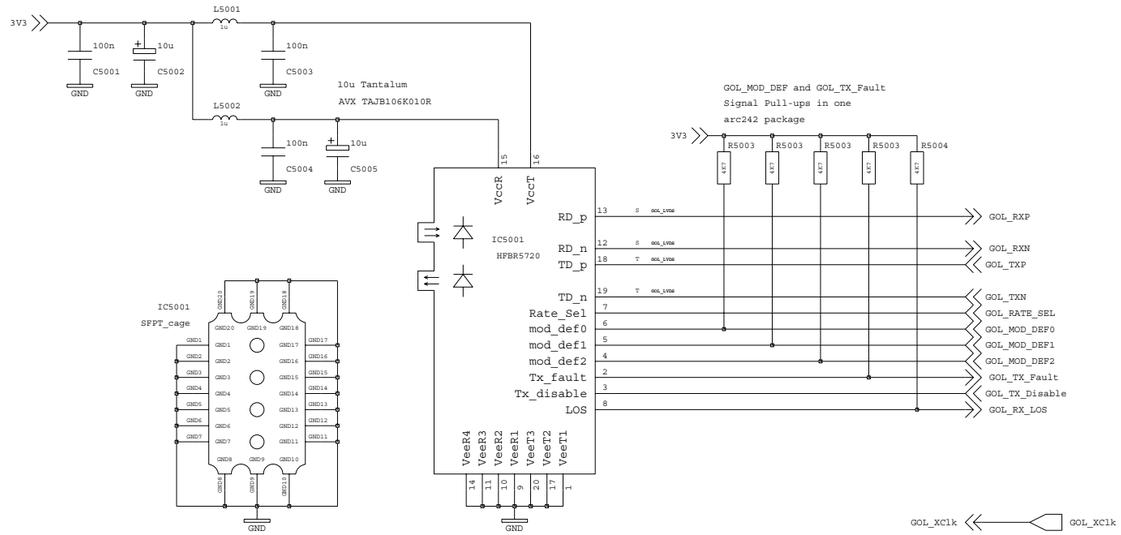
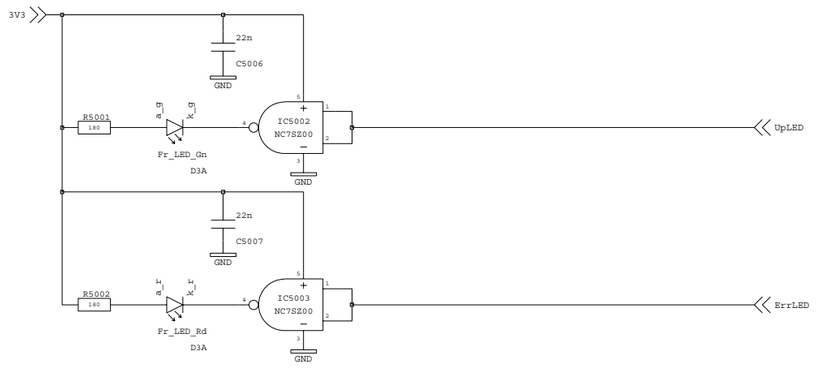
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND

Rev	V2 2
Date	7 Feb 2006
Time	1:53:04 pm
Name	Ton van Reen
Size	A3 4 1 4 A
Dim	420 x 297 mm
Page	6 of 6





channel_in		Rev V2 2	
		Date 7 Feb 2006	
GOL Input		Time 1:50:33 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 1 of 6	

IC5004
XC2VP7FF896

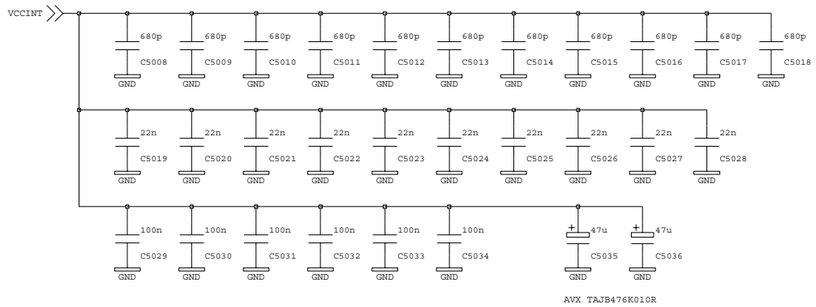
	A2 VCCAUX	A3 VRP_2	A4	A5	A6	A7	A8	A9 GND	A10	A11	A12	A13	A14	A15 VCCAUX	A16 VCCAUX	A17 GOL_LVDS gol_lvds T DP_GOL_RX3A	A18 GOL_LVDS gol_lvds T DP_GOL_RX3A	A19 GOL_LVDS gol_lvds S DP_GOL_TX3A	A20 GOL_LVDS gol_lvds S DP_GOL_TX3A	A21	A22 GND	A23 LEDs(0)	A24	A25	A26	A27	A28 VRP_7	A29 VCCAUX	
B1 VCCAUX	B2 GND	B3 VRN_2	B4 AVCCAUXRX9	B5 VTRXPAD9	B6 AVCCAUXTX9	B7 VTTXPAD9	B8	B9	B10	B11 AVCCAUXRX7	B12 VTRXPAD7	B13 AVCCAUXTX7	B14 VTTXPAD7	B15	B16 GOL_XClk	B17 AVCCAUXRX6	B18 VTRXPAD6	B19 AVCCAUXTX6	B20 VTTXPAD6	B21	B22	B23 LEDs(1)	B24 AVCCAUXRX4	B25 VTRXPAD4	B26 AVCCAUXTX4	B27 VTTXPAD4	B28 VRN_7	B29 GND	B30 VCCAUX
C1	C2	C3 GND	C4	C5	C6 GNDA9	C7	C8	C9	C10	C11	C12 GNDA7	C13	C14 GND	C15	C16	C17 GND	C18 UpLED	C19 GNDA6	C20	C21	C22	C23 LEDs(2)	C24 LEDs(3)	C25 GNDA4	C26 BufA(6)	C27 BufA(7)	C28 GND	C29 BufCE_n	C30 BufA(19)
D1	D2	D3 GND	D4	D5	D6	D7	D8	D9 GND	D10	D11	D12 GND	D13	D14	D15	D16 GOL_RX_LOS	D17 GOL_TX_Disable	D18 ErrLED	D19 GND	D20 GOL_MOD_DEF1	D21 GOL_MOD_DEF0	D22 GND	D23 ChaID(1)	D24 ChaID(0)	D25 DXN	D26 BufD(16)	D27 GND	D28 BufD(33)	D29	D30
E1	E2	E3	E4 GND	E5	E6 VRN_1	E7 VRP_1	E8	E9	E10	E11	E12	E13	E14	E15	E16	R17 GOL_TX_Fault	E18	E19	R20 GOL_MOD_DEF2	R21 GOL_RATE_SEL	E22	E23 ChaID(2)	E24 VRN_0	R25 VRP_0	E26 GND	E27	E28	E29	E30
F1	F2	F3	F4	F5 TDO	F6 GND	F7	F8	F9	F10	F11	F12	F13 GND	F14	F15	F16	F17	F18 GND	F19	F20	F21 TestCon(1)	F22 TestCon(0)	F23	F24	F25 GND	F26 TDI	F27	F28	F29	F30
G1	G2	G3	G4	G5	G6	G7 TCK	G8	G9	G10	G11	G12	G13	G14	G15	G16 Rst_n	G17	G18	G19 TestCon(6)	G20 TestCon(5)	G21 TestCon(4)	G22 TestCon(3)	G23 TestCon(2)	G24 PROG_B	G25 BufD(18)	G26 BufD(17)	G27	G28	G29	G30
H1 GND	H2	H3	H4	H5	H6	H7 VBATT	H8 TMS	H9	H10	H11	H12 TestCon(15)	H13	H14	H15	H16	H17	H18	H19 TestCon(7)	H20 T_Alert_n	H21 SMBData	H22 SMBClk	H23 HSWAP_EN	H24 DXP	H25	H26	H27	H28	H29 BufD(19)	H30 GND
J1	J2	J3	J4	J5	J6	J7	J8 TestCon(14)	J9 VCCO_2	J10 VCCO_1	J11 VCCO_1	J12 VCCO_1	J13 VCCO_1	J14	J15	J16	J17	J18 VCCO_0	J19 VCCO_0	J20 VCCO_0	J21 VCCO_0	J22 VCCO_7	J23 BufD(25)	J24 BufD(24)	J25	J26	J27 BufD(23)	J28 BufD(22)	J29 BufD(21)	J30 BufD(20)
K1	K2	K3	K4	K5	K6	K7	K8	K9 VCCO_2	K10 VCCO_1	K11 VCCO_1	K12 VCCO_1	K13 VCCO_1	K14 VCCO_1	K15 VCCO_1	K16 VCCO_0	K17 VCCO_0	K18 VCCO_0	K19 VCCO_0	K20 VCCO_0	K21 VCCO_0	K22 VCCO_7	K23	K24	K25 BufD(31)	K26 BufD(30)	K27 BufD(29)	K28 BufD(28)	K29 BufD(27)	K30 BufD(26)
L1	L2	L3 GND	L4	L5	L6 GND	L7	L8	L9 VCCO_2	L10 VCCO_2	L11 GND	L12 VCCINT	L13 VCCINT	L14 VCCINT	L15 VCCINT	L16 VCCINT	L17 VCCINT	L18 VCCINT	L19 VCCINT	L20 GND	L21 VCCO_7	L22 VCCO_7	L23	L24	L25 GND	L26 BufA(3)	L27 BufA(4)	L28 GND	L29 BufA(5)	L30 BufD(32)
M1	M2	M3	M4	M5	M6	M7	M8	M9 VCCO_2	M10 VCCO_2	M11 VCCINT	M12 GND	M13 GND	M14 GND	M15 GND	M16 GND	M17 GND	M18 GND	M19 GND	M20 VCCINT	M21 VCCO_7	M22 VCCO_7	M23 BufA(14)	M24 BufA(13)	M25 BufA(12)	M26 BufA(11)	M27 BufA(10)	M28 BufA(0)	M29 BufA(1)	M30 BufA(2)
N1	N2	N3	N4	N5	N6	N7	N8	N9 VCCO_2	N10 VCCO_2	N11 VCCINT	N12 GND	N13 GND	N14 GND	N15 GND	N16 GND	N17 GND	N18 GND	N19 GND	N20 VCCINT	N21 VCCO_7	N22 VCCO_7	N23 BufD(4)	N24 BufD(3)	N25 BufD(2)	N26 BufD(1)	N27 BufD(0)	N28 BufD(35)	N29 BufA(16)	N30 BufA(15)
P1	P2	P3	P4	P5	P6 GND	P7	P8	P9	P10 VCCO_2	P11 VCCINT	P12 GND	P13 GND	P14 GND	P15 GND	P16 GND	P17 GND	P18 GND	P19 GND	P20 VCCINT	P21 VCCO_7	P22 BufD(12)	P23 BufD(11)	P24 BufD(10)	P25 GND	P26 BufD(9)	P27 BufD(8)	P28 BufD(7)	P29 BufD(6)	P30 BufD(5)
R1 VCCAUX	R2	R3	R4	R5	R6	R7	R8	R9	R10 VCCO_2	R11 VCCINT	R12 GND	R13 GND	R14 GND	R15 GND	R16 GND	R17 GND	R18 GND	R19 GND	R20 VCCINT	R21 VCCO_7	R22 BufA(18)	R23 BufA(17)	R24 BufA(8)	R25 BufA(9)	R26 BufD(34)	R27 BufD(15)	R28 BufD(14)	R29 BufD(13)	R30 VCCAUX
T1 VCCAUX	T2	T3	T4	T5 Spare(4)	T6 Spare(3)	T7 Spare(2)	T8 Spare(1)	T9 Spare(0)	T10 VCCO_3	T11 VCCINT	T12 GND	T13 GND	T14 GND	T15 GND	T16 GND	T17 GND	T18 GND	T19 GND	T20 VCCINT	T21 VCCO_6	T22 SDRAM_DQ(6)	T23 SDRAM_DQ(5)	T24 SDRAM_DQ(4)	T25 SDRAM_DQ(3)	T26 SDRAM_DQ(2)	T27 SDRAM_DQ(1)	T28 SDRAM_DQ(0)	T29 BufR_W_n	T30 VCCAUX
U1	U2	U3	U4	U5	U6 GND	U7	U8	U9	U10 VCCO_3	U11 VCCINT	U12 GND	U13 GND	U14 GND	U15 GND	U16 GND	U17 GND	U18 GND	U19 GND	U20 VCCINT	U21 VCCO_6	U22 SDRAM_BA(0)	U23 SDRAM_A(11)	U24 SDRAM_CS_n	U25 GND	U26 SDRAM_RAS_n	U27 SDRAM_CAS_n	U28 SDRAM_WE_n	U29 SDRAM_DQM(0)	U30 SDRAM_DQ(7)
V1 A21_Select	V2	V3	V4	V5	V6	V7	V8	V9 VCCO_3	V10 VCCO_3	V11 VCCINT	V12 GND	V13 GND	V14 GND	V15 GND	V16 GND	V17 GND	V18 GND	V19 GND	V20 VCCINT	V21 VCCO_6	V22 VCCO_6	V23 SDRAM_DQ(17)	V24 SDRAM_DQ(16)	V25 SDRAM_DQM(2)	V26 SDRAM_A(2)	V27 SDRAM_A(1)	V28 SDRAM_A(0)	V29 SDRAM_A(10)	V30 SDRAM_BA(1)
W1 Adr(21)	W2 MS0_n	W3 MS1_n	W4 MS2_n	W5 MS3_n	W6 DMAR_n	W7	W8	W9 VCCO_3	W10 VCCO_3	W11 VCCINT	W12 GND	W13 GND	W14 GND	W15 GND	W16 GND	W17 GND	W18 GND	W19 GND	W20 VCCINT	W21 VCCO_6	W22 VCCO_6	W23 SDRAM_DQ(25)	W24 SDRAM_DQ(24)	W25 SDRAM_DQM(3)	W26 SDRAM_DQ(22)	W27 SDRAM_DQ(21)	W28 SDRAM_DQ(20)	W29 SDRAM_DQ(19)	W30 SDRAM_DQ(18)
Y1 Adr(17)	Y2 Adr(18)	Y3 GND	Y4 Adr(19)	Y5 Adr(20)	Y6 GND	Y7	Y8	Y9 VCCO_3	Y10 VCCO_3	Y11 GND	Y12 VCCINT	Y13 VCCINT	Y14 VCCINT	Y15 VCCINT	Y16 VCCINT	Y17 VCCINT	Y18 VCCINT	Y19 VCCINT	Y20 GND	Y21 VCCO_6	Y22 VCCO_6	Y23	Y24	Y25 GND	Y26 SDRAM_DQ(29)	Y27 SDRAM_DQ(28)	Y28 GND	Y29 SDRAM_DQ(27)	Y30 SDRAM_DQ(26)
AA1 Adr(11)	AA2 Adr(12)	AA3 Adr(13)	AA4 Adr(14)	AA5 Adr(15)	AA6 Adr(16)	AA7	AA8	AA9 VCCO_3	AA10 VCCO_4	AA11 VCCO_4	AA12 VCCO_4	AA13 VCCO_4	AA14 VCCO_4	AA15 VCCO_4	AA16 VCCO_5	AA17 VCCO_5	AA18 VCCO_5	AA19 VCCO_5	AA20 VCCO_5	AA21 VCCO_5	AA22 VCCO_6	AA23	AA24	AA25 SDRAM_A(5)	AA26 SDRAM_A(4)	AA27 SDRAM_A(3)	AA28 SDRAM_DQM(3)	AA29 SDRAM_DQ(31)	AA30 SDRAM_DQ(30)
AB1 Adr(7)	AB2 Adr(8)	AB3 Adr(9)	AB4 Adr(10)	AB5	AB6	AB7	AB8	AB9 VCCO_3	AB10 VCCO_4	AB11 VCCO_4	AB12 VCCO_4	AB13 VCCO_4	AB14 VCCO_4	AB15 Data(3)	AB16 IRQ2_n	AB17	AB18 VCCO_5	AB19 VCCO_5	AB20 VCCO_5	AB21 VCCO_5	AB22 VCCO_6	AB23	AB24	AB25	AB26 SDRAM_A(9)	AB27 SDRAM_A(9)	AB28 SDRAM_A(8)	AB29 SDRAM_A(7)	AB30 SDRAM_A(6)
AC1 GND	AC2 Adr(4)	AC3 Adr(5)	AC4 Adr(6)	AC5	AC6	AC7 CCLK	AC8 DONE	AC9 D0	AC10 Data(16)	AC11 Data(11)	AC12 Data(9)	AC13	AC14	AC15 Data(2)	AC16 IRQ1_n	AC17	AC18	AC19 TestCon(8)	AC20 TestCon(9)	AC21 TestCon(10)	AC22 D7	AC23 M2	AC24 M1	AC25	AC26 SDRAM_DQM(1)	AC27	AC28 SDRAM_A(12)	AC29 SDRAM_CKE	AC30 GND
AD1	AD2	AD3	AD4	AD5 Adr(2)	AD6 Adr(3)	AD7 PWRDWN_B	AD8	AD9 D1	AD10 Data(15)	AD11 Data(10)	AD12 Data(8)	AD13	AD14 Data(7)	AD15 Data(1)	AD16 IRQ0_n	AD17	AD18	AD19 TestCon(11)	AD20 TestCon(12)	AD21 TestCon(13)	AD22 D6	AD23	AD24 M0	AD25 SDRAM_DQ(9)	AD26 SDRAM_DQ(8)	AD27	AD28	AD29	AD30
AE1	AE2	AE3	AE4	AE5	AE6 GND	AE7 Data(25)	AE8 Data(24)	AE9 Data(20)	AE10 Data(14)	AE11	AE12	AE13 GND	AE14 Data(6)	AE15 Data(0)	AE16 Empty	AE17	AE18 GND	AE19	AE20	AE21	AE22	AE23	AE24	AE25 GND	AE26	AE27	AE28	AE29	AE30
AF1	AF2	AF3	AF4	AF5 GND	AF6	AF7 INIT_B	AF8 Data(23)	AF9 Data(19)	AF10 Data(13)	AF11	AF12	AF13	AF14 Data(5)	AF15 SDRAM_CLKin	AF16 SDRAM_CLK	AF17	AF18	AF19	AF20	AF21 TTC_n(7)	AF22 TTC_n(6)	AF23 TTC_n(4)	AF24 RDWR_B	AF25	AF26 GND	AF27	AF28	AF29	AF30
AG1 Data(30)	AG2 Data(31)	AG3 Adr(0)	AG4 GND	AG5 Adr(1)	AG6 DOUT	AG7 D2	AG8 VRP_4	AG9 GND	AG10 Data(12)	AG11	AG12 GND	AG13	AG14 Data(4)	AG15 ShareWr_n	AG16 LHC_Clk	AG17 ChaBusy	AG18	AG19 GND	AG20	AG21 TTC_n(5)	AG22 GND	AG23 VRN_5	AG24 D5	AG25 CS_B	AG26 SDRAM_DQ(13)	AG27 GND	AG28 SDRAM_DQ(12)	AG29 SDRAM_DQ(11)	AG30 SDRAM_DQ(10)
AH1 Data(26)	AH2 Data(27)	AH3 GND	AH4 Data(28)	AH5 Data(29)	AH6 GNDA16	AH7 D3	AH8 VRN_4	AH9 Data(18)	AH10	AH11	AH12 GNDA18	AH13	AH14 GND	AH15 ShareRd_n	AH16 Clk	AH17 GND	AH18	AH19 GNDA19	AH20	AH21	AH22 TTC_n(3)	AH23 VRP_5	AH24 D4	AH25 GNDA21	AH26	AH27	AH28 GND	AH29 SDRAM_DQ(15)	AH30 SDRAM_DQ(14)
AJ1 VCCAUX	AJ2 GND	AJ3 VRP_3	AJ4 AVCCAUXRX16	AJ5 VTRXPAD16	AJ6 AVCCAUXTX16	AJ7 VTTXPAD16	AJ8 Data(22)	AJ9 Data(17)	AJ10	AJ11 AVCCAUXRX18	AJ12 VTRXPAD18	AJ13 AVCCAUXTX18	AJ14 VTTXPAD18	AJ15 Rocket_XC1k	AJ16 Clkx2	AJ17 AVCCAUXRX19	AJ18 VTRXPAD19	AJ19 AVCCAUXTX19	AJ20 VTTXPAD19	AJ21	AJ22 TTC_n(2)	AJ23 TTC_n(1)	AJ24 AVCCAUXRX21	AJ25 VTRXPAD21	AJ26 AVCCAUXTX21	AJ27 VTTXPAD21	AJ28 VRP_6	AJ29 GND	AJ30 VCCAUX
	AK2 VCCAUX	AK3 VRN_3	AK4	AK5	AK6	AK7	AK8 Data(21)	AK9 GND	AK10	AK11	AK12	AK13	AK14	AK15 VCCAUX	AK16 VCCAUX	AK17 ROCKET_LVDS rocket_lvds T Rocket_RXN	AK18 ROCKET_LVDS rocket_lvds T Rocket_RXP	AK19 ROCKET_LVDS rocket_lvds S Rocket_TXP	AK20 ROCKET_LVDS rocket_lvds S Rocket_TXN	AK21	AK22 GND	AK23 TTC_n(0)	AK24	AK25	AK26	AK27	AK28 VRN_6	AK29 VCCAUX	

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

channel_in	Rev V2 2
	Date 7 Feb 2006
Input FPGA	Time 1:50:53 pm
Proj: MROD-X	Proj.No: 38405
	Name tonvr
Peter Jansweijer	peterj@nikhef.nl
	Size A3 4 1 4 A
NIKHEF	Dim 420 x 297 mm
© ET-Nikhef Amsterdam	Page 2 of 6

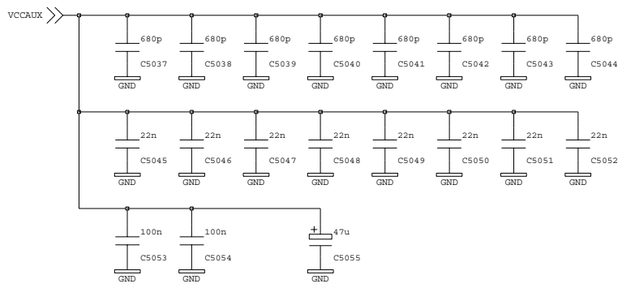
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND

XC2VP7/20 VCCINT Decoupling Capacitors
Min. Power-On Current XC2VP20
IccINT = 600 mA



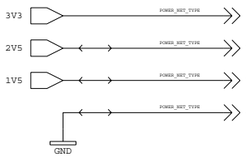
AVX TAJB476K010R

XC2VP7/20 VCCAUX Decoupling Capacitors
Min. Power-On Current XC2VP20
IccAUX = 250 mA (min)



AVX TAJB476K010R

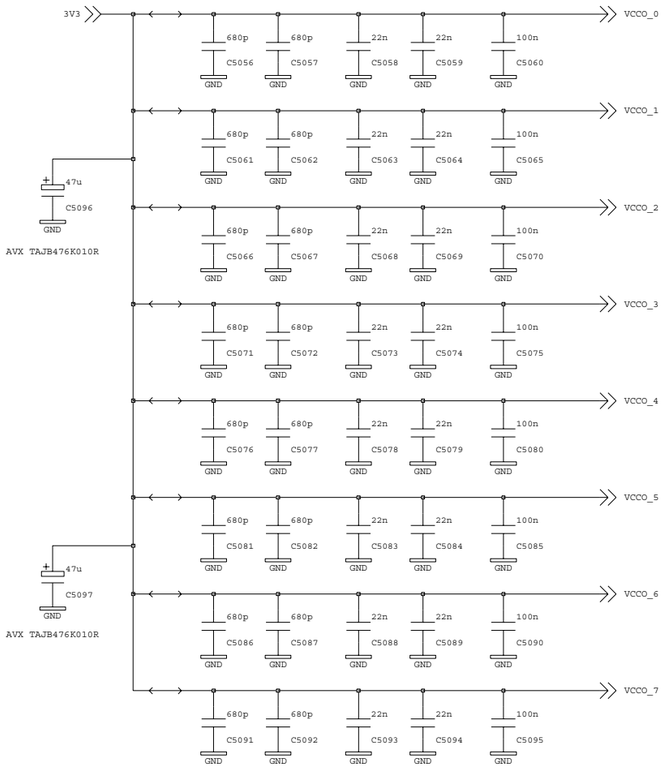
Power Inputs
For Xilinx Virtex-II Pro, power supplies
can be turned on in any sequence.



VCCAUX and VCCO can ramp up at any rate

VCCINT Ramp rate 200 us min. and 50 ms max.

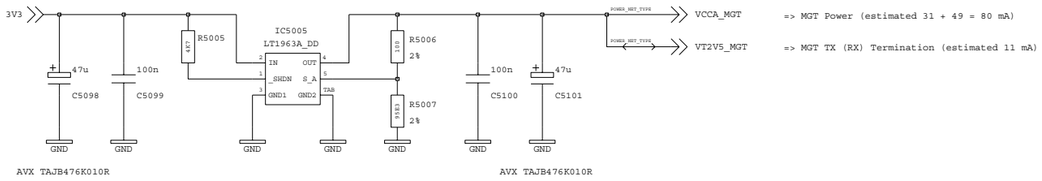
All GND nets on the FPGA need
to be connected to golbal GROUND.



AVX TAJB476K010R

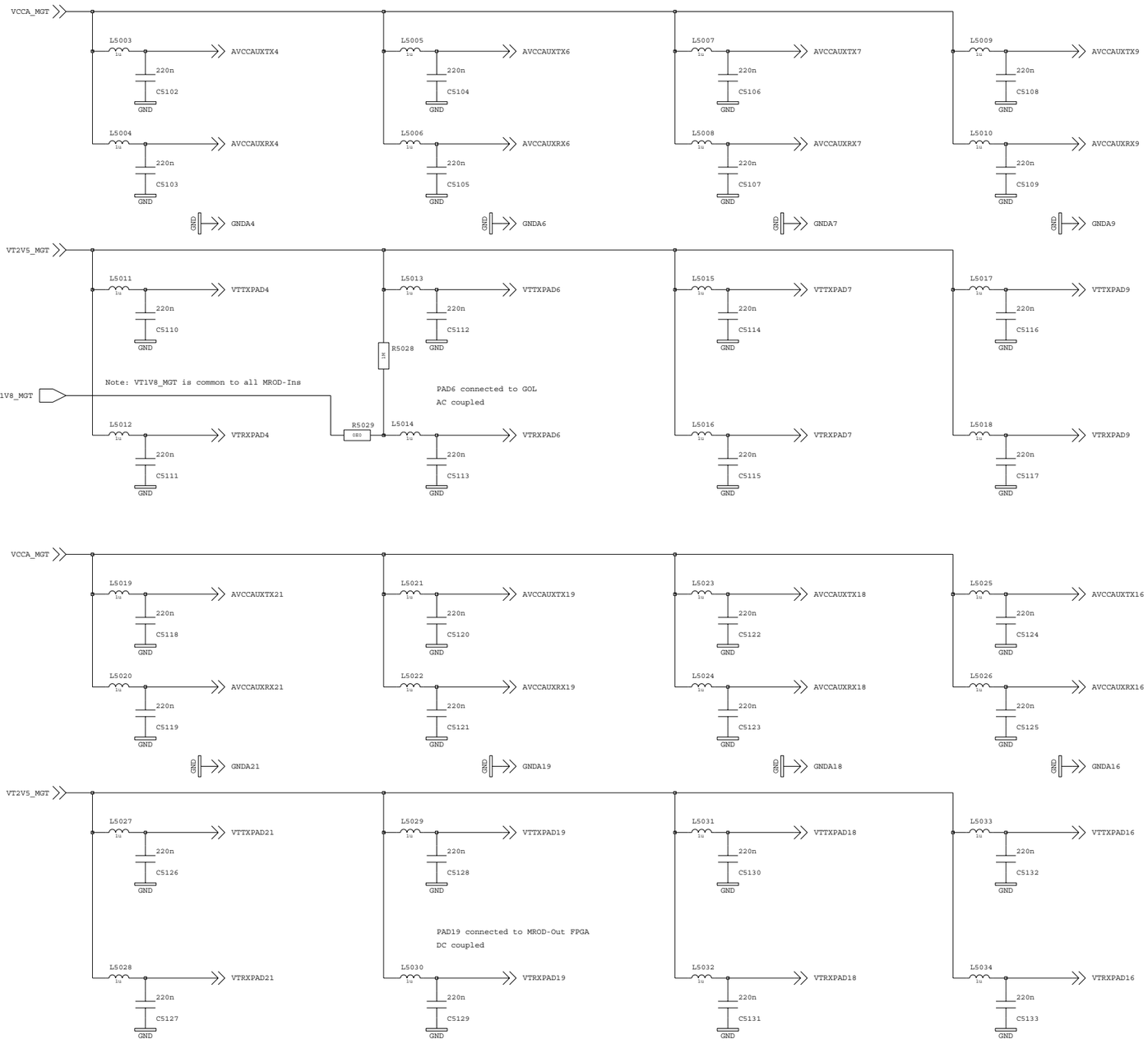
channel_in		Rev V2 2
		Date 7 Feb 2006
Input FPGA Power Supply Decoupling		Time 1:51:34 pm
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
		Dim 420 x 297 mm
		Page 3 of 6

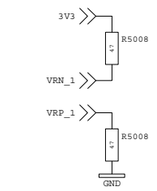
2V5 @ 1,5A



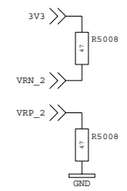
=> MGT Power (estimated 31 + 49 = 80 mA)

=> MGT TX (RX) Termination (estimated 11 mA)

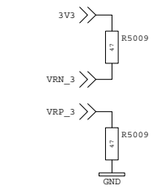




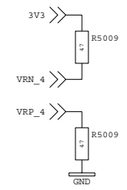
Series Termination for
Not (yet) used



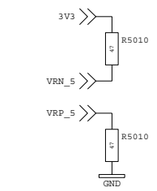
Series Termination for
Not (yet) used



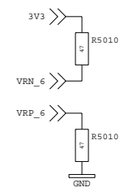
Series Termination for
Sharc Addressbus



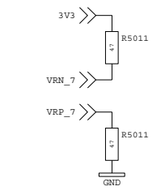
Series Termination for
Sharc Databus



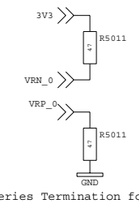
Series Termination for
General purpose



Series Termination for
SDRAM interface



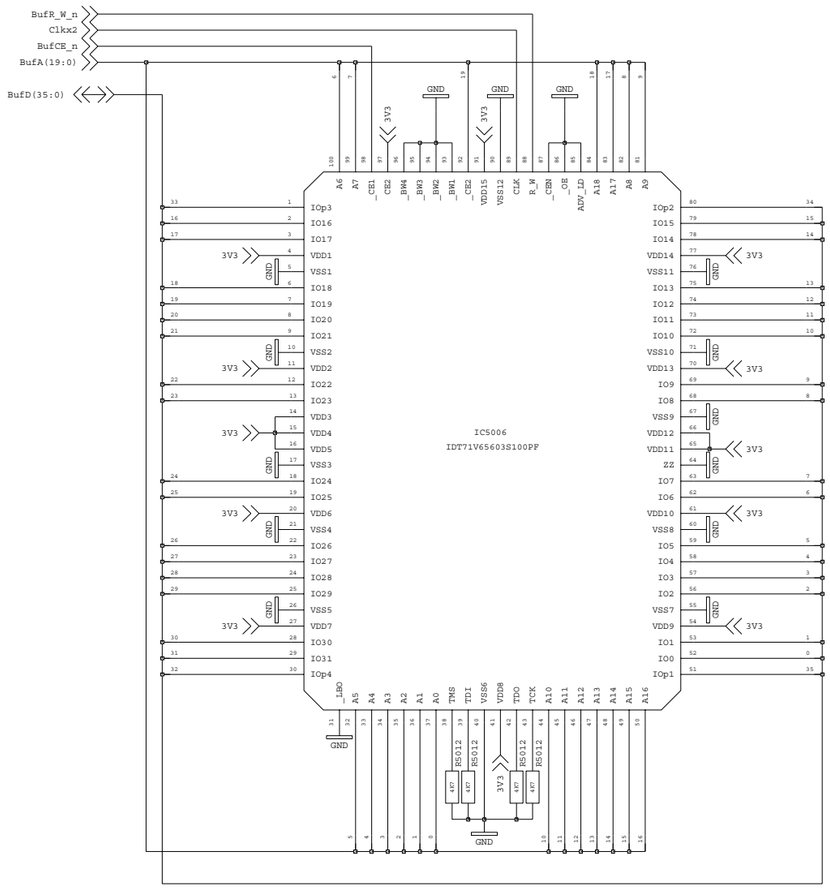
Series Termination for
Buffer Memory interface

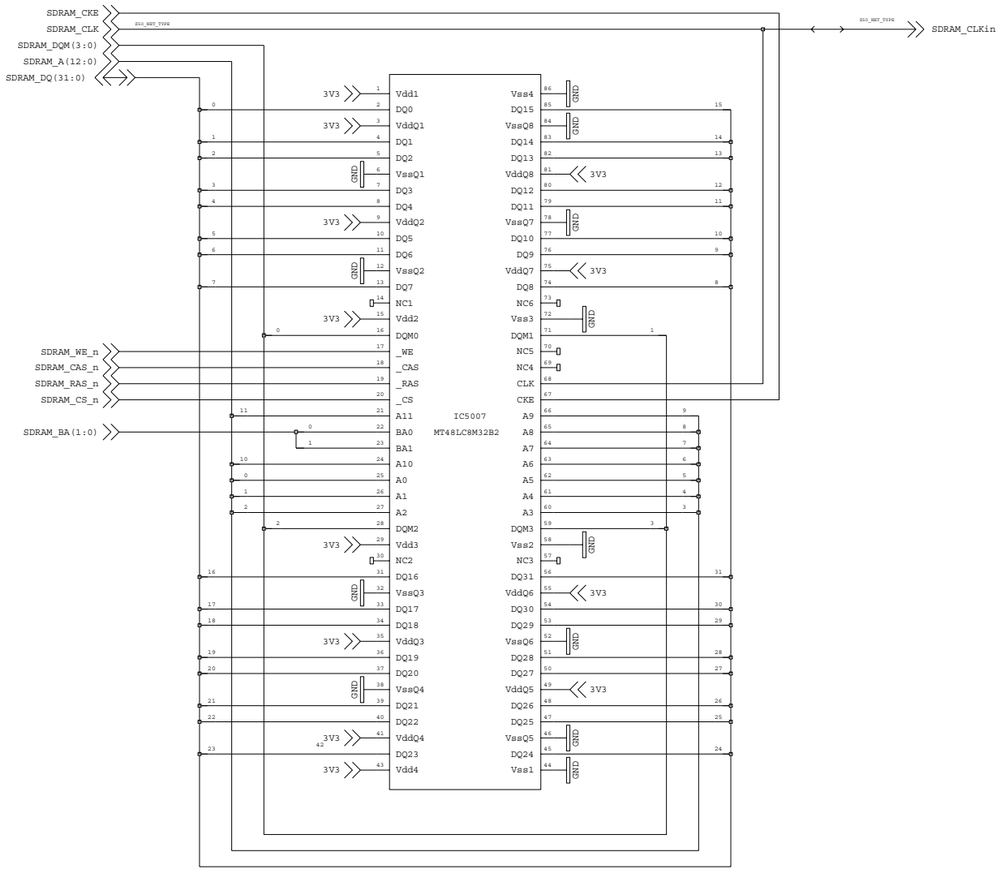


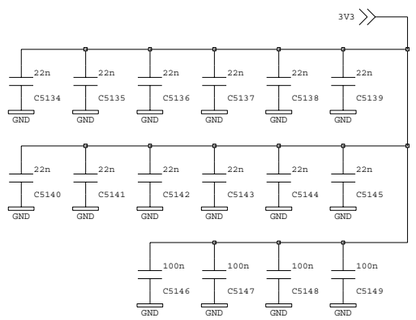
Series Termination for
General purpose

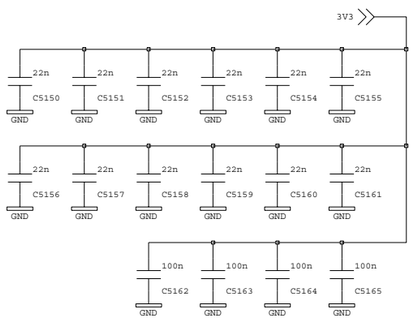
channel_in		Rev V2 2	
		Date 7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time 1:52:01 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
© ET-Nikhef Amsterdam		Page 4 of 6	

SDRAM_A(12) is not connected









channel_in		Rev V2 2	
		Date 7 Feb 2006	
Buffer Memory (ZBT and SDRAM)		Time 1:52:29 pm	
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
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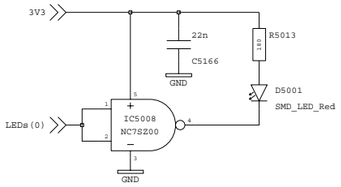
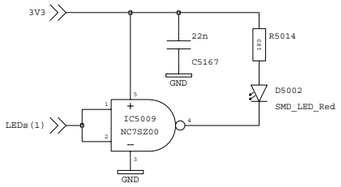
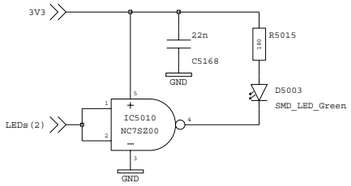
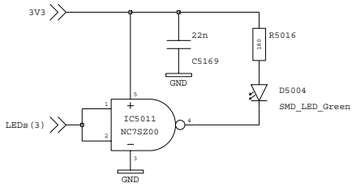
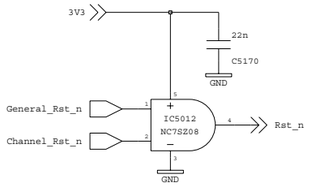


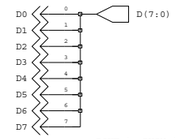


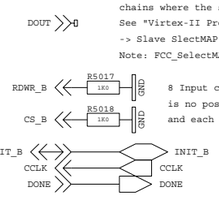






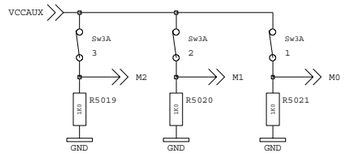
Fiducial20 Fiducial21





DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices.
See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SlectMAP programming Mode -> BUSY.
Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!

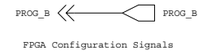
8 Input channels are loaded in parallel so there is no possibility for readback (RDWR_B = '0') and each CS_B = '0'



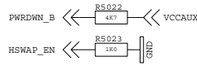
M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.



FPGA Configuration Signals

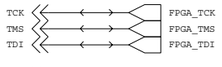


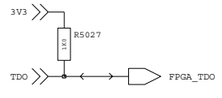
PWRDWN_B is unsupported (should be pulled high)

HSWAP_EN = '0' => User IOs have pull-up resistors during configuration

VBATT is decriptor key memory backup supply

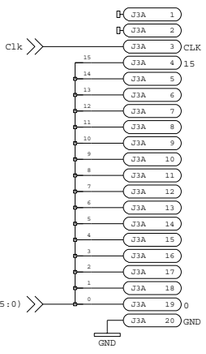
FPGA Control signals



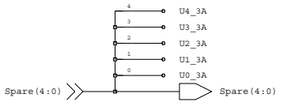


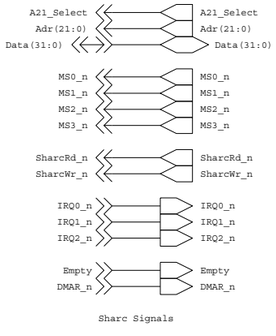
FPGA JTAG Signals

Optinal Test Connector



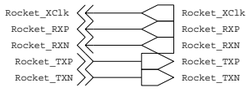
Testpoints force Spare lines to be accessible.





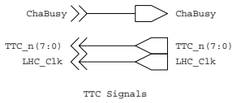
Sharc Signals

Input Channel ID bits

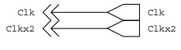


Frontend to Backend

Rocket IO Signals

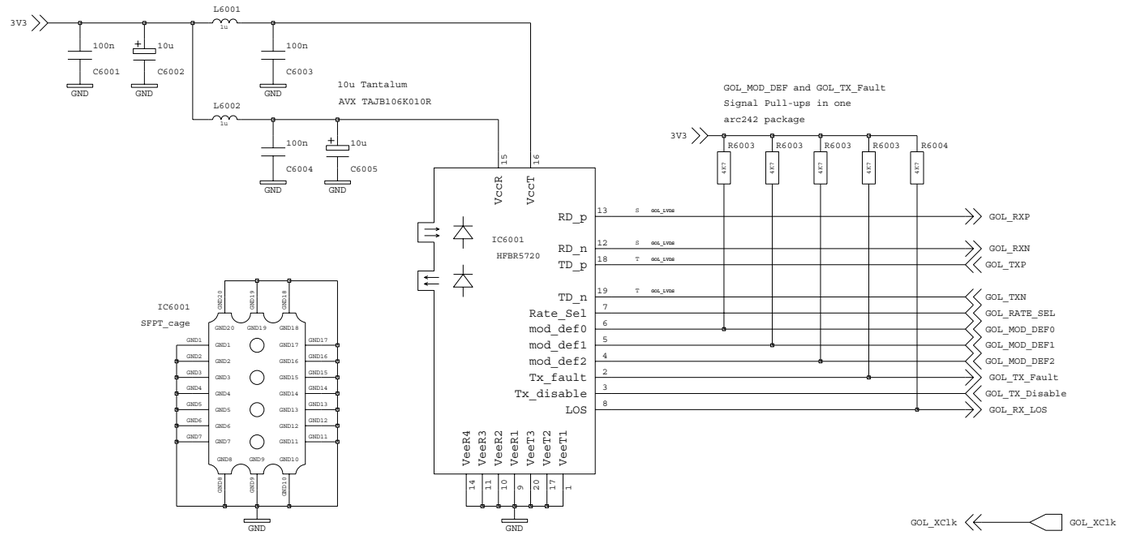


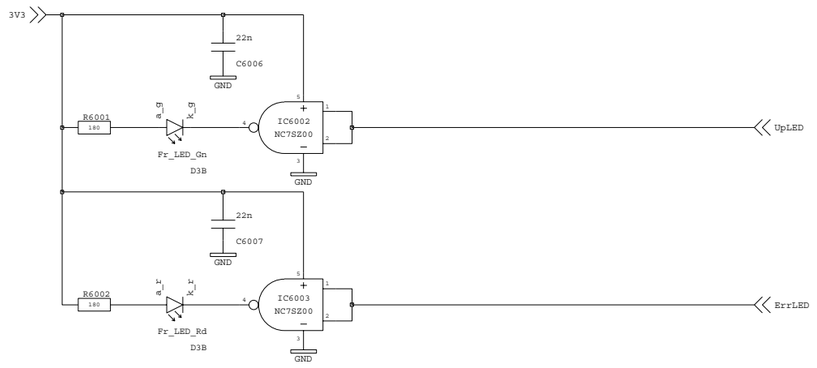
TTC Signals



Clock Signals

channel_in		Rev V2 2
		Date 7 Feb 2006
		Time 1:53:04 pm
		Name Ton van Reen
Input FPGA Auxiliary Connections		
Proj: MROD-X	Proj.No: 38405	
Peter Jansweijer	peterj@nikhef.nl	Size A3 4 1 4 A
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
© ET-Nikhef Amsterdam		Page 6 of 6





channel_in		Rev V2 2	
		Date 7 Feb 2006	
GOL Input		Time 1:50:33 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
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IC6004
XC2VP7FF896

	A2 VCCAUX	A3 VRP_2	A4	A5	A6	A7	A8	A9 GND	A10	A11	A12	A13	A14	A15 VCCAUX	A16 VCCAUX	A17 GOL_LVDS gol_lvds T DP_GOL_RX3B	A18 GOL_LVDS gol_lvds T DP_GOL_RX3B	A19 GOL_LVDS gol_lvds S DP_GOL_TX3B	A20 GOL_LVDS gol_lvds S DP_GOL_TX3B	A21	A22 GND	A23 LEDs(0)	A24	A25	A26	A27	A28 VRP_7	A29 VCCAUX	
B1 VCCAUX	B2 GND	B3 VRN_2	B4 AVCCAUXRX9	B5 VTRXPAD9	B6 AVCCAUXTX9	B7 VTTXPAD9	B8	B9	B10	B11 AVCCAUXRX7	B12 VTRXPAD7	B13 AVCCAUXTX7	B14 VTTXPAD7	B15	B16 GOL_Xclk	B17 AVCCAUXRX6	B18 VTRXPAD6	B19 AVCCAUXTX6	B20 VTTXPAD6	B21	B22	B23 LEDs(1)	B24 AVCCAUXRX4	B25 VTRXPAD4	B26 AVCCAUXTX4	B27 VTTXPAD4	B28 VRN_7	B29 GND	B30 VCCAUX
C1	C2	C3 GND	C4	C5	C6 GNDA9	C7	C8	C9	C10	C11	C12 GNDA7	C13	C14 GND	C15	C16	C17 GND	C18 UpLED	C19 GNDA6	C20	C21	C22	C23 LEDs(2)	C24 LEDs(3)	C25 GNDA4	C26 BufA(6)	C27 BufA(7)	C28 GND	C29 BufCE_n	C30 BufA(19)
D1	D2	D3 GND	D4	D5	D6	D7	D8	D9 GND	D10	D11	D12 GND	D13	D14	D15	D16 GOL_RX_LOS	D17 GOL_TX_Disable	D18 ErrLED	D19 GND	D20 GOL_MOD_DEF1	D21 GOL_MOD_DEF0	D22 GND	D23 ChaID(1)	D24 ChaID(0)	D25 DXN	D26 BufD(16)	D27 GND	D28 BufD(33)	D29	D30
E1	E2	E3	E4 GND	E5	E6 VRN_1	E7 VRP_1	E8	E9	E10	E11	E12	E13	E14	E15	E16	R17 GOL_TX_Fault	E18	E19	E20 GOL_MOD_DEF2	E21 GOL_RATE_SEL	E22	E23 ChaID(2)	E24 VRN_0	E25 VRP_0	E26 GND	E27	E28	E29	E30
F1	F2	F3	F4	F5 TDO	F6 GND	F7	F8	F9	F10	F11	F12	F13 GND	F14	F15	F16	F17	F18 GND	F19	F20	F21 TestCon(1)	F22 TestCon(0)	F23	F24	F25 GND	F26 TDI	F27	F28	F29	F30
G1	G2	G3	G4	G5	G6	G7 TCK	G8	G9	G10	G11	G12	G13	G14	G15	G16 Rst_n	G17	G18	G19 TestCon(6)	G20 TestCon(5)	G21 TestCon(4)	G22 TestCon(3)	G23 TestCon(2)	G24 PROG_B	G25 BufD(18)	G26 BufD(17)	G27	G28	G29	G30
H1 GND	H2	H3	H4	H5	H6	H7 VBATT	H8 TMS	H9	H10	H11	H12 TestCon(15)	H13	H14	H15	H16	H17	H18	H19 TestCon(7)	H20 T_Alert_n	H21 SMBData	H22 SMBClk	H23 HSWAP_EN	H24 DXP	H25	H26	H27	H28	H29 BufD(19)	H30 GND
J1	J2	J3	J4	J5	J6	J7	J8 TestCon(14)	J9 VCCO_2	J10 VCCO_1	J11 VCCO_1	J12 VCCO_1	J13 VCCO_1	J14	J15	J16	J17	J18 VCCO_0	J19 VCCO_0	J20 VCCO_0	J21 VCCO_0	J22 VCCO_7	J23 BufD(25)	J24 BufD(24)	J25	J26	J27 BufD(23)	J28 BufD(22)	J29 BufD(21)	J30 BufD(20)
K1	K2	K3	K4	K5	K6	K7	K8	K9 VCCO_2	K10 VCCO_1	K11 VCCO_1	K12 VCCO_1	K13 VCCO_1	K14 VCCO_1	K15 VCCO_1	K16 VCCO_0	K17 VCCO_0	K18 VCCO_0	K19 VCCO_0	K20 VCCO_0	K21 VCCO_0	K22 VCCO_7	K23	K24	K25 BufD(31)	K26 BufD(30)	K27 BufD(29)	K28 BufD(28)	K29 BufD(27)	K30 BufD(26)
L1	L2	L3 GND	L4	L5	L6 GND	L7	L8	L9 VCCO_2	L10 VCCO_2	L11 GND	L12 VCCINT	L13 VCCINT	L14 VCCINT	L15 VCCINT	L16 VCCINT	L17 VCCINT	L18 VCCINT	L19 VCCINT	L20 GND	L21 VCCO_7	L22 VCCO_7	L23	L24	L25 GND	L26 BufA(3)	L27 BufA(4)	L28 GND	L29 BufA(5)	L30 BufD(32)
M1	M2	M3	M4	M5	M6	M7	M8	M9 VCCO_2	M10 VCCO_2	M11 VCCINT	M12 GND	M13 GND	M14 GND	M15 GND	M16 GND	M17 GND	M18 GND	M19 GND	M20 VCCINT	M21 VCCO_7	M22 VCCO_7	M23 BufA(14)	M24 BufA(13)	M25 BufA(12)	M26 BufA(11)	M27 BufA(10)	M28 BufA(0)	M29 BufA(1)	M30 BufA(2)
N1	N2	N3	N4	N5	N6	N7	N8	N9 VCCO_2	N10 VCCO_2	N11 VCCINT	N12 GND	N13 GND	N14 GND	N15 GND	N16 GND	N17 GND	N18 GND	N19 GND	N20 VCCINT	N21 VCCO_7	N22 VCCO_7	N23 BufD(4)	N24 BufD(3)	N25 BufD(2)	N26 BufD(1)	N27 BufD(0)	N28 BufD(35)	N29 BufA(16)	N30 BufA(15)
P1	P2	P3	P4	P5	P6 GND	P7	P8	P9	P10 VCCO_2	P11 VCCINT	P12 GND	P13 GND	P14 GND	P15 GND	P16 GND	P17 GND	P18 GND	P19 GND	P20 VCCINT	P21 VCCO_7	P22 BufD(12)	P23 BufD(11)	P24 BufD(10)	P25 GND	P26 BufD(9)	P27 BufD(8)	P28 BufD(7)	P29 BufD(6)	P30 BufD(5)
R1 VCCAUX	R2	R3	R4	R5	R6	R7	R8	R9	R10 VCCO_2	R11 VCCINT	R12 GND	R13 GND	R14 GND	R15 GND	R16 GND	R17 GND	R18 GND	R19 GND	R20 VCCINT	R21 VCCO_7	R22 BufA(18)	R23 BufA(17)	R24 BufA(8)	R25 BufA(9)	R26 BufD(34)	R27 BufD(15)	R28 BufD(14)	R29 BufD(13)	R30 VCCAUX
T1 VCCAUX	T2	T3	T4	T5 Spare(4)	T6 Spare(3)	T7 Spare(2)	T8 Spare(1)	T9 Spare(0)	T10 VCCO_3	T11 VCCINT	T12 GND	T13 GND	T14 GND	T15 GND	T16 GND	T17 GND	T18 GND	T19 GND	T20 VCCINT	T21 VCCO_6	T22 SDRAM_DQ(6)	T23 SDRAM_DQ(5)	T24 SDRAM_DQ(4)	T25 SDRAM_DQ(3)	T26 SDRAM_DQ(2)	T27 SDRAM_DQ(1)	T28 SDRAM_DQ(0)	T29 BufR_W_n	T30 VCCAUX
U1	U2	U3	U4	U5	U6 GND	U7	U8	U9	U10 VCCO_3	U11 VCCINT	U12 GND	U13 GND	U14 GND	U15 GND	U16 GND	U17 GND	U18 GND	U19 GND	U20 VCCINT	U21 VCCO_6	U22 SDRAM_BA(0)	U23 SDRAM_A(11)	U24 SDRAM_CS_n	U25 GND	U26 SDRAM_RAS_n	U27 SDRAM_CAS_n	U28 SDRAM_WE_n	U29 SDRAM_DQM(0)	U30 SDRAM_DQ(7)
V1 A21_Select	V2	V3	V4	V5	V6	V7	V8	V9 VCCO_3	V10 VCCO_3	V11 VCCINT	V12 GND	V13 GND	V14 GND	V15 GND	V16 GND	V17 GND	V18 GND	V19 GND	V20 VCCINT	V21 VCCO_6	V22 VCCO_6	V23 SDRAM_DQ(17)	V24 SDRAM_DQ(16)	V25 SDRAM_DQM(2)	V26 SDRAM_A(2)	V27 SDRAM_A(1)	V28 SDRAM_A(0)	V29 SDRAM_A(10)	V30 SDRAM_BA(1)
W1 Adr(21)	W2 MS0_n	W3 MS1_n	W4 MS2_n	W5 MS3_n	W6 DMAR_n	W7	W8	W9 VCCO_3	W10 VCCO_3	W11 VCCINT	W12 GND	W13 GND	W14 GND	W15 GND	W16 GND	W17 GND	W18 GND	W19 GND	W20 VCCINT	W21 VCCO_6	W22 VCCO_6	W23 SDRAM_DQ(25)	W24 SDRAM_DQ(24)	W25 SDRAM_DQ(23)	W26 SDRAM_DQ(22)	W27 SDRAM_DQ(21)	W28 SDRAM_DQ(20)	W29 SDRAM_DQ(19)	W30 SDRAM_DQ(18)
Y1 Adr(17)	Y2 Adr(18)	Y3 GND	Y4 Adr(19)	Y5 Adr(20)	Y6 GND	Y7	Y8	Y9 VCCO_3	Y10 VCCO_3	Y11 GND	Y12 VCCINT	Y13 VCCINT	Y14 VCCINT	Y15 VCCINT	Y16 VCCINT	Y17 VCCINT	Y18 VCCINT	Y19 VCCINT	Y20 GND	Y21 VCCO_6	Y22 VCCO_6	Y23	Y24	Y25 GND	Y26 SDRAM_DQ(29)	Y27 SDRAM_DQ(28)	Y28 GND	Y29 SDRAM_DQ(27)	Y30 SDRAM_DQ(26)
AA1 Adr(11)	AA2 Adr(12)	AA3 Adr(13)	AA4 Adr(14)	AA5 Adr(15)	AA6 Adr(16)	AA7	AA8	AA9 VCCO_3	AA10 VCCO_4	AA11 VCCO_4	AA12 VCCO_4	AA13 VCCO_4	AA14 VCCO_4	AA15 VCCO_4	AA16 VCCO_5	AA17 VCCO_5	AA18 VCCO_5	AA19 VCCO_5	AA20 VCCO_5	AA21 VCCO_5	AA22 VCCO_6	AA23	AA24	AA25 SDRAM_A(5)	AA26 SDRAM_A(4)	AA27 SDRAM_A(3)	AA28 SDRAM_DQM(3)	AA29 SDRAM_DQ(31)	AA30 SDRAM_DQ(30)
AB1 Adr(7)	AB2 Adr(8)	AB3 Adr(9)	AB4 Adr(10)	AB5	AB6	AB7	AB8	AB9 VCCO_3	AB10 VCCO_4	AB11 VCCO_4	AB12 VCCO_4	AB13 VCCO_4	AB14	AB15 Data(3)	AB16 IRQ2_n	AB17	AB18 VCCO_5	AB19 VCCO_5	AB20 VCCO_5	AB21 VCCO_5	AB22 VCCO_6	AB23	AB24	AB25	AB26	AB27 SDRAM_A(9)	AB28 SDRAM_A(8)	AB29 SDRAM_A(7)	AB30 SDRAM_A(6)
AC1 GND	AC2 Adr(4)	AC3 Adr(5)	AC4 Adr(6)	AC5	AC6	AC7 CCLK	AC8 DONE	AC9 D0	AC10 Data(16)	AC11 Data(11)	AC12 Data(9)	AC13	AC14	AC15 Data(2)	AC16 IRQ1_n	AC17	AC18	AC19 TestCon(8)	AC20 TestCon(9)	AC21 TestCon(10)	AC22 D7	AC23 M2	AC24 M1	AC25	AC26	AC27 SDRAM_DQM(1)	AC28 SDRAM_A(12)	AC29 SDRAM_CKE	AC30 GND
AD1	AD2	AD3	AD4	AD5 Adr(2)	AD6 Adr(3)	AD7 PWRDWN_B	AD8	AD9 D1	AD10 Data(15)	AD11 Data(10)	AD12 Data(8)	AD13	AD14 Data(7)	AD15 Data(1)	AD16 IRQ0_n	AD17	AD18	AD19 TestCon(11)	AD20 TestCon(12)	AD21 TestCon(13)	AD22 D6	AD23 M0	AD24	AD25 SDRAM_DQ(9)	AD26 SDRAM_DQ(8)	AD27	AD28	AD29	AD30
AE1	AE2	AE3	AE4	AE5	AE6 GND	AE7 Data(25)	AE8 Data(24)	AE9 Data(20)	AE10 Data(14)	AE11	AE12	AE13 GND	AE14 Data(6)	AE15 Data(0)	AE16 Empty	AE17	AE18 GND	AE19	AE20	AE21	AE22	AE23	AE24	AE25 GND	AE26	AE27	AE28	AE29	AE30
AF1	AF2	AF3	AF4	AF5 GND	AF6	AF7 INIT_B	AF8 Data(23)	AF9 Data(19)	AF10 Data(13)	AF11	AF12	AF13	AF14 Data(5)	AF15 SDRAM_CLKin	AF16 SDRAM_CLK	AF17	AF18	AF19	AF20	AF21 TTC_n(7)	AF22 TTC_n(6)	AF23 TTC_n(4)	AF24 RDWR_B	AF25	AF26 GND	AF27	AF28	AF29	AF30
AG1 Data(30)	AG2 Data(31)	AG3 Adr(0)	AG4 GND	AG5 Adr(1)	AG6 DOUT	AG7 D2	AG8 VRP_4	AG9 GND	AG10 Data(12)	AG11	AG12 GND	AG13	AG14 Data(4)	AG15 SharcWr_n	AG16 LHC_Clk	AG17 ChaBusy	AG18	AG19 GND	AG20	AG21 TTC_n(5)	AG22 GND	AG23 VRN_5	AG24 D5	AG25 CS_B	AG26 SDRAM_DQ(13)	AG27 GND	AG28 SDRAM_DQ(12)	AG29 SDRAM_DQ(11)	AG30 SDRAM_DQ(10)
AH1 Data(26)	AH2 Data(27)	AH3 GND	AH4 Data(28)	AH5 Data(29)	AH6 GNDA16	AH7 D3	AH8 VRN_4	AH9 Data(18)	AH10	AH11	AH12 GNDA18	AH13	AH14 GND	AH15 SharcRd_n	AH16 Clk	AH17 GND	AH18	AH19 GNDA19	AH20	AH21	AH22 TTC_n(3)	AH23 VRP_5	AH24 D4	AH25 GNDA21	AH26	AH27	AH28 GND	AH29 SDRAM_DQ(15)	AH30 SDRAM_DQ(14)
AJ1 VCCAUX	AJ2 GND	AJ3 VRP_3	AJ4 AVCCAUXRX16	AJ5 VTRXPAD16	AJ6 AVCCAUXTX16	AJ7 VTTXPAD16	AJ8 Data(22)	AJ9 Data(17)	AJ10	AJ11 AVCCAUXRX18	AJ12 VTRXPAD18	AJ13 AVCCAUXTX18	AJ14 VTTXPAD18	AJ15 Rocket_XC1k	AJ16 Clkx2	AJ17 AVCCAUXRX19	AJ18 VTRXPAD19	AJ19 AVCCAUXTX19	AJ20 VTTXPAD19	AJ21	AJ22 TTC_n(2)	AJ23 TTC_n(1)	AJ24 AVCCAUXRX21	AJ25 VTRXPAD21	AJ26 AVCCAUXTX21	AJ27 VTTXPAD21	AJ28 VRP_6	AJ29 GND	AJ30 VCCAUX
	AK2 VCCAUX	AK3 VRN_3	AK4	AK5	AK6	AK7	AK8 Data(21)	AK9 GND	AK10	AK11	AK12	AK13	AK14	AK15 VCCAUX	AK16 VCCAUX	AK17 ROCKET_LVDS rocket T DP_ROCKET_RXN	AK18 ROCKET_LVDS rocket T DP_ROCKET_RXP	AK19 ROCKET_LVDS rocket S DP_ROCKET_TXP	AK20 ROCKET_LVDS rocket S DP_ROCKET_TXN	AK21	AK22 GND	AK23 TTC_n(0)	AK24	AK25	AK26	AK27	AK28 VRN_6	AK29 VCCAUX	

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

channel_in	Rev V2 2
	Date 7 Feb 2006
Input FPGA	Time 1:50:53 pm
Proj: MROD-X	Proj.No: 38405
	Name tonvr
Peter Jansweijer	peterj@nikhef.nl
	Size A3 4 1 4 A
NIKHEF	Dim 420 x 297 mm
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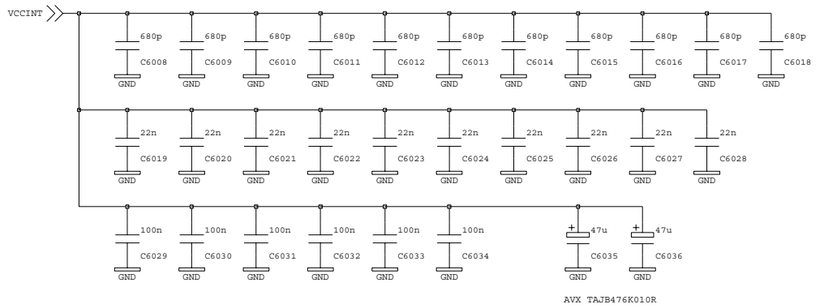
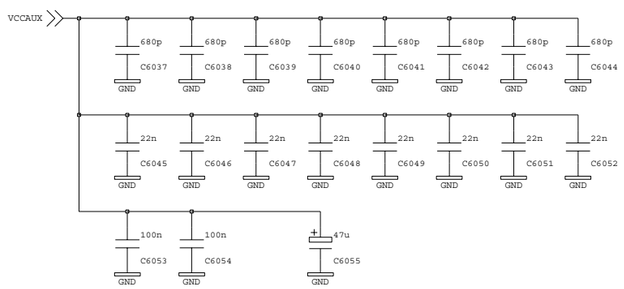
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND

XC2VP7/20 VCCINT Decoupling Capacitors
Min. Power-On Current XC2VP20
IccINT = 600 mA



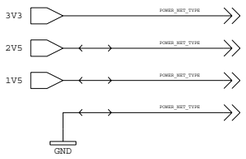
AVX TAJB476K010R

XC2VP7/20 VCCAUX Decoupling Capacitors
Min. Power-On Current XC2VP20
IccAUX = 250 mA (min)



AVX TAJB476K010R

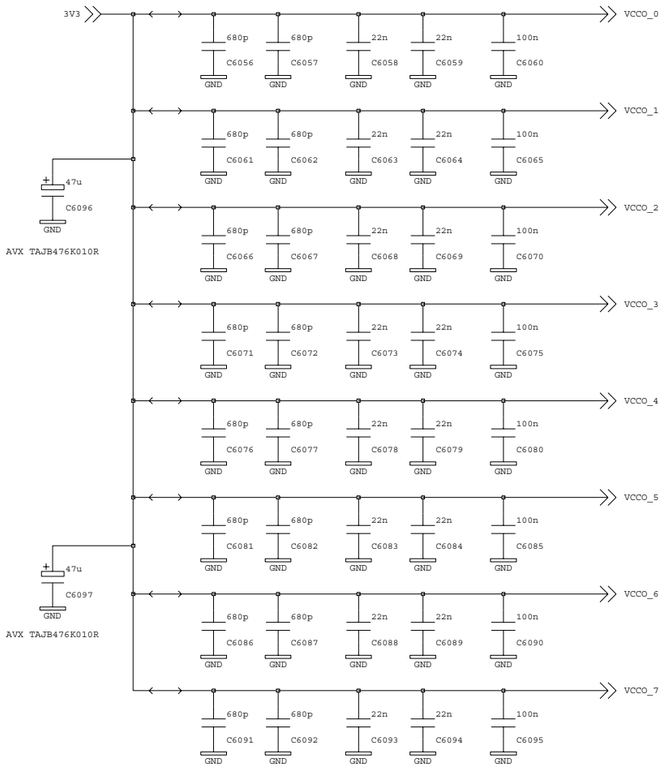
Power Inputs
For Xilinx Virtex-II Pro, power supplies
can be turned on in any sequence.



VCCAUX and VCCO can ramp up at any rate

VCCINT Ramp rate 200 us min. and 50 ms max.

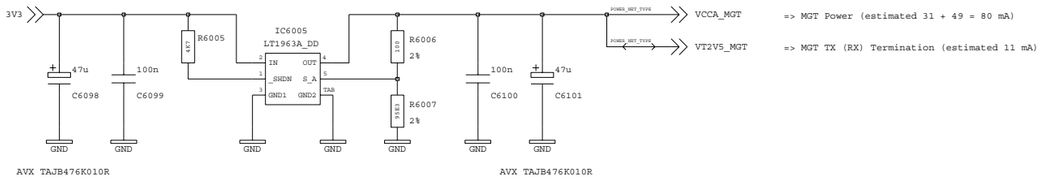
All GND nets on the FPGA need
to be connected to golbal GROUND.



AVX TAJB476K010R

channel_in		Rev V2 2
		Date 7 Feb 2006
Input FPGA Power Supply Decoupling		Time 1:51:34 pm
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 3 of 6

2V5 @ 1,5A

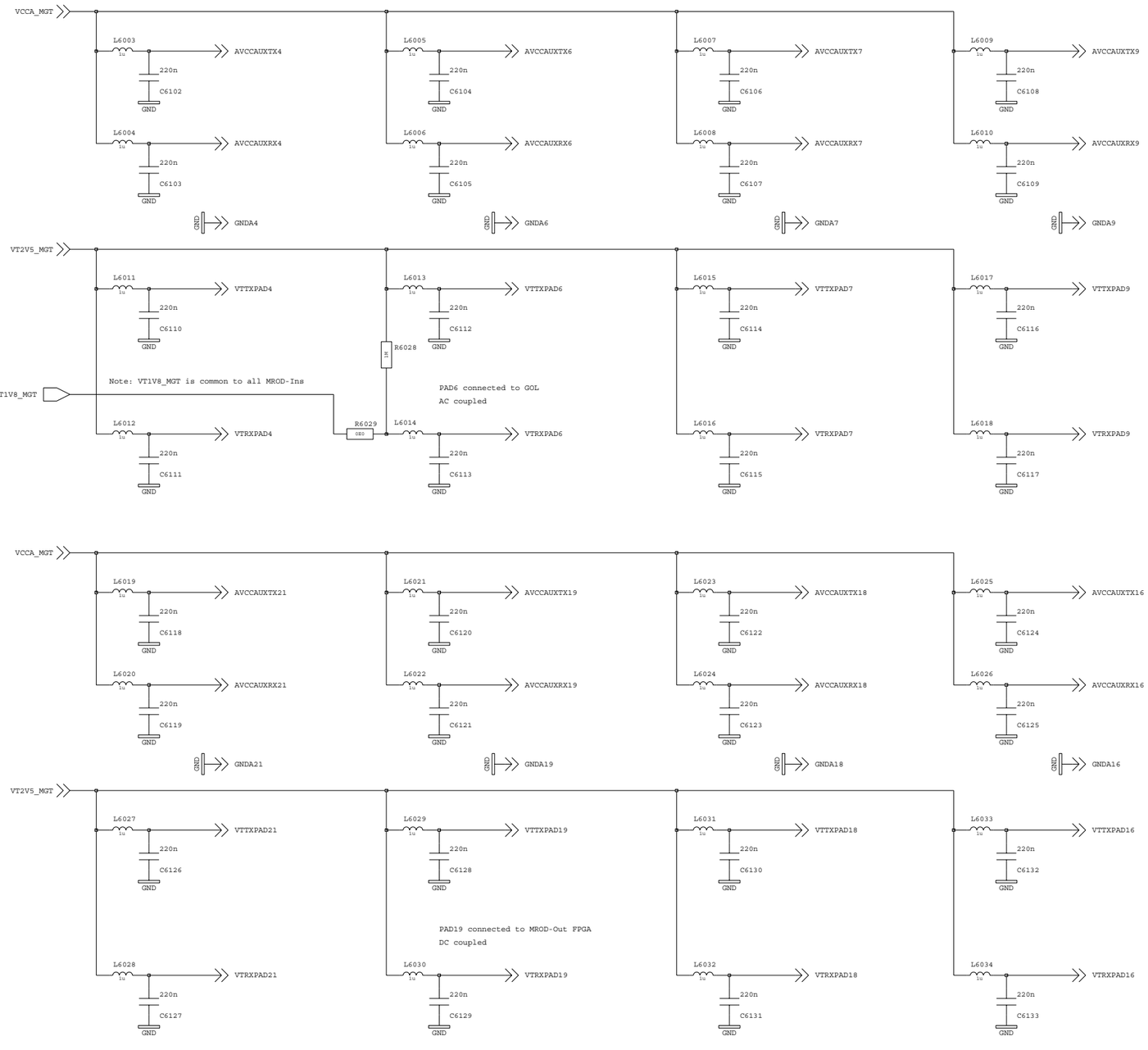


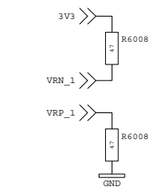
AVX TAJB476K010R

AVX TAJB476K010R

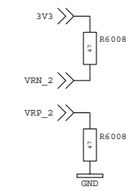
=> MGT Power (estimated 31 + 49 = 80 mA)

=> MGT TX (RX) Termination (estimated 11 mA)

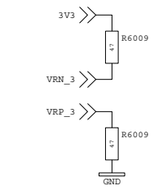




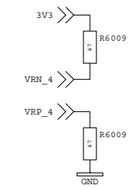
Series Termination for
Not (yet) used



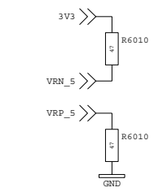
Series Termination for
Not (yet) used



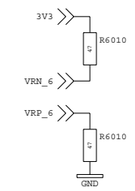
Series Termination for
Sharc Addressbus



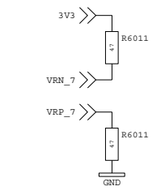
Series Termination for
Sharc Databus



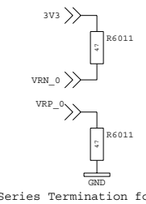
Series Termination for
General purpose



Series Termination for
SDRAM interface



Series Termination for
Buffer Memory interface



Series Termination for
General purpose

channel_in		Rev V2 2	
		Date 7 Feb 2006	
Input FPGA MGT Pwr Decoupling, Termination		Time 1:52:01 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
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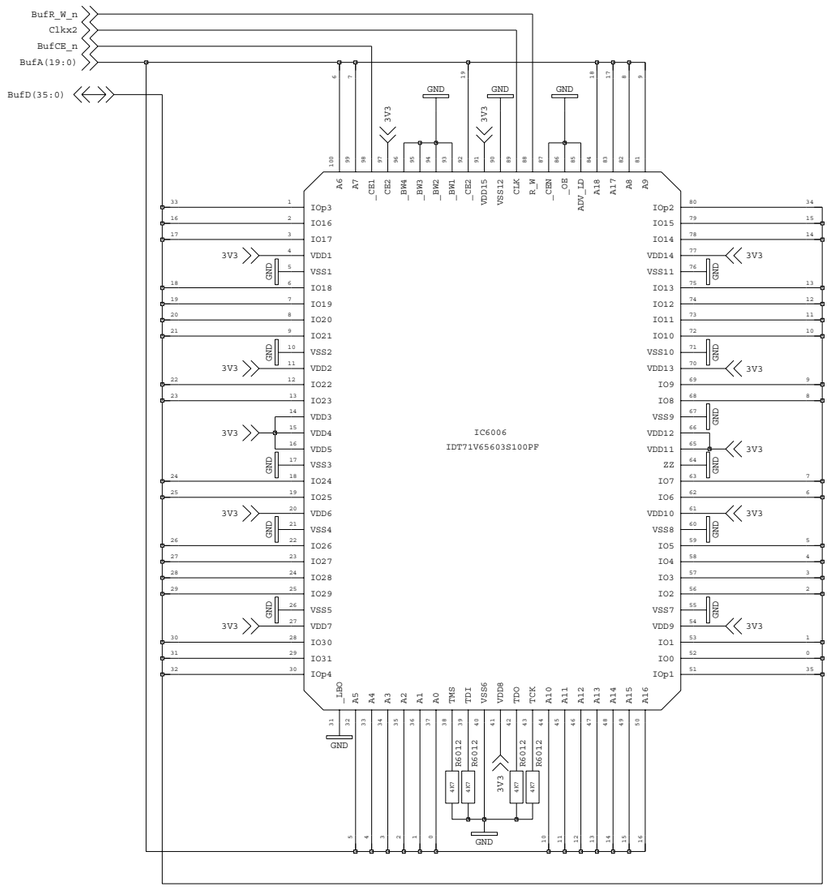
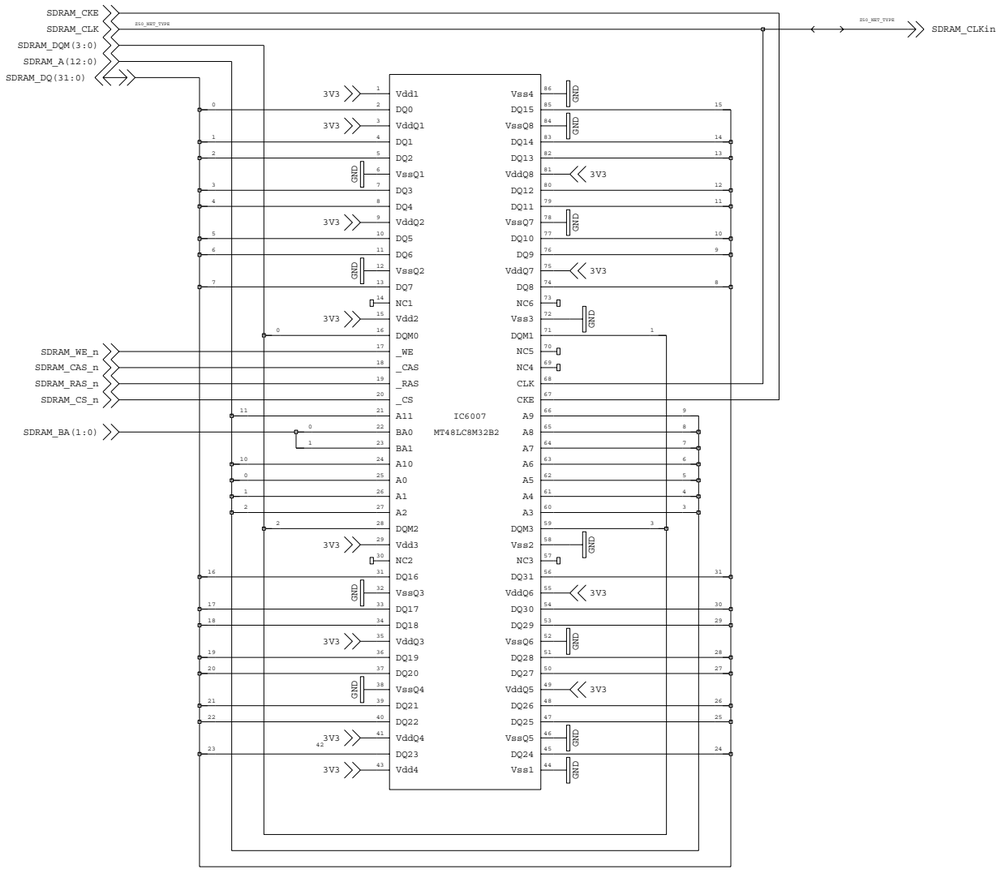
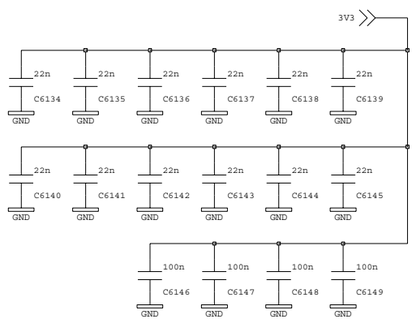
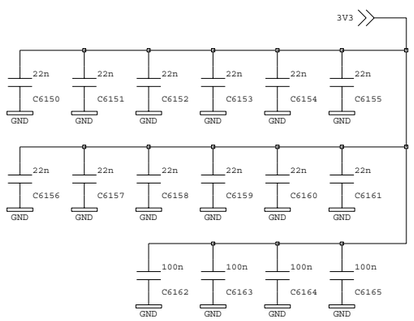
SDRAM_A(12) is not connected

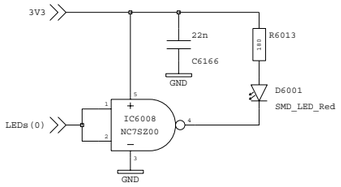


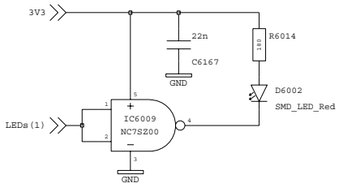


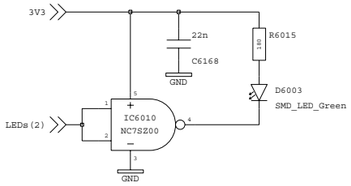


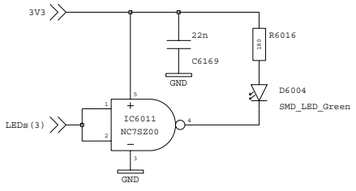


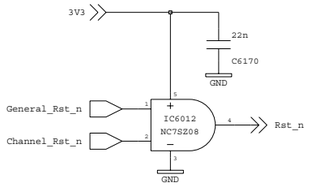
channel_in		Rev	V2 2
		Date	7 Feb 2006
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm
Proj: MROD-X	Proj.No: 38405	Name	Ton van Reen
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size	A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim	420 x 297 mm
		Page	5 of 6



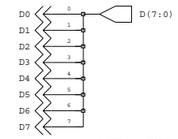


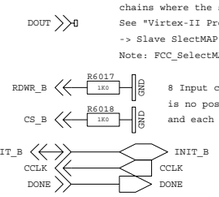






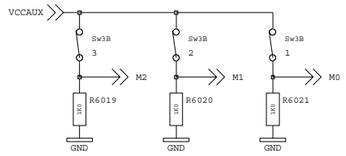
Fiducial6001 Fiducial6002





DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices.
See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SlectMAP programming Mode -> BUSY.
Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!

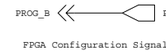
8 Input channels are loaded in parallel so there is no possibility for readback (RDWR_B = '0') and each CS_B = '0'



M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.



FPGA Configuration Signals

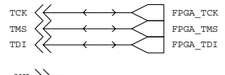
PWRDWN_B is unsupported (should be pulled high)

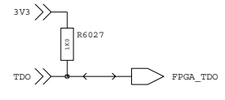
HSWAP_EN = '0' => User IOs have pull-up resistors during configuration

Temperature sensing diode

VBATT is decriptor key memory backup supply

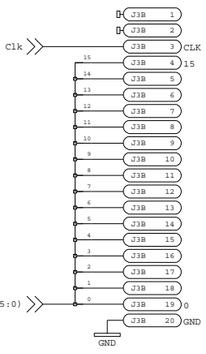
FPGA Control signals



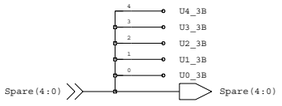


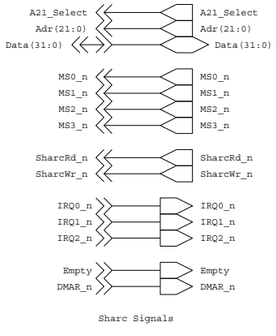
FPGA JTAG Signals

Optinal Test Connector



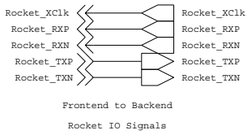
Testpoints force Spare lines to be accessible.





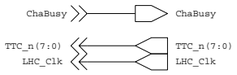
Sharc Signals

Input Channel ID bits

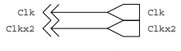


Frontend to Backend

Rocket IO Signals

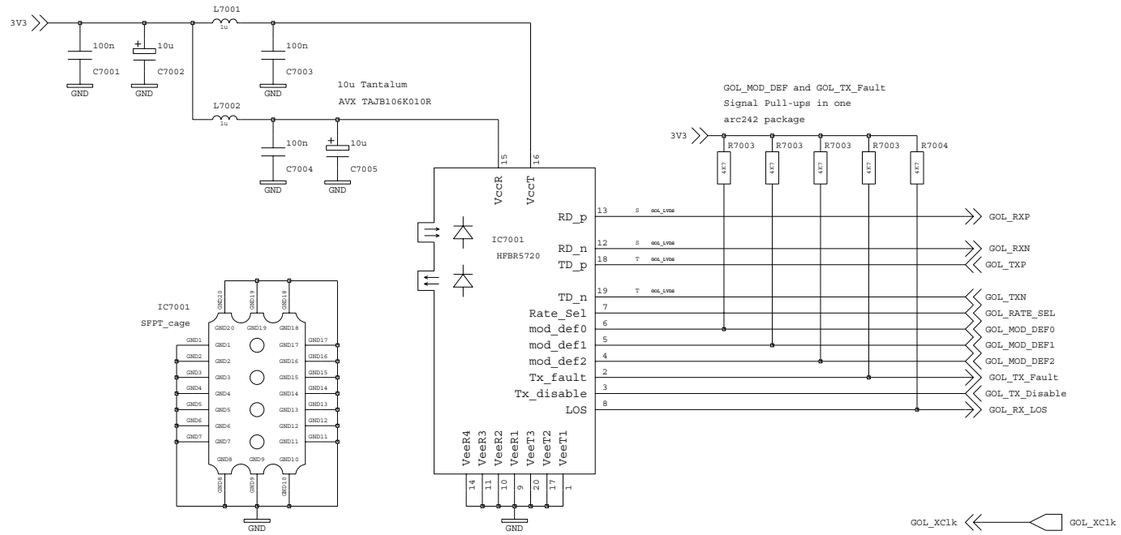


TTC Signals



Clock Signals

channel_in		Rev V2 2
		Date 7 Feb 2006
		Time 1:53:04 pm
Input FPGA Auxiliary Connections		Name Ton van Reen
Proj: MROD-X	Proj.No: 38405	
Peter Jansweijer	peterj@nikhef.nl	Size A3 4 1 4 A
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
© ET-Nikhef Amsterdam		Page 6 of 6



channel_in	Rev V2 2
	Date 7 Feb 2006
GOL Input	Time 1:50:33 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	
NIKHEF	Size A3 / 4 1 4 A
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
© ET-Nikhef Amsterdam	Page 1 of 6

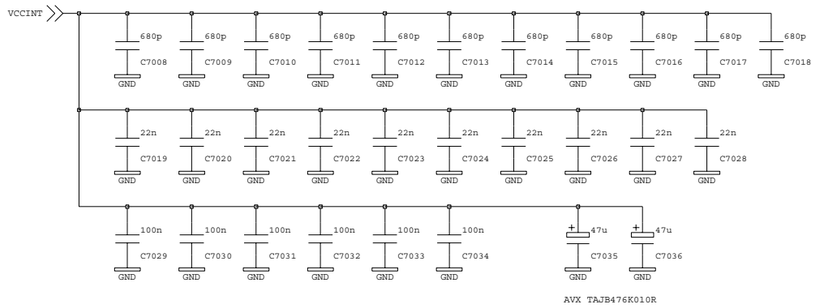
IC7004
XC2VP7FF896

	A2 VCCAUX	A3 VRP_2	A4	A5	A6	A7	A8	A9 GND	A10	A11	A12 VTRXPAD7	A13	A14 VTTXPAD7	A15 VCCAUX	A16 VCCAUX	A17 GOL_LVDS GOL_LVDS T DP_GOL_RX4A GOL_RXN	A18 GOL_LVDS GOL_LVDS T DP_GOL_RX4A GOL_RXP	A19 GOL_LVDS GOL_LVDS S DP_GOL_TX4A GOL_TXP	A20 GOL_LVDS GOL_LVDS S DP_GOL_TX4A GOL_TXN	A21	A22 GND	A23 LEDs(0)	A24	A25	A26	A27	A28 VRP_7	A29 VCCAUX	
B1 VCCAUX	B2 GND	B3 VRN_2	B4 AVCCAUXRX9	B5 VTRXPAD9	B6 AVCCAUXTX9	B7 VTTXPAD9	B8	B9	B10	B11 AVCCAUXRX7	B12	B13 AVCCAUXTX7	B14 VTTXPAD7	B15	B16 GOL_XClk	B17 AVCCAUXRX6	B18 VTRXPAD6	B19 AVCCAUXTX6	B20 VTTXPAD6	B21	B22 GND	B23 LEDs(1)	B24 AVCCAUXRX4	B25 VTRXPAD4	B26 AVCCAUXTX4	B27 VTTXPAD4	B28 VRN_7	B29 GND	B30 VCCAUX
C1	C2	C3 GND	C4	C5	C6 GNDA9	C7	C8	C9	C10	C11	C12 GNDA7	C13	C14 GND	C15	C16	C17 GND	C18 UpLED	C19 GNDA6	C20	C21	C22	C23 LEDs(2)	C24 LEDs(3)	C25 GNDA4	C26 BufA(6)	C27 BufA(7)	C28 GND	C29 BufCE_n	C30 BufA(19)
D1	D2	D3 GND	D4	D5	D6	D7	D8	D9 GND	D10	D11	D12 GND	D13	D14	D15	D16 GOL_RX_LOS	D17 GOL_TX_Disable	D18 ErrLED	D19 GND	D20 GOL_MOD_DEF1	D21 GOL_MOD_DEF0	D22 GND	D23 ChaID(1)	D24 ChaID(0)	D25 DXN	D26 BufD(16)	D27 GND	D28 BufD(33)	D29	D30
E1	E2	E3	E4 GND	E5	E6 VRN_1	E7 VRP_1	E8	E9	E10	E11	E12	E13	E14	E15	E16	R17 GOL_TX_Fault	E18	E19	R20 GOL_MOD_DEF2	R21 GOL_RATE_SEL	E22	E23 ChaID(2)	E24 VRN_0	R25 VRP_0	E26 GND	E27	E28	E29	E30
F1	F2	F3	F4	F5 TDO	F6 GND	F7	F8	F9	F10	F11	F12	F13 GND	F14	F15	F16	F17	F18 GND	F19	F20	F21 TestCon(1)	F22 TestCon(0)	F23	F24	F25 GND	F26 TDI	F27	F28	F29	F30
G1	G2	G3	G4	G5	G6	G7 TCK	G8	G9	G10	G11	G12	G13	G14	G15	G16 Rst_n	G17	G18	G19 TestCon(6)	G20 TestCon(5)	G21 TestCon(4)	G22 TestCon(3)	G23 TestCon(2)	G24 PROG_B	G25 BufD(18)	G26 BufD(17)	G27	G28	G29	G30
H1 GND	H2	H3	H4	H5	H6	H7 VBATT	H8 TMS	H9	H10	H11	H12 TestCon(15)	H13	H14	H15	H16	H17	H18	H19 TestCon(7)	H20 T_Alert_n	H21 SMBData	H22 SMBClk	H23 HSWAP_EN	H24 DXP	H25	H26	H27	H28	H29 BufD(19)	H30 GND
J1	J2	J3	J4	J5	J6	J7	J8 TestCon(14)	J9 VCCO_2	J10 VCCO_1	J11 VCCO_1	J12 VCCO_1	J13 VCCO_1	J14	J15	J16	J17	J18 VCCO_0	J19 VCCO_0	J20 VCCO_0	J21 VCCO_0	J22 VCCO_7	J23 BufD(25)	J24 BufD(24)	J25	J26	J27 BufD(23)	J28 BufD(22)	J29 BufD(21)	J30 BufD(20)
K1	K2	K3	K4	K5	K6	K7	K8	K9 VCCO_2	K10 VCCO_1	K11 VCCO_1	K12 VCCO_1	K13 VCCO_1	K14 VCCO_1	K15 VCCO_1	K16 VCCO_0	K17 VCCO_0	K18 VCCO_0	K19 VCCO_0	K20 VCCO_0	K21 VCCO_0	K22 VCCO_7	K23	K24	K25 BufD(31)	K26 BufD(30)	K27 BufD(29)	K28 BufD(28)	K29 BufD(27)	K30 BufD(26)
L1	L2	L3 GND	L4	L5	L6 GND	L7	L8	L9 VCCO_2	L10 VCCO_2	L11 GND	L12 VCCINT	L13 VCCINT	L14 VCCINT	L15 VCCINT	L16 VCCINT	L17 VCCINT	L18 VCCINT	L19 VCCINT	L20 GND	L21 VCCO_7	L22 VCCO_7	L23	L24	L25 GND	L26 BufA(3)	L27 BufA(4)	L28 GND	L29 BufA(5)	L30 BufD(32)
M1	M2	M3	M4	M5	M6	M7	M8	M9 VCCO_2	M10 VCCO_2	M11 VCCINT	M12 GND	M13 GND	M14 GND	M15 GND	M16 GND	M17 GND	M18 GND	M19 GND	M20 VCCINT	M21 VCCO_7	M22 VCCO_7	M23 BufA(14)	M24 BufA(13)	M25 BufA(12)	M26 BufA(11)	M27 BufA(10)	M28 BufA(0)	M29 BufA(1)	M30 BufA(2)
N1	N2	N3	N4	N5	N6	N7	N8	N9 VCCO_2	N10 VCCO_2	N11 VCCINT	N12 GND	N13 GND	N14 GND	N15 GND	N16 GND	N17 GND	N18 GND	N19 GND	N20 VCCINT	N21 VCCO_7	N22 VCCO_7	N23 BufD(4)	N24 BufD(3)	N25 BufD(2)	N26 BufD(1)	N27 BufD(0)	N28 BufD(35)	N29 BufA(16)	N30 BufA(15)
P1	P2	P3	P4	P5	P6 GND	P7	P8	P9	P10 VCCO_2	P11 VCCINT	P12 GND	P13 GND	P14 GND	P15 GND	P16 GND	P17 GND	P18 GND	P19 GND	P20 VCCINT	P21 VCCO_7	P22 BufD(12)	P23 BufD(11)	P24 BufD(10)	P25 GND	P26 BufD(9)	P27 BufD(8)	P28 BufD(7)	P29 BufD(6)	P30 BufD(5)
R1 VCCAUX	R2	R3	R4	R5	R6	R7	R8	R9	R10 VCCO_2	R11 VCCINT	R12 GND	R13 GND	R14 GND	R15 GND	R16 GND	R17 GND	R18 GND	R19 GND	R20 VCCINT	R21 VCCO_7	R22 BufA(18)	R23 BufA(17)	R24 BufA(8)	R25 BufA(9)	R26 BufD(34)	R27 BufD(15)	R28 BufD(14)	R29 BufD(13)	R30 VCCAUX
T1 VCCAUX	T2	T3	T4	T5 Spare(4)	T6 Spare(3)	T7 Spare(2)	T8 Spare(1)	T9 Spare(0)	T10 VCCO_3	T11 VCCINT	T12 GND	T13 GND	T14 GND	T15 GND	T16 GND	T17 GND	T18 GND	T19 GND	T20 VCCINT	T21 VCCO_6	T22 SDRAM_DQ(6)	T23 SDRAM_DQ(5)	T24 SDRAM_DQ(4)	T25 SDRAM_DQ(3)	T26 SDRAM_DQ(2)	T27 SDRAM_DQ(1)	T28 SDRAM_DQ(0)	T29 BufR_W_n	T30 VCCAUX
U1	U2	U3	U4	U5	U6 GND	U7	U8	U9	U10 VCCO_3	U11 VCCINT	U12 GND	U13 GND	U14 GND	U15 GND	U16 GND	U17 GND	U18 GND	U19 GND	U20 VCCINT	U21 VCCO_6	U22 SDRAM_BA(0)	U23 SDRAM_A(11)	U24 SDRAM_CS_n	U25 GND	U26 SDRAM_RAS_n	U27 SDRAM_CAS_n	U28 SDRAM_WE_n	U29 SDRAM_DQM(0)	U30 SDRAM_DQ(7)
V1 A21_Select	V2	V3	V4	V5	V6	V7	V8	V9 VCCO_3	V10 VCCO_3	V11 VCCINT	V12 GND	V13 GND	V14 GND	V15 GND	V16 GND	V17 GND	V18 GND	V19 GND	V20 VCCINT	V21 VCCO_6	V22 VCCO_6	V23 SDRAM_DQ(17)	V24 SDRAM_DQ(16)	V25 SDRAM_DQM(2)	V26 SDRAM_A(2)	V27 SDRAM_A(1)	V28 SDRAM_A(0)	V29 SDRAM_A(10)	V30 SDRAM_BA(1)
W1 Adr(21)	W2 MS0_n	W3 MS1_n	W4 MS2_n	W5 MS3_n	W6 DMAR_n	W7	W8	W9 VCCO_3	W10 VCCO_3	W11 VCCINT	W12 GND	W13 GND	W14 GND	W15 GND	W16 GND	W17 GND	W18 GND	W19 GND	W20 VCCINT	W21 VCCO_6	W22 VCCO_6	W23 SDRAM_DQ(25)	W24 SDRAM_DQ(24)	W25 SDRAM_DQM(3)	W26 SDRAM_DQ(22)	W27 SDRAM_DQ(21)	W28 SDRAM_DQ(20)	W29 SDRAM_DQ(19)	W30 SDRAM_DQ(18)
Y1 Adr(17)	Y2 Adr(18)	Y3 GND	Y4 Adr(19)	Y5 Adr(20)	Y6 GND	Y7	Y8	Y9 VCCO_3	Y10 VCCO_3	Y11 GND	Y12 VCCINT	Y13 VCCINT	Y14 VCCINT	Y15 VCCINT	Y16 VCCINT	Y17 VCCINT	Y18 VCCINT	Y19 VCCINT	Y20 GND	Y21 VCCO_6	Y22 VCCO_6	Y23	Y24	Y25 GND	Y26 SDRAM_DQ(29)	Y27 SDRAM_DQ(28)	Y28 GND	Y29 SDRAM_DQ(27)	Y30 SDRAM_DQ(26)
AA1 Adr(11)	AA2 Adr(12)	AA3 Adr(13)	AA4 Adr(14)	AA5 Adr(15)	AA6 Adr(16)	AA7	AA8	AA9 VCCO_3	AA10 VCCO_4	AA11 VCCO_4	AA12 VCCO_4	AA13 VCCO_4	AA14 VCCO_4	AA15 VCCO_4	AA16 VCCO_5	AA17 VCCO_5	AA18 VCCO_5	AA19 VCCO_5	AA20 VCCO_5	AA21 VCCO_5	AA22 VCCO_6	AA23	AA24	AA25 SDRAM_A(5)	AA26 SDRAM_A(4)	AA27 SDRAM_A(3)	AA28 SDRAM_DQM(3)	AA29 SDRAM_DQ(31)	AA30 SDRAM_DQ(30)
AB1 Adr(7)	AB2 Adr(8)	AB3 Adr(9)	AB4 Adr(10)	AB5	AB6	AB7	AB8	AB9 VCCO_3	AB10 VCCO_4	AB11 VCCO_4	AB12 VCCO_4	AB13 VCCO_4	AB14	AB15 Data(3)	AB16 IRQ2_n	AB17	AB18 VCCO_5	AB19 VCCO_5	AB20 VCCO_5	AB21 VCCO_5	AB22 VCCO_6	AB23	AB24	AB25	AB26	AB27 SDRAM_A(9)	AB28 SDRAM_A(8)	AB29 SDRAM_A(7)	AB30 SDRAM_A(6)
AC1 GND	AC2 Adr(4)	AC3 Adr(5)	AC4 Adr(6)	AC5	AC6	AC7 CCLK	AC8 DONE	AC9 D0	AC10 Data(16)	AC11 Data(11)	AC12 Data(9)	AC13	AC14	AC15 Data(2)	AC16 IRQ1_n	AC17	AC18	AC19 TestCon(8)	AC20 TestCon(9)	AC21 TestCon(10)	AC22 D7	AC23 M2	AC24 M1	AC25	AC26	AC27 SDRAM_DQM(1)	AC28 SDRAM_A(12)	AC29 SDRAM_CKE	AC30 GND
AD1	AD2	AD3	AD4	AD5 Adr(2)	AD6 Adr(3)	AD7 PWRDWN_B	AD8	AD9 D1	AD10 Data(15)	AD11 Data(10)	AD12 Data(8)	AD13	AD14 Data(7)	AD15 Data(1)	AD16 IRQ0_n	AD17	AD18	AD19 TestCon(11)	AD20 TestCon(12)	AD21 TestCon(13)	AD22 D6	AD23	AD24 M0	AD25 SDRAM_DQ(9)	AD26 SDRAM_DQ(8)	AD27	AD28	AD29	AD30
AE1	AE2	AE3	AE4	AE5	AE6 GND	AE7 Data(25)	AE8 Data(24)	AE9 Data(20)	AE10 Data(14)	AE11	AE12	AE13 GND	AE14 Data(6)	AE15 Data(0)	AE16 Empty	AE17	AE18 GND	AE19	AE20	AE21	AE22	AE23	AE24	AE25 GND	AE26	AE27	AE28	AE29	AE30
AF1	AF2	AF3	AF4	AF5 GND	AF6	AF7 INIT_B	AF8 Data(23)	AF9 Data(19)	AF10 Data(13)	AF11	AF12	AF13	AF14 Data(5)	AF15 SDRAM_CLKin	AF16 SDRAM_CLK	AF17	AF18	AF19	AF20	AF21 TTC_n(7)	AF22 TTC_n(6)	AF23 TTC_n(4)	AF24 RDWR_B	AF25	AF26 GND	AF27	AF28	AF29	AF30
AG1 Data(30)	AG2 Data(31)	AG3 Adr(0)	AG4 GND	AG5 Adr(1)	AG6 DOUT	AG7 D2	AG8 VRP_4	AG9 GND	AG10 Data(12)	AG11	AG12 GND	AG13	AG14 Data(4)	AG15 SharcWr_n	AG16 LHC_Clk	AG17 ChaBusy	AG18	AG19 GND	AG20	AG21 TTC_n(5)	AG22 GND	AG23 VRN_5	AG24 D5	AG25 CS_B	AG26 SDRAM_DQ(13)	AG27 GND	AG28 SDRAM_DQ(12)	AG29 SDRAM_DQ(11)	AG30 SDRAM_DQ(10)
AH1 Data(26)	AH2 Data(27)	AH3 GND	AH4 Data(28)	AH5 Data(29)	AH6 GNDA16	AH7 D3	AH8 VRN_4	AH9 Data(18)	AH10	AH11	AH12 GNDA18	AH13	AH14 GND	AH15 SharcRd_n	AH16 Clk	AH17 GND	AH18	AH19 GNDA19	AH20	AH21	AH22 TTC_n(3)	AH23 VRP_5	AH24 D4	AH25 GNDA21	AH26	AH27	AH28 GND	AH29 SDRAM_DQ(15)	AH30 SDRAM_DQ(14)
AJ1 VCCAUX	AJ2 GND	AJ3 VRP_3	AJ4 AVCCAUXRX16	AJ5 VTRXPAD16	AJ6 AVCCAUXTX16	AJ7 VTTXPAD16	AJ8 Data(22)	AJ9 Data(17)	AJ10	AJ11 AVCCAUXRX18	AJ12 VTRXPAD18	AJ13 AVCCAUXTX18	AJ14 VTTXPAD18	AJ15 Rocket_XC1k	AJ16 Clkx2	AJ17 AVCCAUXRX19	AJ18 VTRXPAD19	AJ19 AVCCAUXTX19	AJ20 VTTXPAD19	AJ21	AJ22 TTC_n(2)	AJ23 TTC_n(1)	AJ24 AVCCAUXRX21	AJ25 VTRXPAD21	AJ26 AVCCAUXTX21	AJ27 VTTXPAD21	AJ28 VRP_6	AJ29 GND	AJ30 VCCAUX
	AK2 VCCAUX	AK3 VRN_3	AK4	AK5	AK6	AK7	AK8 Data(21)	AK9 GND	AK10	AK11	AK12	AK13	AK14	AK15 VCCAUX	AK16 VCCAUX	AK17 ROCKET_LVDS T Rocket_RXN	AK18 ROCKET_LVDS T Rocket_RXP	AK19 ROCKET_LVDS S Rocket_TXP	AK20 ROCKET_LVDS S Rocket_TXN	AK21	AK22 GND	AK23 TTC_n(0)	AK24	AK25	AK26	AK27	AK28 VRN_6	AK29 VCCAUX	

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

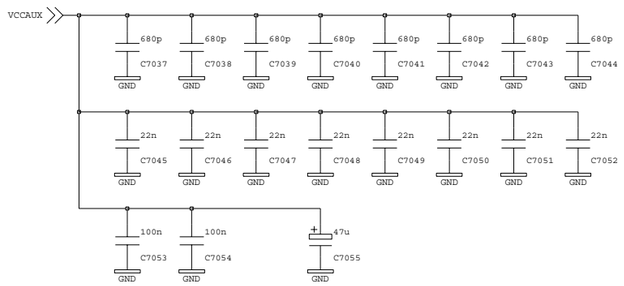
channel_in	Rev V2 2
	Date 7 Feb 2006
Input FPGA	Time 1:50:53 pm
Proj: MROD-X	Proj.No: 38405
	Name tonvr
Peter Jansweijer	peterj@nikhef.nl
	Size A3 4 1 4 A
NIKHEF © ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND
	Dim 420 x 297 mm
	Page 2 of 6

XC2VP7/20 VCCINT Decoupling Capacitors
Min. Power-On Current XC2VP20
IccINT = 600 mA



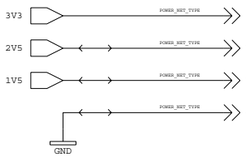
AVX TAJB476K010R

XC2VP7/20 VCCAUX Decoupling Capacitors
Min. Power-On Current XC2VP20
IccAUX = 250 mA (min)



AVX TAJB476K010R

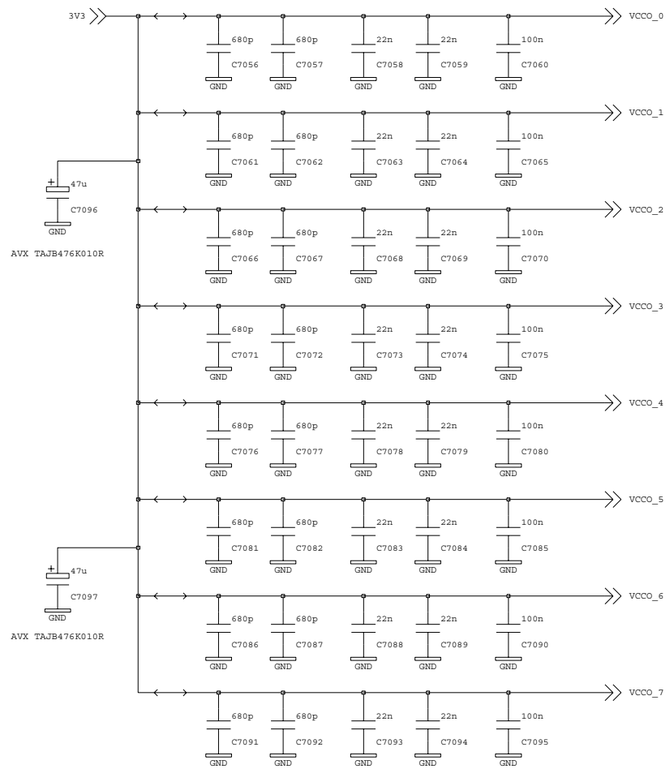
Power Inputs
For Xilinx Virtex-II Pro, power supplies
can be turned on in any sequence.



VCCAUX and VCCO can ramp up at any rate

VCCINT Ramp rate 200 us min. and 50 ms max.

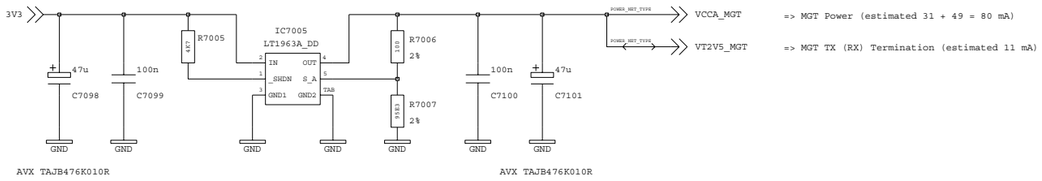
All GND nets on the FPGA need
to be connected to golbal GROUND.

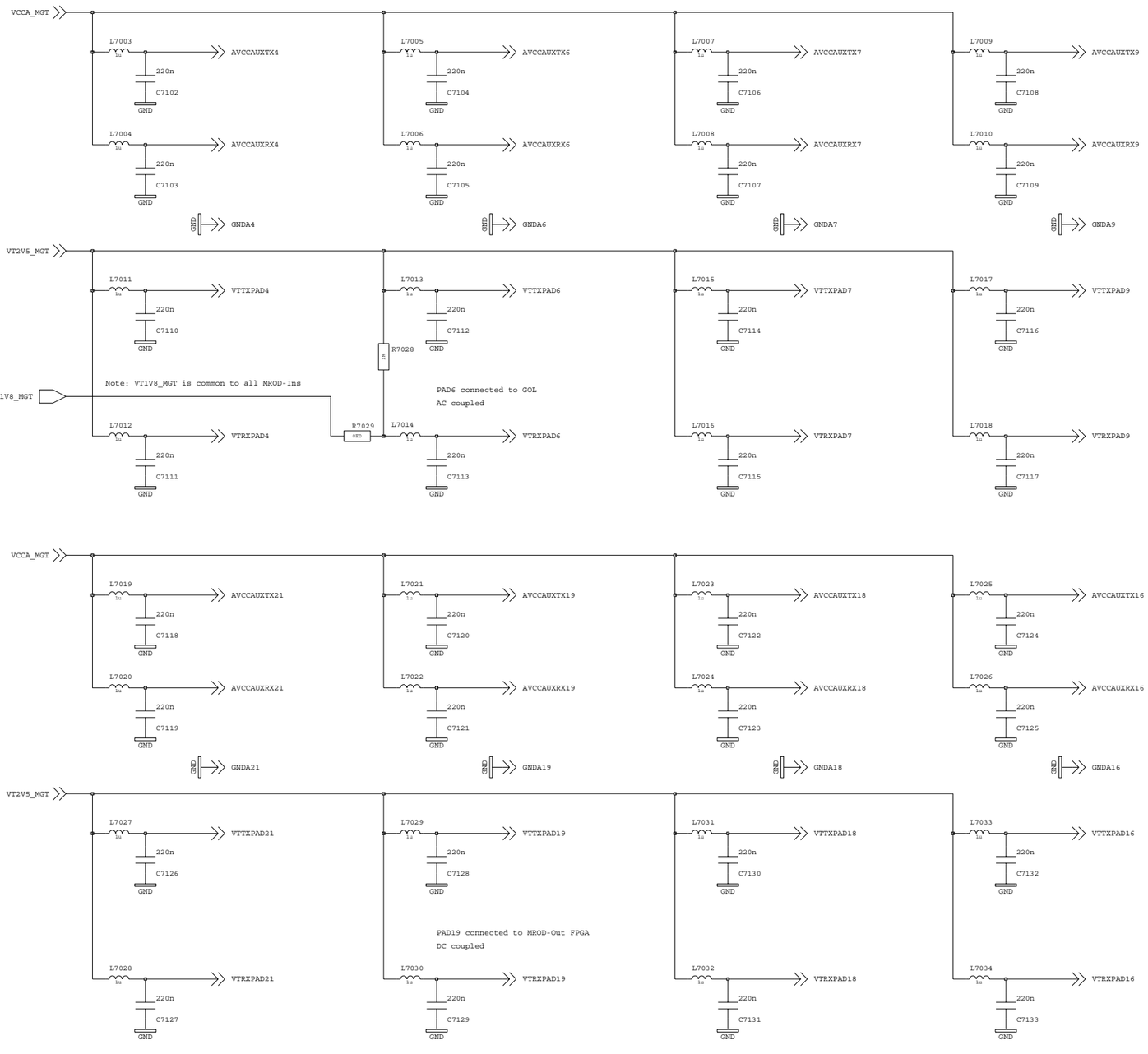


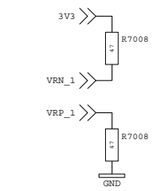
AVX TAJB476K010R

channel_in		Rev V2 2
		Date 7 Feb 2006
Input FPGA Power Supply Decoupling		Time 1:51:34 pm
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© BT-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 3 of 6

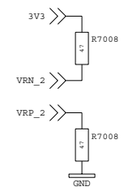
2V5 @ 1,5A



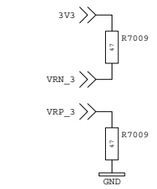




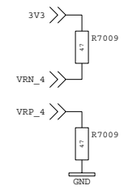
Series Termination for
Not (yet) used



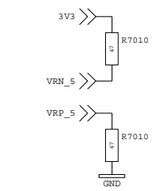
Series Termination for
Not (yet) used



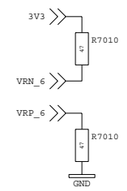
Series Termination for
Sharc Addressbus



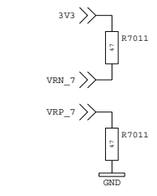
Series Termination for
Sharc Databus



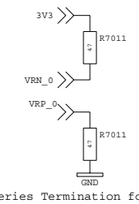
Series Termination for
General purpose



Series Termination for
SDRAM interface



Series Termination for
Buffer Memory interface



Series Termination for
General purpose

channel_in

Input FPGA MGT Pwr Decoupling, Termination

Proj: MROD-X | Proj.No: 38405

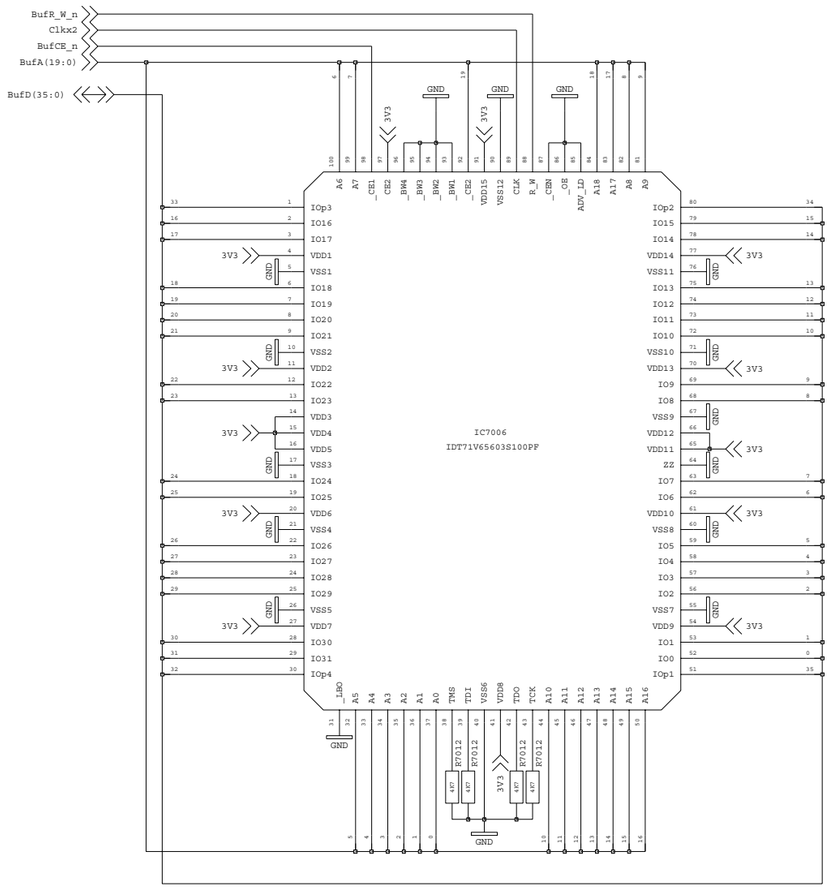
Peter Jansweijer | peterj@nikhef.nl

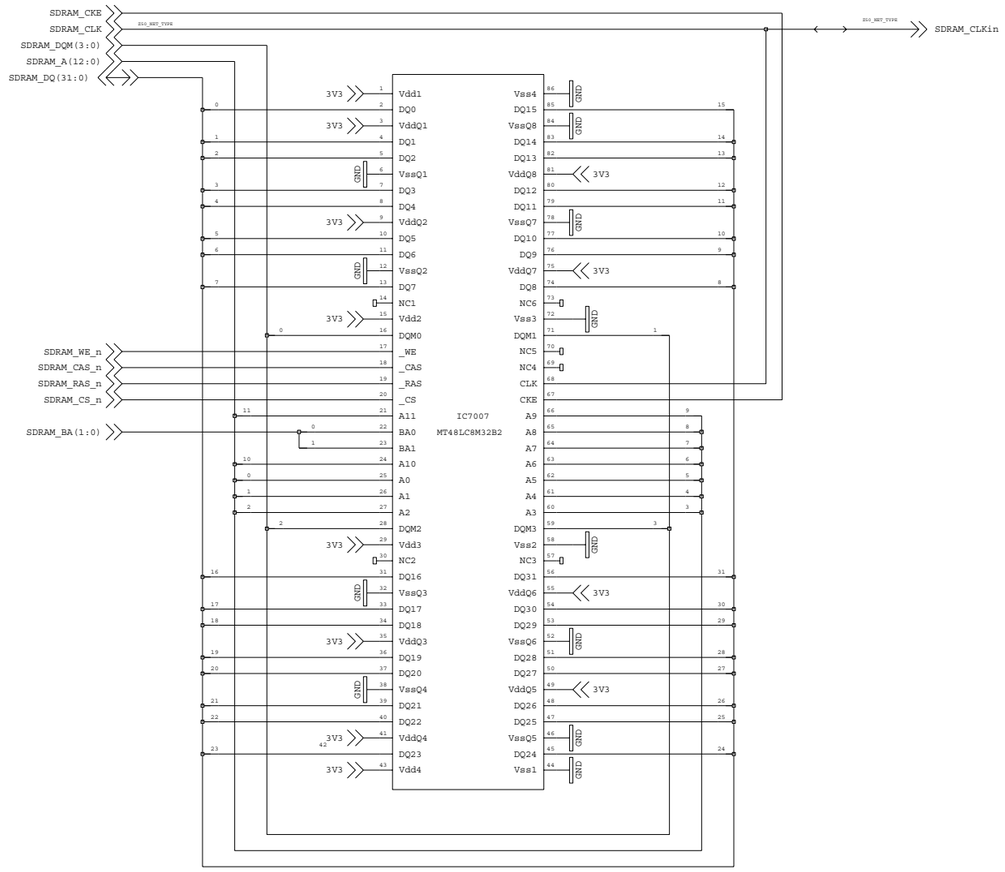
NIKHEF

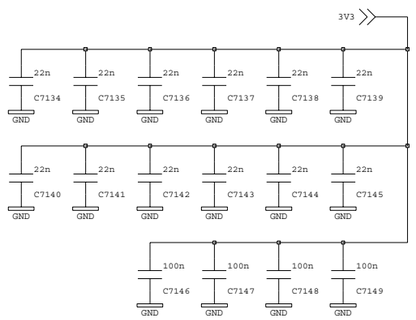
NATIONAAL INSTITUUT VOOR KERN-
FYSICA EN HOGE ENERGIE-FYSICA
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND

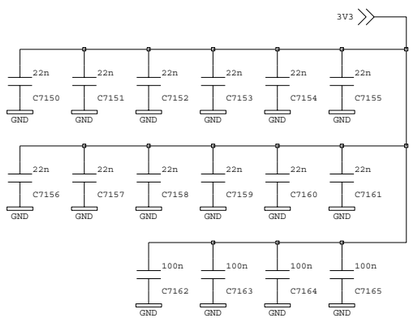
Rev	V2 2
Date	7 Feb 2006
Time	1:52:01 pm
Name	tonvr
Size	A3 — 4 1 4 A
Dim	420 x 297 mm
Page	4 of 6

SDRAM_A(12) is not connected

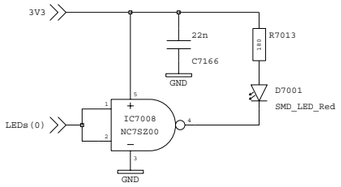


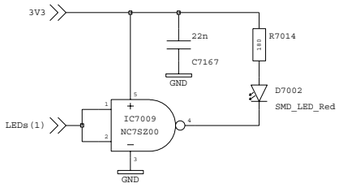


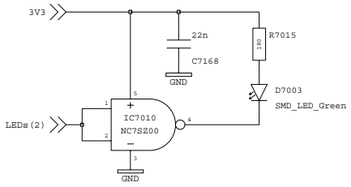


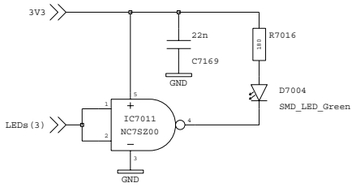


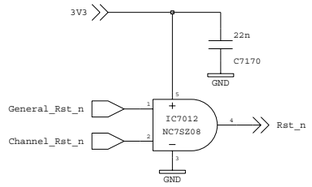
channel_in		Rev	V2 2
		Date	7 Feb 2006
Buffer Memory (ZBT and SDRAM)		Time	1:52:29 pm
Proj: MROD-X	Proj.No: 38405	Name	Ton van Reen
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size	A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim	420 x 297 mm
		Page	5 of 6



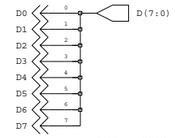


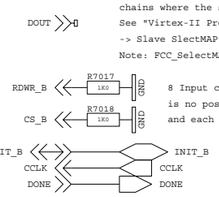






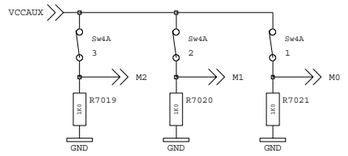
Fiducial7001 Fiducial7002





DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices.
See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SlectMAP programming Mode -> BUSY.
Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!

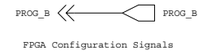
8 Input channels are loaded in parallel so there is no possibility for readback (RDWR_B = '0')
and each CS_B = '0'



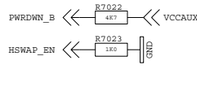
M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.

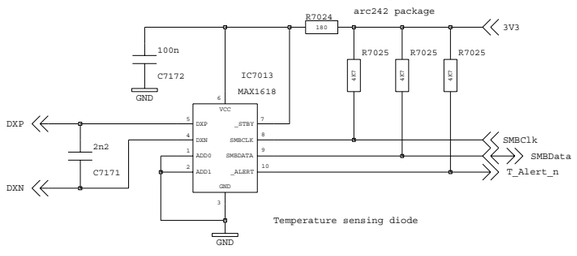


FPGA Configuration Signals



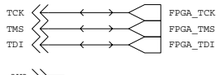
PWRDWN_B is unsupported (should be pulled high)

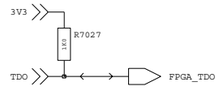
HSWAP_EN = '0' => User IOs have pull-up resistors during configuration



VBATT is decriptor key memory backup supply

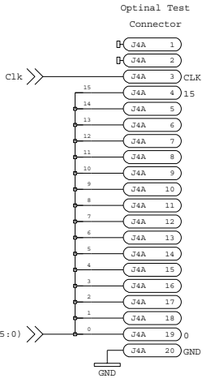
FPGA Control signals



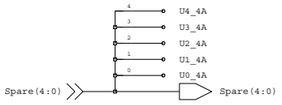


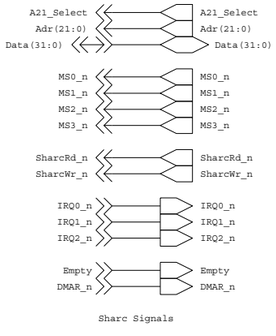
FPGA JTAG Signals

Optinal Test Connector



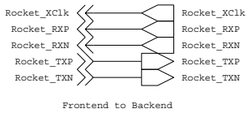
Testpoints force Spare lines to be accessible.



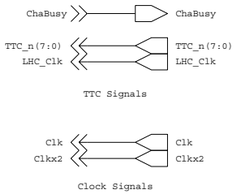


Sharc Signals

Input Channel ID bits



Frontend to Backend
Rocket IO Signals



TTC Signals

Clock Signals

channel_in	Rev V2 2
	Date 7 Feb 2006
	Time 1:53:04 pm
	Name Ton van Reen
Input FPGA Auxiliary Connections	
Proj: MROD-X	Proj.No: 38405
Peter Jansweijer	peterj@nikhef.nl
	Size A3 4 1 4 A
NIKHEF	Dim 420 x 297 mm
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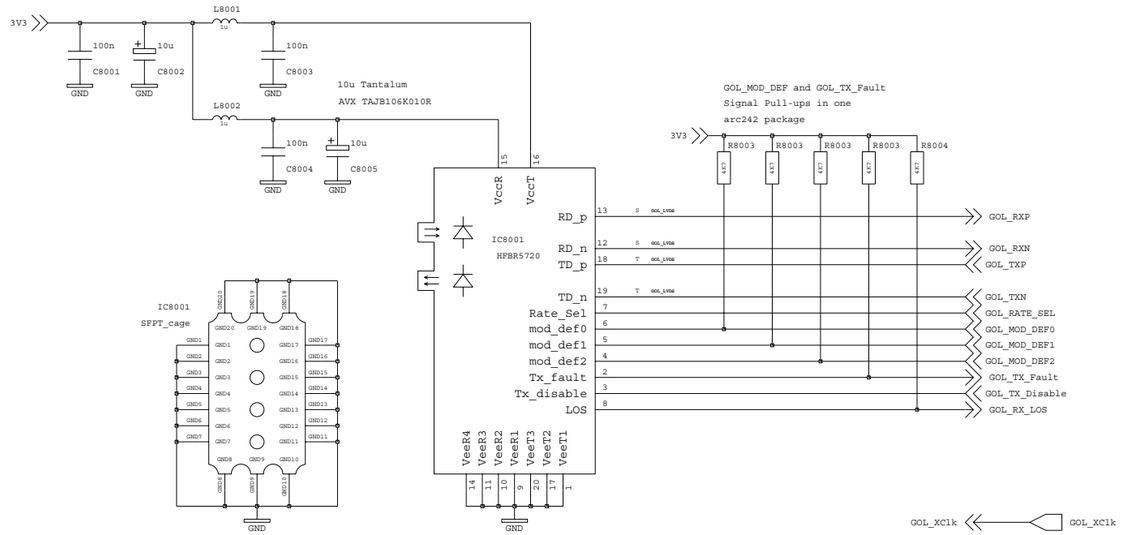
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND



channel_in	Rev V2 2
	Date 7 Feb 2006
	Time 1:50:33 pm
GOL Input	Name tonvr
Proj: MROD-X / Proj.No: 38405	
Peter Jansweijer / peterj@nikhef.nl	
NIKHEF	Size A3 / 4 1 4 A
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
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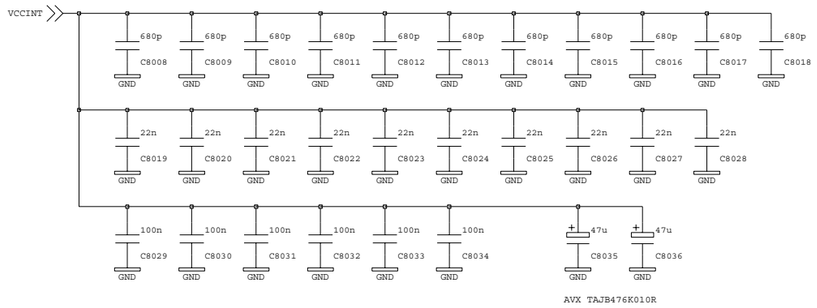
IC8004
XC2VP7FF896

	A2 VCCAUX	A3 VRP_2	A4	A5	A6	A7	A8	A9 GND	A10	A11	A12	A13	A14	A15 VCCAUX	A16 VCCAUX	A17 GOL_LVDS GOL_LVDS T DP_GOL_RX4B	A18 GOL_LVDS GOL_LVDS T DP_GOL_RX4B	A19 GOL_LVDS GOL_LVDS S DP_GOL_TX4B	A20 GOL_LVDS GOL_LVDS S DP_GOL_TX4B	A21	A22 GND	A23 LEDs(0)	A24	A25	A26	A27	A28 VRP_7	A29 VCCAUX	
B1 VCCAUX	B2 GND	B3 VRN_2	B4 AVCCAUXRX9	B5 VTRXPAD9	B6 AVCCAUXTX9	B7 VTTXPAD9	B8	B9	B10	B11 AVCCAUXRX7	B12 VTRXPAD7	B13 AVCCAUXTX7	B14 VTTXPAD7	B15	B16 GOL_Xclk	B17 AVCCAUXRX6	B18 VTRXPAD6	B19 AVCCAUXTX6	B20 VTTXPAD6	B21	B22	B23 LEDs(1)	B24 AVCCAUXRX4	B25 VTRXPAD4	B26 AVCCAUXTX4	B27 VTTXPAD4	B28 VRN_7	B29 GND	B30 VCCAUX
C1	C2	C3 GND	C4	C5	C6 GNDA9	C7	C8	C9	C10	C11	C12 GNDA7	C13	C14 GND	C15	C16	C17 GND	C18 UpLED	C19 GNDA6	C20	C21	C22	C23 LEDs(2)	C24 LEDs(3)	C25 GNDA4	C26 BufA(6)	C27 BufA(7)	C28 GND	C29 BufCE_n	C30 BufA(19)
D1	D2	D3 GND	D4	D5	D6	D7	D8	D9 GND	D10	D11	D12 GND	D13	D14	D15	D16 GOL_RX_LOS	D17 GOL_TX_Disable	D18 ErrLED	D19 GND	D20 GOL_MOD_DEF1	D21 GOL_MOD_DEF0	D22 GND	D23 ChaID(1)	D24 ChaID(0)	D25 DXN	D26 BufD(16)	D27 GND	D28 BufD(33)	D29	D30
E1	E2	E3	E4 GND	E5	E6 VRN_1	E7 VRP_1	E8	E9	E10	E11	E12	E13	E14	E15	E16	R17 GOL_TX_Fault	E18	E19	E20 GOL_MOD_DEF2	E21 GOL_RATE_SEL	E22	E23 ChaID(2)	E24 VRN_0	E25 VRP_0	E26 GND	E27	E28	E29	E30
F1	F2	F3	F4	F5 TDO	F6 GND	F7	F8	F9	F10	F11	F12	F13 GND	F14	F15	F16	F17	F18 GND	F19	F20	F21 TestCon(1)	F22 TestCon(0)	F23	F24	F25 GND	F26 TDI	F27	F28	F29	F30
G1	G2	G3	G4	G5	G6	G7 TCK	G8	G9	G10	G11	G12	G13	G14	G15	G16 Rst_n	G17	G18	G19 TestCon(6)	G20 TestCon(5)	G21 TestCon(4)	G22 TestCon(3)	G23 TestCon(2)	G24 PROG_B	G25 BufD(18)	G26 BufD(17)	G27	G28	G29	G30
H1 GND	H2	H3	H4	H5	H6	H7 VBATT	H8 TMS	H9	H10	H11	H12 TestCon(15)	H13	H14	H15	H16	H17	H18	H19 TestCon(7)	H20 T_Alert_n	H21 SMBData	H22 SMBClk	H23 HSWAP_EN	H24 DXP	H25	H26	H27	H28	H29 BufD(19)	H30 GND
J1	J2	J3	J4	J5	J6	J7	J8 TestCon(14)	J9 VCCO_2	J10 VCCO_1	J11 VCCO_1	J12 VCCO_1	J13 VCCO_1	J14	J15	J16	J17	J18 VCCO_0	J19 VCCO_0	J20 VCCO_0	J21 VCCO_0	J22 VCCO_7	J23 BufD(25)	J24 BufD(24)	J25	J26	J27 BufD(23)	J28 BufD(22)	J29 BufD(21)	J30 BufD(20)
K1	K2	K3	K4	K5	K6	K7	K8	K9 VCCO_2	K10 VCCO_1	K11 VCCO_1	K12 VCCO_1	K13 VCCO_1	K14 VCCO_1	K15 VCCO_1	K16 VCCO_0	K17 VCCO_0	K18 VCCO_0	K19 VCCO_0	K20 VCCO_0	K21 VCCO_0	K22 VCCO_7	K23	K24	K25 BufD(31)	K26 BufD(30)	K27 BufD(29)	K28 BufD(28)	K29 BufD(27)	K30 BufD(26)
L1	L2	L3 GND	L4	L5	L6 GND	L7	L8	L9 VCCO_2	L10 VCCO_2	L11 GND	L12 VCCINT	L13 VCCINT	L14 VCCINT	L15 VCCINT	L16 VCCINT	L17 VCCINT	L18 VCCINT	L19 VCCINT	L20 GND	L21 VCCO_7	L22 VCCO_7	L23	L24	L25 GND	L26 BufA(3)	L27 BufA(4)	L28 GND	L29 BufA(5)	L30 BufD(32)
M1	M2	M3	M4	M5	M6	M7	M8	M9 VCCO_2	M10 VCCO_2	M11 VCCINT	M12 GND	M13 GND	M14 GND	M15 GND	M16 GND	M17 GND	M18 GND	M19 GND	M20 VCCINT	M21 VCCO_7	M22 VCCO_7	M23 BufA(14)	M24 BufA(13)	M25 BufA(12)	M26 BufA(11)	M27 BufA(10)	M28 BufA(0)	M29 BufA(1)	M30 BufA(2)
N1	N2	N3	N4	N5	N6	N7	N8	N9 VCCO_2	N10 VCCO_2	N11 VCCINT	N12 GND	N13 GND	N14 GND	N15 GND	N16 GND	N17 GND	N18 GND	N19 GND	N20 VCCINT	N21 VCCO_7	N22 VCCO_7	N23 BufD(4)	N24 BufD(3)	N25 BufD(2)	N26 BufD(1)	N27 BufD(0)	N28 BufD(35)	N29 BufA(16)	N30 BufA(15)
P1	P2	P3	P4	P5	P6 GND	P7	P8	P9	P10 VCCO_2	P11 VCCINT	P12 GND	P13 GND	P14 GND	P15 GND	P16 GND	P17 GND	P18 GND	P19 GND	P20 VCCINT	P21 VCCO_7	P22 BufD(12)	P23 BufD(11)	P24 BufD(10)	P25 GND	P26 BufD(9)	P27 BufD(8)	P28 BufD(7)	P29 BufD(6)	P30 BufD(5)
R1 VCCAUX	R2	R3	R4	R5	R6	R7	R8	R9	R10 VCCO_2	R11 VCCINT	R12 GND	R13 GND	R14 GND	R15 GND	R16 GND	R17 GND	R18 GND	R19 GND	R20 VCCINT	R21 VCCO_7	R22 BufA(18)	R23 BufA(17)	R24 BufA(8)	R25 BufA(9)	R26 BufD(34)	R27 BufD(15)	R28 BufD(14)	R29 BufD(13)	R30 VCCAUX
T1 VCCAUX	T2	T3	T4	T5 Spare(4)	T6 Spare(3)	T7 Spare(2)	T8 Spare(1)	T9 Spare(0)	T10 VCCO_3	T11 VCCINT	T12 GND	T13 GND	T14 GND	T15 GND	T16 GND	T17 GND	T18 GND	T19 GND	T20 VCCINT	T21 VCCO_6	T22 SDRAM_DQ(6)	T23 SDRAM_DQ(5)	T24 SDRAM_DQ(4)	T25 SDRAM_DQ(3)	T26 SDRAM_DQ(2)	T27 SDRAM_DQ(1)	T28 SDRAM_DQ(0)	T29 BufR_W_n	T30 VCCAUX
U1	U2	U3	U4	U5	U6 GND	U7	U8	U9	U10 VCCO_3	U11 VCCINT	U12 GND	U13 GND	U14 GND	U15 GND	U16 GND	U17 GND	U18 GND	U19 GND	U20 VCCINT	U21 VCCO_6	U22 SDRAM_BA(0)	U23 SDRAM_A(11)	U24 SDRAM_CS_n	U25 GND	U26 SDRAM_RAS_n	U27 SDRAM_CAS_n	U28 SDRAM_WE_n	U29 SDRAM_DQM(0)	U30 SDRAM_DQ(7)
V1 A21_Select	V2	V3	V4	V5	V6	V7	V8	V9 VCCO_3	V10 VCCO_3	V11 VCCINT	V12 GND	V13 GND	V14 GND	V15 GND	V16 GND	V17 GND	V18 GND	V19 GND	V20 VCCINT	V21 VCCO_6	V22 VCCO_6	V23 SDRAM_DQ(17)	V24 SDRAM_DQ(16)	V25 SDRAM_DQM(2)	V26 SDRAM_A(2)	V27 SDRAM_A(1)	V28 SDRAM_A(0)	V29 SDRAM_A(10)	V30 SDRAM_BA(1)
W1 Adr(21)	W2 MS0_n	W3 MS1_n	W4 MS2_n	W5 MS3_n	W6 DMAR_n	W7	W8	W9 VCCO_3	W10 VCCO_3	W11 VCCINT	W12 GND	W13 GND	W14 GND	W15 GND	W16 GND	W17 GND	W18 GND	W19 GND	W20 VCCINT	W21 VCCO_6	W22 VCCO_6	W23 SDRAM_DQ(25)	W24 SDRAM_DQ(24)	W25 SDRAM_DQ(23)	W26 SDRAM_DQ(22)	W27 SDRAM_DQ(21)	W28 SDRAM_DQ(20)	W29 SDRAM_DQ(19)	W30 SDRAM_DQ(18)
Y1 Adr(17)	Y2 Adr(18)	Y3 GND	Y4 Adr(19)	Y5 Adr(20)	Y6 GND	Y7	Y8	Y9 VCCO_3	Y10 VCCO_3	Y11 GND	Y12 VCCINT	Y13 VCCINT	Y14 VCCINT	Y15 VCCINT	Y16 VCCINT	Y17 VCCINT	Y18 VCCINT	Y19 VCCINT	Y20 GND	Y21 VCCO_6	Y22 VCCO_6	Y23	Y24	Y25 GND	Y26 SDRAM_DQ(29)	Y27 SDRAM_DQ(28)	Y28 GND	Y29 SDRAM_DQ(27)	Y30 SDRAM_DQ(26)
AA1 Adr(11)	AA2 Adr(12)	AA3 Adr(13)	AA4 Adr(14)	AA5 Adr(15)	AA6 Adr(16)	AA7	AA8	AA9 VCCO_3	AA10 VCCO_4	AA11 VCCO_4	AA12 VCCO_4	AA13 VCCO_4	AA14 VCCO_4	AA15 VCCO_4	AA16 VCCO_5	AA17 VCCO_5	AA18 VCCO_5	AA19 VCCO_5	AA20 VCCO_5	AA21 VCCO_5	AA22 VCCO_6	AA23	AA24	AA25 SDRAM_A(5)	AA26 SDRAM_A(4)	AA27 SDRAM_A(3)	AA28 SDRAM_DQM(3)	AA29 SDRAM_DQ(31)	AA30 SDRAM_DQ(30)
AB1 Adr(7)	AB2 Adr(8)	AB3 Adr(9)	AB4 Adr(10)	AB5	AB6	AB7	AB8	AB9 VCCO_3	AB10 VCCO_4	AB11 VCCO_4	AB12 VCCO_4	AB13 VCCO_4	AB14	AB15 Data(3)	AB16 IRQ2_n	AB17	AB18 VCCO_5	AB19 VCCO_5	AB20 VCCO_5	AB21 VCCO_5	AB22 VCCO_6	AB23	AB24	AB25	AB26	AB27 SDRAM_A(9)	AB28 SDRAM_A(8)	AB29 SDRAM_A(7)	AB30 SDRAM_A(6)
AC1 GND	AC2 Adr(4)	AC3 Adr(5)	AC4 Adr(6)	AC5	AC6	AC7 CCLK	AC8 DONE	AC9 D0	AC10 Data(16)	AC11 Data(11)	AC12 Data(9)	AC13	AC14	AC15 Data(2)	AC16 IRQ1_n	AC17	AC18	AC19 TestCon(8)	AC20 TestCon(9)	AC21 TestCon(10)	AC22 D7	AC23 M2	AC24 M1	AC25	AC26	AC27 SDRAM_DQM(1)	AC28 SDRAM_A(12)	AC29 SDRAM_CKE	AC30 GND
AD1	AD2	AD3	AD4	AD5 Adr(2)	AD6 Adr(3)	AD7 PWRDWN_B	AD8	AD9 D1	AD10 Data(15)	AD11 Data(10)	AD12 Data(8)	AD13	AD14 Data(7)	AD15 Data(1)	AD16 IRQ0_n	AD17	AD18	AD19 TestCon(11)	AD20 TestCon(12)	AD21 TestCon(13)	AD22 D6	AD23	AD24 M0	AD25 SDRAM_DQ(9)	AD26 SDRAM_DQ(8)	AD27	AD28	AD29	AD30
AE1	AE2	AE3	AE4	AE5	AE6 GND	AE7 Data(25)	AE8 Data(24)	AE9 Data(20)	AE10 Data(14)	AE11	AE12	AE13 GND	AE14 Data(6)	AE15 Data(0)	AE16 Empty	AE17	AE18 GND	AE19	AE20	AE21	AE22	AE23	AE24	AE25 GND	AE26	AE27	AE28	AE29	AE30
AF1	AF2	AF3	AF4	AF5 GND	AF6	AF7 INIT_B	AF8 Data(23)	AF9 Data(19)	AF10 Data(13)	AF11	AF12	AF13	AF14 Data(5)	AF15 SDRAM_CLKin	AF16 SDRAM_CLK	AF17	AF18	AF19	AF20	AF21 TTC_n(7)	AF22 TTC_n(6)	AF23 TTC_n(4)	AF24 RDWR_B	AF25	AF26 GND	AF27	AF28	AF29	AF30
AG1 Data(30)	AG2 Data(31)	AG3 Adr(0)	AG4 GND	AG5 Adr(1)	AG6 DOUT	AG7 D2	AG8 VRP_4	AG9 GND	AG10 Data(12)	AG11	AG12 GND	AG13	AG14 Data(4)	AG15 SharcWr_n	AG16 LHC_Clk	AG17 ChaBusy	AG18	AG19 GND	AG20	AG21 TTC_n(5)	AG22 GND	AG23 VRN_5	AG24 D5	AG25 CS_B	AG26 SDRAM_DQ(13)	AG27 GND	AG28 SDRAM_DQ(12)	AG29 SDRAM_DQ(11)	AG30 SDRAM_DQ(10)
AH1 Data(26)	AH2 Data(27)	AH3 GND	AH4 Data(28)	AH5 Data(29)	AH6 GNDA16	AH7 D3	AH8 VRN_4	AH9 Data(18)	AH10	AH11	AH12 GNDA18	AH13	AH14 GND	AH15 SharcRd_n	AH16 Clk	AH17 GND	AH18	AH19 GNDA19	AH20	AH21	AH22 TTC_n(3)	AH23 VRP_5	AH24 D4	AH25 GNDA21	AH26	AH27	AH28 GND	AH29 SDRAM_DQ(15)	AH30 SDRAM_DQ(14)
AJ1 VCCAUX	AJ2 GND	AJ3 VRP_3	AJ4 AVCCAUXRX16	AJ5 VTRXPAD16	AJ6 AVCCAUXTX16	AJ7 VTTXPAD16	AJ8 Data(22)	AJ9 Data(17)	AJ10	AJ11 AVCCAUXRX18	AJ12 VTRXPAD18	AJ13 AVCCAUXTX18	AJ14 VTTXPAD18	AJ15 Rocket_XC1k	AJ16 Clkx2	AJ17 AVCCAUXRX19	AJ18 VTRXPAD19	AJ19 AVCCAUXTX19	AJ20 VTTXPAD19	AJ21	AJ22 TTC_n(2)	AJ23 TTC_n(1)	AJ24 AVCCAUXRX21	AJ25 VTRXPAD21	AJ26 AVCCAUXTX21	AJ27 VTTXPAD21	AJ28 VRP_6	AJ29 GND	AJ30 VCCAUX
	AK2 VCCAUX	AK3 VRN_3	AK4	AK5	AK6	AK7	AK8 Data(21)	AK9 GND	AK10	AK11	AK12	AK13	AK14	AK15 VCCAUX	AK16 VCCAUX	AK17 ROCKET_LVDS ROCKET_LVDS T Rocket_RXN	AK18 ROCKET_LVDS ROCKET_LVDS T Rocket_RXP	AK19 ROCKET_LVDS ROCKET_LVDS S Rocket_TXP	AK20 ROCKET_LVDS ROCKET_LVDS S Rocket_TXN	AK21	AK22 GND	AK23 TTC_n(0)	AK24	AK25	AK26	AK27	AK28 VRN_6	AK29 VCCAUX	

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

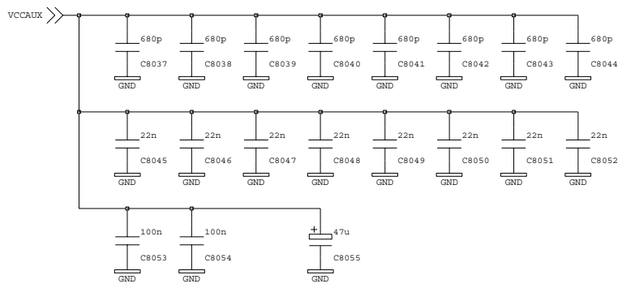
channel_in	Rev V2 2
Input FPGA	Date 7 Feb 2006
Proj: MROD-X	Time 1:50:53 pm
Peter Jansweijer	Proj.No: 38405
NIKHEF	Name tonvr
ET-Nikhef Amsterdam	Size A3 4 1 4 A
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
peterj@nikhef.nl	Page 2 of 6

XC2VP7/20 VCCINT Decoupling Capacitors
Min. Power-On Current XC2VP20
IccINT = 600 mA



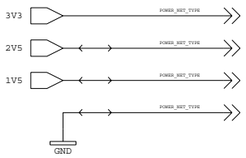
AVX TAJB476K010R

XC2VP7/20 VCCAUX Decoupling Capacitors
Min. Power-On Current XC2VP20
IccAUX = 250 mA (min)



AVX TAJB476K010R

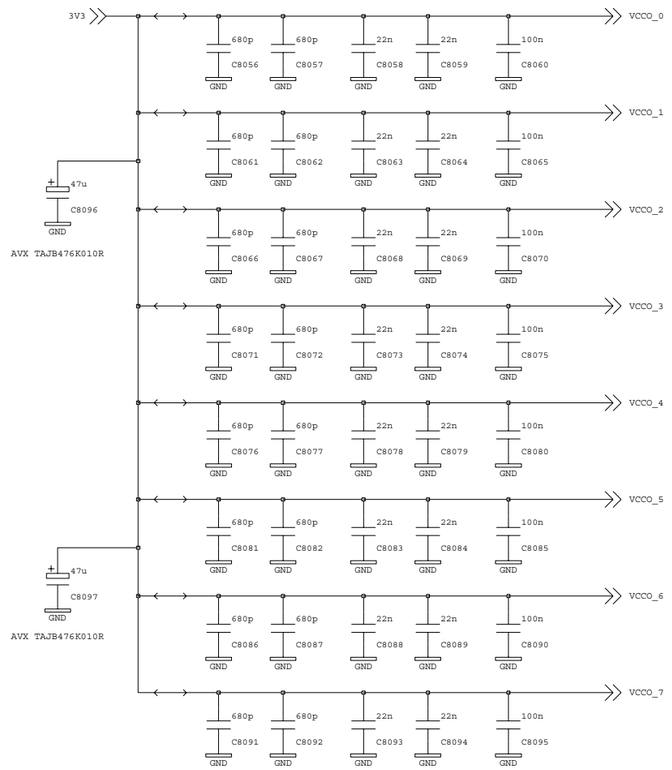
Power Inputs
For Xilinx Virtex-II Pro, power supplies
can be turned on in any sequence.



VCCAUX and VCCO can ramp up at any rate

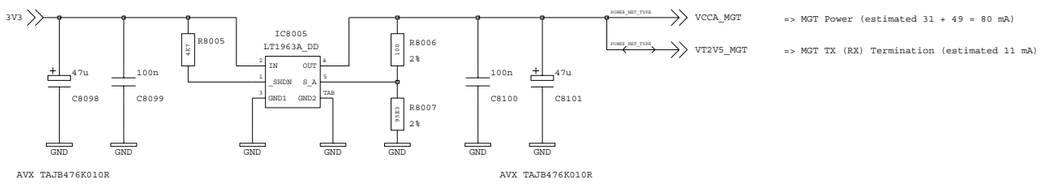
VCCINT Ramp rate 200 us min. and 50 ms max.

All GND nets on the FPGA need
to be connected to golbal GROUND.



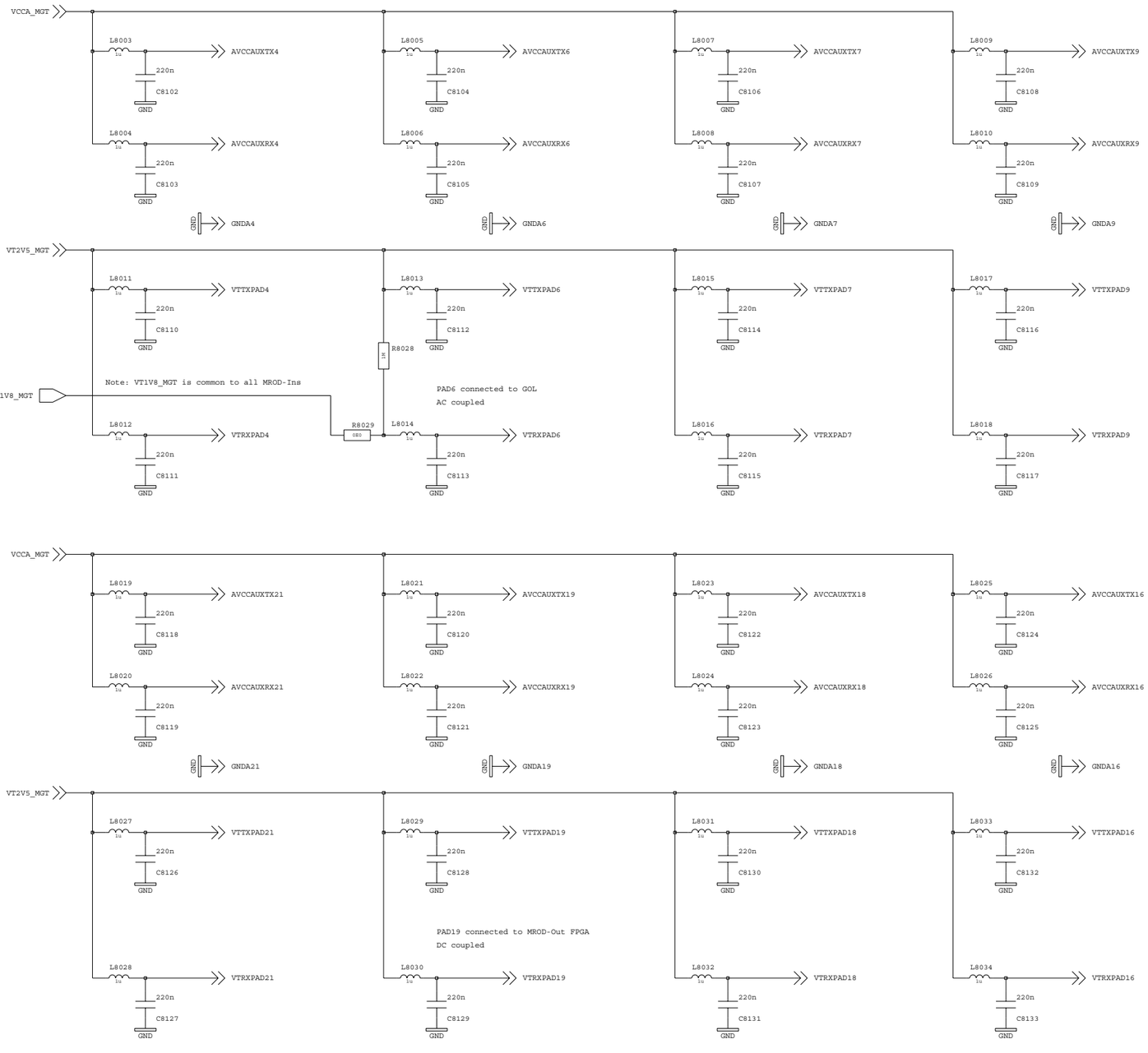
channel_in		Rev V2 2	
		Date 7 Feb 2006	
Input FPGA Power Supply Decoupling		Time 1:51:34 pm	
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
		Page 3 of 6	

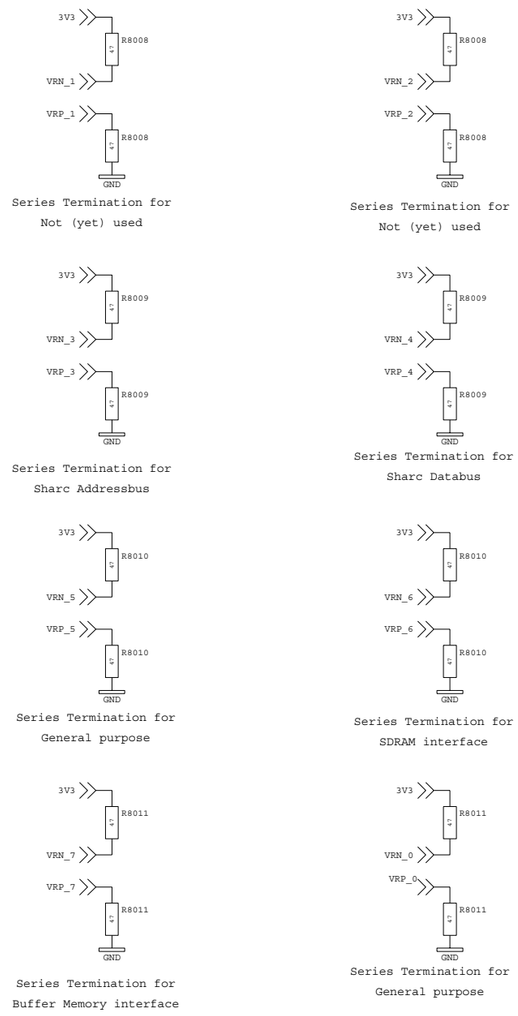
2V5 @ 1,5A



=> MGT Power (estimated 31 + 49 = 80 mA)

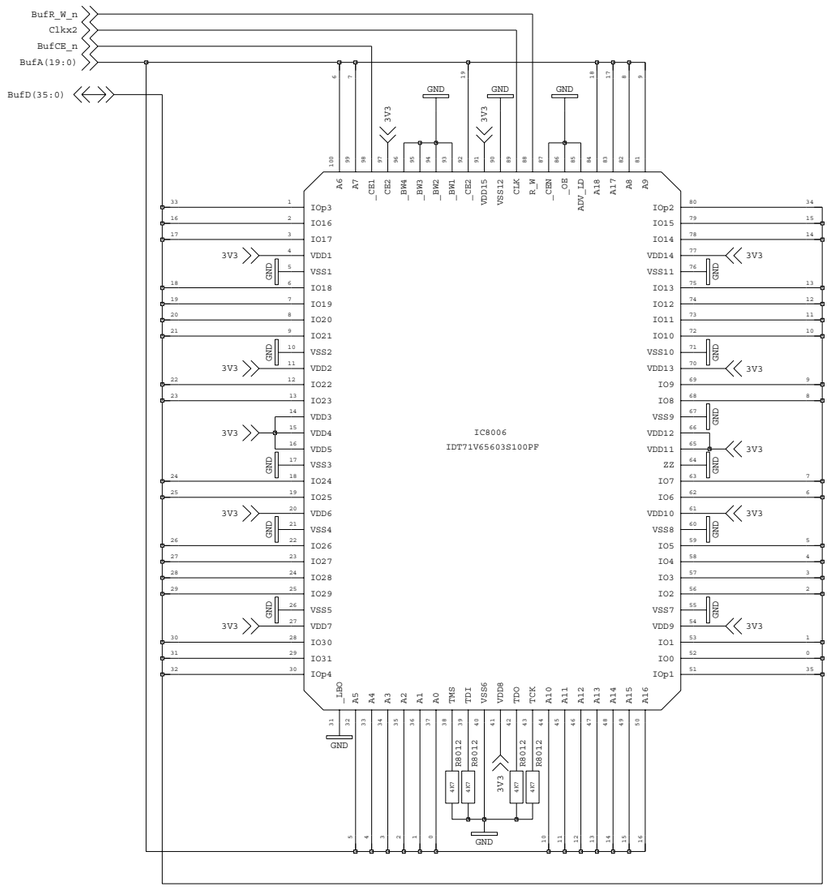
=> MGT TX (RX) Termination (estimated 11 mA)

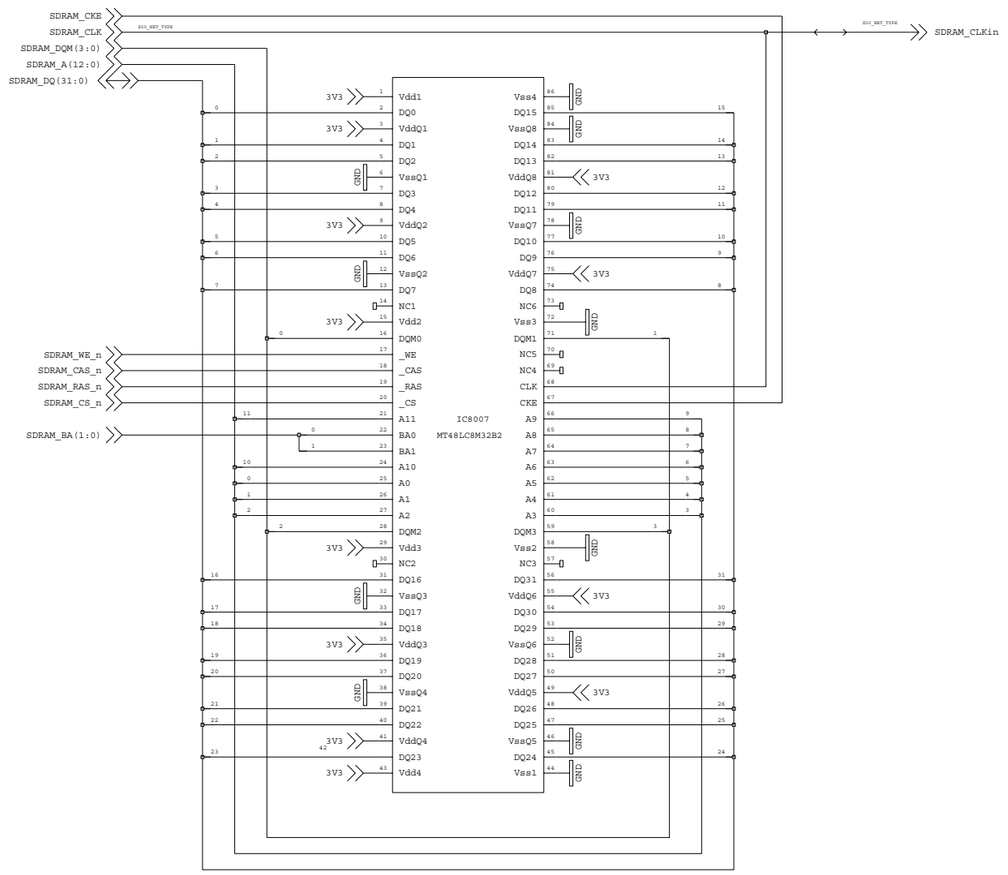


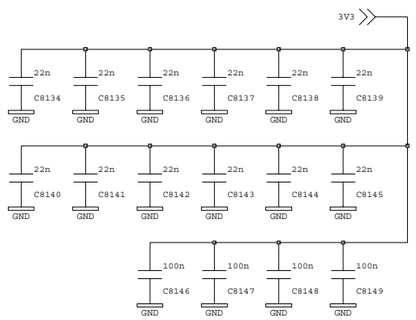


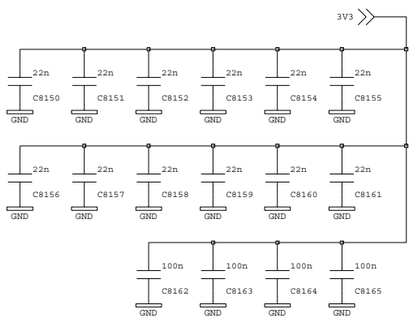
channel_in	Rev V2 2
	Date 7 Feb 2006
Input FPGA MGT Pwr Decoupling, Termination	Time 1:52:01 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	Size A3 / 4 1 4 A
NIKHEF	Dim 420 x 297 mm
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA, KRUISLAAN 409, 020-592 2000, 1098 SJ AMSTERDAM NEDERLAND	Page 4 of 6

SDRAM_A(12) is not connected

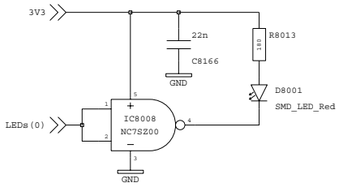


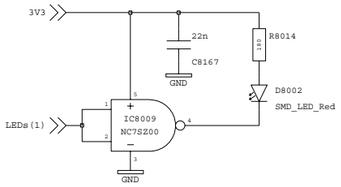


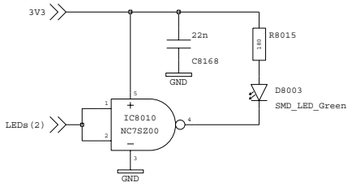


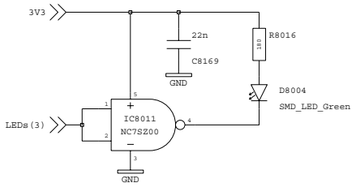


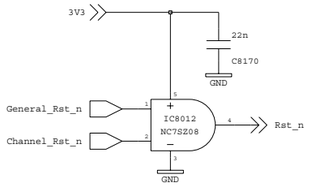
channel_in		Rev V2 2
		Date 7 Feb 2006
Buffer Memory (ZBT and SDRAM)		Time 1:52:29 pm
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 5 of 6



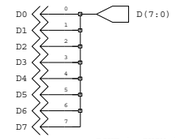


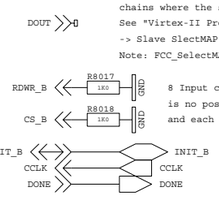






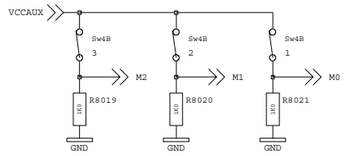
Fiducial8001 Fiducial8002





DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices.
See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SlectMAP programming Mode -> BUSY.
Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!

8 Input channels are loaded in parallel so there is no possibility for readback (RDWR_B = '0') and each CS_B = '0'



M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

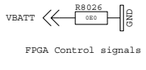
Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.

FPGA Configuration Signals

PWRDWN_B is unsupported (should be pulled high)

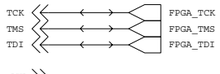
HSWAP_EN = '0' => User IOs have pull-up resistors during configuration

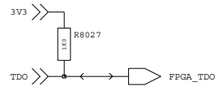
Temperature sensing diode



VBATT is decriptor key memory backup supply

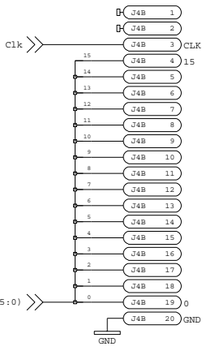
FPGA Control signals



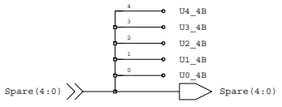


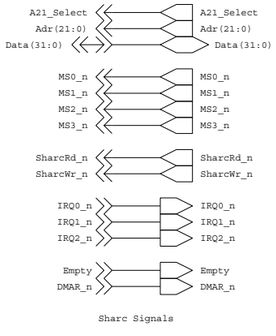
FPGA JTAG Signals

Optinal Test Connector



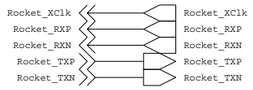
Testpoints force Spare lines to be accessible.





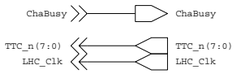
Sharc Signals

Input Channel ID bits



Frontend to Backend

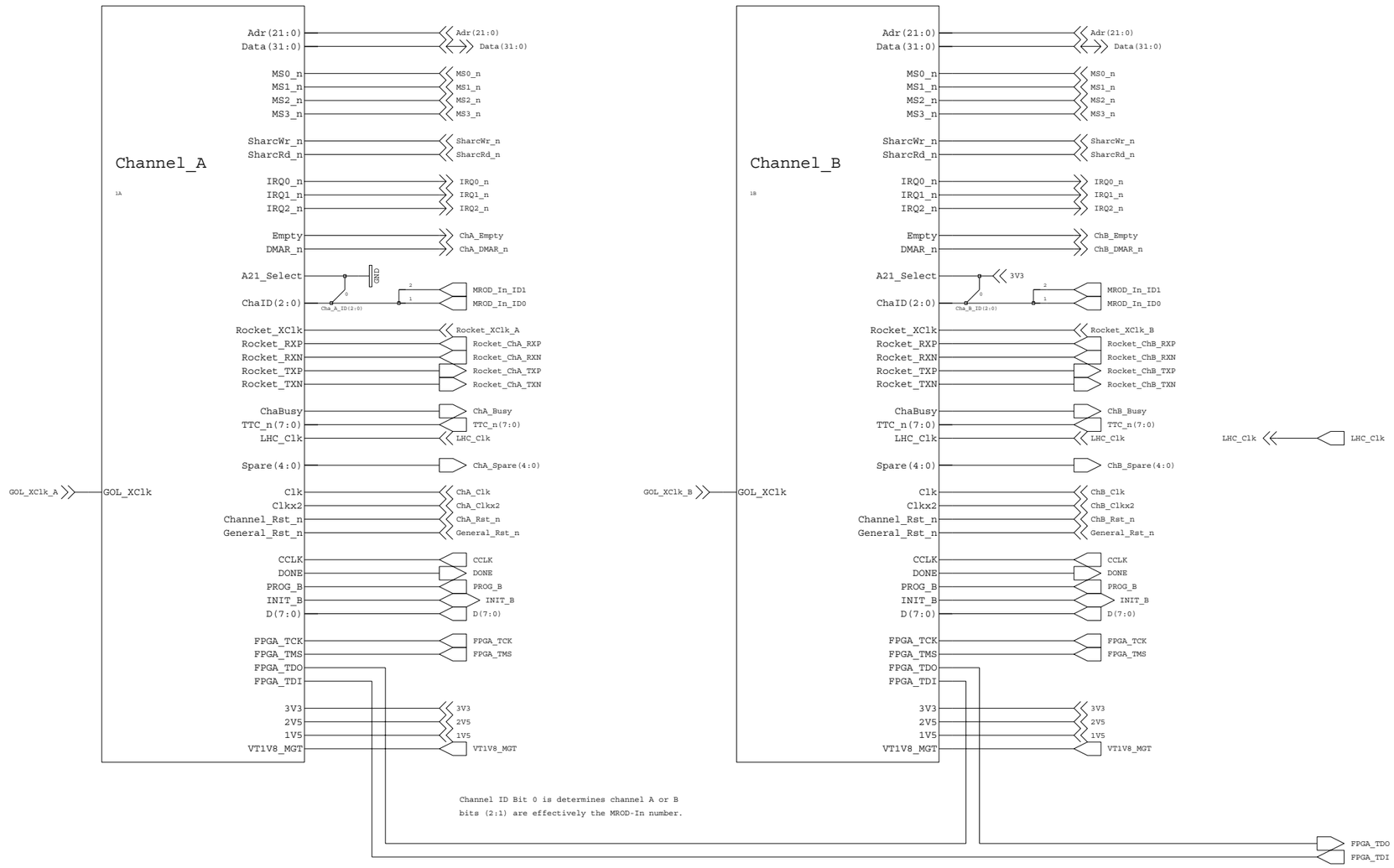
Rocket IO Signals



TTC Signals

Clock Signals

channel_in		Rev V2 2
		Date 7 Feb 2006
		Time 1:53:04 pm
Input FPGA Auxiliary Connections		Name Ton van Reen
Proj: MROD-X	Proj.No: 38405	
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 6 of 6



MROD-In		Rev V2 2	
Input Channels		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:45:51 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
		Page 1 of 4	

IC101
ADSP21160N

A1 DATA(14)	A2 DATA(13)	A3 DATA(10)	A4 DATA(8)	A5 DATA(4)	A6 DATA(2)	A7 TDI TDI	A8 TRST_n TRST_n	A9 RESET_n Rst_n	A10 RPBA GND	A11 IRQ0_n IRQ0_n	A12 FLAG1 ChB_Rst_n	A13 TIMEXP	A14 NC_A14	A15 NC_A15	A16 TFS1 TFS1	A17 RFS1 RFS1	A18 RCLK0	A19 DT0	A20 L0DAT(4) L0DATi(4)
B1 DATA(22)	B2 DATA(16)	B3 DATA(15)	B4 DATA(9)	B5 DATA(6)	B6 DATA(3)	B7 DATA(0) TCK	B8 TCK TCK	B9 EMU_n Sharc_EMU_n	B10 IRQ2_n IRQ2_n	B11 FLAG3 ChB_Empty	B12 FLAG0 ChA_Rst_n	B13 NC_B13	B14 NC_B14	B15 DT1	B16 RCLK1	B17 RFS0 RFS0	B18 TCLK0	B19 L0DAT(5) L0DATi(5)	B20 L0DAT(2) L0DATi(2)
C1 DATA(24)	C2 DATA(18)	C3 DATA(17)	C4 DATA(11)	C5 DATA(7)	C6 DATA(5)	C7 DATA(1) TMS	C8 TMS TMS	C9 TDO TDO	C10 IRQ1_n IRQ1_n	C11 FLAG2 ChA_Empty	C12 NC_C12	C13 NC_C13	C14 TCLK1	C15 DR1	C16 DR0	C17 L0DAT(7) L0DATi(7)	C18 L0DAT(6) L0DATi(6)	C19 L0ACK L0ACKi	C20 L0DAT(0) L0DATi(0)
D1 DATA(28)	D2 DATA(25)	D3 DATA(20)	D4 DATA(19)	D5 DATA(12)	D6 VDDEXT_D6 VDDEXT	D7 VDDINT_D7 VDDINT	D8 VDDEXT_D8 VDDEXT	D9 VDDEXT_D9 VDDEXT	D10 VDDEXT_D10 VDDEXT	D11 VDDEXT_D11 VDDEXT	D12 VDDEXT_D12 VDDEXT	D13 VDDINT_D13 VDDINT	D14 VDDEXT_D14 VDDEXT	D15 TFS0 TFS0	D16 L1DAT(7) L1DATi(7)	D17 L0CLK L0CLKi	D18 L0DAT(3) L0DATi(3)	D19 L0DAT(1) L0DATi(1)	D20 L1CLK L1CLKi
E1 DATA(30)	E2 DATA(29)	E3 DATA(23)	E4 DATA(21)	E5 VDDEXT_E5 VDDEXT	E6 VDDINT_E6 VDDINT	E7 VDDINT_E7 VDDINT	E8 VDDINT_E8 VDDINT	E9 VDDINT_E9 VDDINT	E10 VDDINT_E10 VDDINT	E11 GND_E11 GND	E12 VDDINT_E12 VDDINT	E13 VDDINT_E13 VDDINT	E14 VDDINT_E14 VDDINT	E15 VDDINT_E15 VDDINT	E16 VDDEXT_E16 VDDEXT	E17 L1DAT(6) L1DATi(6)	E18 L1DAT(5) L1DATi(5)	E19 L1ACK L1ACKi	E20 L1DAT(1) L1DATi(1)
F1 DATA(34) Data(2)	F2 DATA(33) Data(1)	F3 DATA(27)	F4 DATA(26)	F5 VDDEXT_F5 VDDEXT	F6 VDDINT_F6 VDDINT	F7 GND_F7 GND	F8 GND_F8 GND	F9 GND_F9 GND	F10 GND_F10 GND	F11 GND_F11 GND	F12 GND_F12 GND	F13 GND_F13 GND	F14 GND_F14 GND	F15 VDDINT_F15 VDDINT	F16 VDDEXT_F16 VDDEXT	F17 L1DAT(4) L1DATi(4)	F18 L1DAT(3) L1DATi(3)	F19 L1DAT(0) L1DATi(0)	F20 L2DAT(7) L2DATi(7)
G1 DATA(38) Data(6)	G2 DATA(35) Data(3)	G3 DATA(32) Data(0)	G4 DATA(31)	G5 VDDEXT_G5 VDDEXT	G6 VDDINT_G6 VDDINT	G7 GND_G7 GND	G8 GND_G8 GND	G9 GND_G9 GND	G10 GND_G10 GND	G11 GND_G11 GND	G12 GND_G12 GND	G13 GND_G13 GND	G14 GND_G14 GND	G15 VDDINT_G15 VDDINT	G16 VDDEXT_G16 VDDEXT	G17 L1DAT(2) L1DATi(2)	G18 L2DAT(6) L2DATi(6)	G19 L2DAT(4) L2DATi(4)	G20 L2CLK L2CLKi
H1 DATA(40) Data(8)	H2 DATA(39) Data(7)	H3 DATA(37) Data(5)	H4 DATA(36) Data(4)	H5 VDDEXT_H5 VDDEXT	H6 VDDINT_H6 VDDINT	H7 GND_H7 GND	H8 GND_H8 GND	H9 GND_H9 GND	H10 GND_H10 GND	H11 GND_H11 GND	H12 GND_H12 GND	H13 GND_H13 GND	H14 GND_H14 GND	H15 VDDINT_H15 VDDINT	H16 VDDEXT_H16 VDDEXT	H17 L2DAT(5) L2DATi(5)	H18 L2ACK L2ACKi	H19 L2DAT(3) L2DATi(3)	H20 L2DAT(1) L2DATi(1)
J1 DATA(44) Data(12)	J2 DATA(43) Data(11)	J3 DATA(42) Data(10)	J4 DATA(41) Data(9)	J5 VDDEXT_J5 VDDEXT	J6 VDDINT_J6 VDDINT	J7 GND_J7 GND	J8 GND_J8 GND	J9 GND_J9 GND	J10 GND_J10 GND	J11 GND_J11 GND	J12 GND_J12 GND	J13 GND_J13 GND	J14 GND_J14 GND	J15 VDDINT_J15 VDDINT	J16 VDDEXT_J16 VDDEXT	J17 L2DAT(2) L2DATi(2)	J18 L2DAT(0) L2DATi(0)	J19 HBG_n HBG_n	J20 HBR_n VDDEXT
K1 CLK_CFG_0 GND	K2 DATA(46) Data(14)	K3 DATA(45) Data(13)	K4 DATA(47) Data(15)	K5 VDDEXT_K5 VDDEXT	K6 VDDINT_K6 VDDINT	K7 GND_K7 GND	K8 GND_K8 GND	K9 GND_K9 GND	K10 GND_K10 GND	K11 GND_K11 GND	K12 GND_K12 GND	K13 GND_K13 GND	K14 GND_K14 GND	K15 VDDINT_K15 VDDINT	K16 VDDEXT_K16 VDDEXT	K17 BR6_n BReq_n	K18 BR5_n BReq_n	K19 BR4_n BReq_n	K20 BR3_n BReq_n
L1 CLKIN Sharc_Clk	L2 CLK_CFG_1 VDDEXT	L3 AGND GND	L4 CLK_CFG_2 GND	L5 VDDEXT_L5 VDDEXT	L6 VDDINT_L6 VDDINT	L7 GND_L7 GND	L8 GND_L8 GND	L9 GND_L9 GND	L10 GND_L10 GND	L11 GND_L11 GND	L12 GND_L12 GND	L13 GND_L13 GND	L14 GND_L14 GND	L15 VDDINT_L15 VDDINT	L16 VDDEXT_L16 VDDEXT	L17 BR2_n BReq_n	L18 BR1_n BReq_n	L19 ACK	L20 REDY
M1 AVDD AVDD	M2 CLK_CFG_3 GND	M3 CLKOUT	M4 NC_M4	M5 VDDEXT_M5 VDDEXT	M6 VDDINT_M6 VDDINT	M7 GND_M7 GND	M8 GND_M8 GND	M9 GND_M9 GND	M10 GND_M10 GND	M11 GND_M11 GND	M12 GND_M12 GND	M13 GND_M13 GND	M14 GND_M14 GND	M15 VDDINT_M15 VDDINT	M16 VDDEXT_M16 VDDEXT	M17 PAGE	M18 SBTS_n VDDEXT	M19 PA_n	M20 L3DAT(7) L3DATi(7)
N1 NC_N1	N2 NC_N2	N3 DATA(48) Data(16)	N4 DATA(51) Data(19)	N5 VDDEXT_N5 VDDEXT	N6 VDDINT_N6 VDDINT	N7 GND_N7 GND	N8 GND_N8 GND	N9 GND_N9 GND	N10 GND_N10 GND	N11 GND_N11 GND	N12 GND_N12 GND	N13 GND_N13 GND	N14 GND_N14 GND	N15 VDDINT_N15 VDDINT	N16 VDDEXT_N16 VDDEXT	N17 L3DAT(5) L3DATi(5)	N18 L3DAT(6) L3DATi(6)	N19 L3DAT(4) L3DATi(4)	N20 L3CLK L3CLKi
P1 DATA(49) Data(17)	P2 DATA(50) Data(18)	P3 DATA(52) Data(20)	P4 DATA(55) Data(23)	P5 VDDEXT_P5 VDDEXT	P6 VDDINT_P6 VDDINT	P7 GND_P7 GND	P8 GND_P8 GND	P9 GND_P9 GND	P10 GND_P10 GND	P11 GND_P11 GND	P12 GND_P12 GND	P13 GND_P13 GND	P14 GND_P14 GND	P15 VDDINT_P15 VDDINT	P16 VDDEXT_P16 VDDEXT	P17 L3DAT(2) L3DATi(2)	P18 L3DAT(1) L3DATi(1)	P19 L3DAT(3) L3DATi(3)	P20 L3ACK L3ACKi
R1 DATA(53) Data(21)	R2 DATA(54) Data(22)	R3 DATA(57) Data(25)	R4 DATA(60) Data(28)	R5 VDDEXT_R5 VDDEXT	R6 VDDINT_R6 VDDINT	R7 GND_R7 GND	R8 GND_R8 GND	R9 GND_R9 GND	R10 GND_R10 GND	R11 GND_R11 GND	R12 GND_R12 GND	R13 GND_R13 GND	R14 GND_R14 GND	R15 GND_R15 GND	R16 VDDEXT_R16 VDDEXT	R17 L4DAT(5) L4DATi(5)	R18 L4DAT(6) L4DATi(6)	R19 L4DAT(7) L4DATi(7)	R20 L3DAT(0) L3DATi(0)
T1 DATA(56) Data(24)	T2 DATA(58) Data(26)	T3 DATA(59) Data(27)	T4 DATA(63) Data(31)	T5 VDDEXT_T5 VDDEXT	T6 VDDINT_T6 VDDINT	T7 VDDINT_T7 VDDINT	T8 VDDINT_T8 VDDINT	T9 VDDINT_T9 VDDINT	T10 VDDINT_T10 VDDINT	T11 VDDINT_T11 VDDINT	T12 VDDINT_T12 VDDINT	T13 VDDINT_T13 VDDINT	T14 VDDINT_T14 VDDINT	T15 VDDINT_T15 VDDINT	T16 VDDEXT_T16 VDDEXT	T17 L4DAT(3) L4DATi(3)	T18 L4ACK L4ACKi	T19 L4CLK L4CLKi	T20 L4DAT(4) L4DATi(4)
U1 DATA(61) Data(29)	U2 DATA(62) Data(30)	U3 ADDR(3) Adr(3)	U4 ADDR(2) Adr(2)	U5 VDDEXT_U5 VDDEXT	U6 VDDEXT_U6 VDDEXT	U7 VDDEXT_U7 VDDEXT	U8 VDDEXT_U8 VDDEXT	U9 VDDEXT_U9 VDDEXT	U10 VDDEXT_U10 VDDEXT	U11 VDDEXT_U11 VDDEXT	U12 VDDEXT_U12 VDDEXT	U13 VDDEXT_U13 VDDEXT	U14 VDDEXT_U14 VDDEXT	U15 VDDEXT_U15 VDDEXT	U16 VDDEXT_U16 VDDEXT	U17 L5DAT(7) L5DATi(7)	U18 L4DAT(0) L4DATi(0)	U19 L4DAT(1) L4DATi(1)	U20 L4DAT(2) L4DATi(2)
V1 ADDR(4) Adr(4)	V2 ADDR(6) Adr(6)	V3 ADDR(7) Adr(7)	V4 ADDR(10) Adr(10)	V5 ADDR(14) Adr(14)	V6 ADDR(18) Adr(18)	V7 ADDR(22)	V8 ADDR(25)	V9 ADDR(28)	V10 ID0 GND	V11 ADDR(1) Adr(1)	V12 MS1_n MS1_n	V13 CS_n VDDEXT	V14 RDL_n	V15 DMAR2_n ChB_DMAR_n	V16 L5DAT(0) L5DATi(0)	V17 L5DAT(2) L5DATi(2)	V18 L5ACK L5ACKi	V19 L5DAT(4) L5DATi(4)	V20 L5DAT(6) L5DATi(6)
W1 ADDR(5) Adr(5)	W2 ADDR(9) Adr(9)	W3 ADDR(12) Adr(12)	W4 ADDR(15) Adr(15)	W5 ADDR(17) Adr(17)	W6 ADDR(20) Adr(20)	W7 ADDR(23)	W8 ADDR(26)	W9 ADDR(29)	W10 ID1 GND	W11 ADDR(0) Adr(0)	W12 BMS_n BMS_n	W13 MS2_n MS2_n	W14 CIP_n	W15 RDH_n SharcRd_n	W16 DMAG2_n	W17 LBOOT VDDEXT	W18 L5DAT(1) L5DATi(1)	W19 L5DAT(3) L5DATi(3)	W20 L5DAT(5) L5DATi(5)
Y1 ADDR(8) Adr(8)	Y2 ADDR(11) Adr(11)	Y3 ADDR(13) Adr(13)	Y4 ADDR(16) Adr(16)	Y5 ADDR(19) Adr(19)	Y6 ADDR(21) Adr(21)	Y7 ADDR(24)	Y8 ADDR(27)	Y9 ADDR(30)	Y10 ADDR(31)	Y11 ID2 GND	Y12 BRST BRST	Y13 MS0_n MS0_n	Y14 MS3_n MS3_n	Y15 WRH_n SharcWr_n	Y16 WRL_n	Y17 DMAG1_n DMAG1_n	Y18 DMAR1_n ChA_DMAR_n	Y19 EBOOT GND	Y20 L5CLK L5CLKi

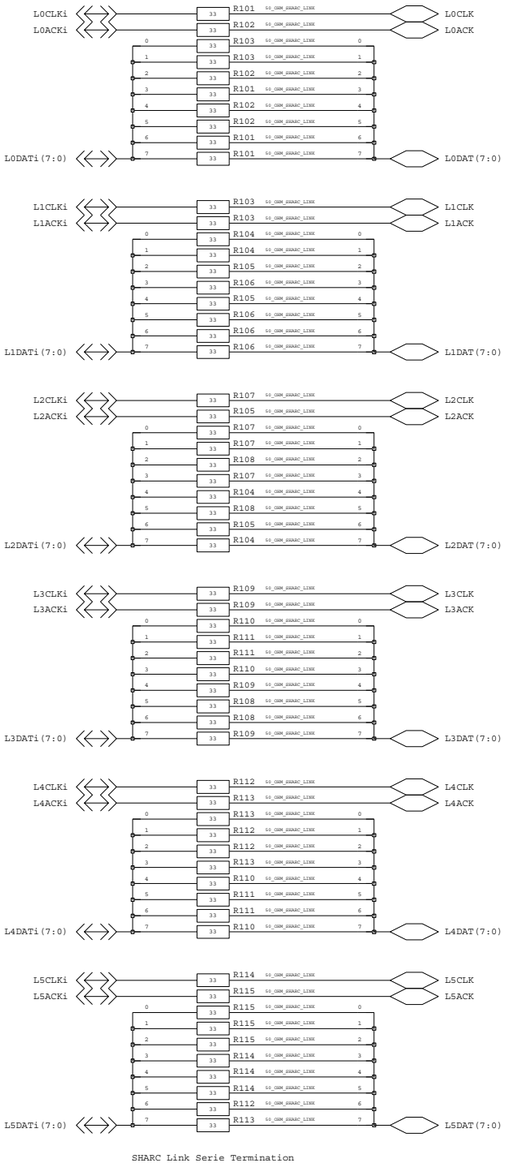
Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

ID = "000"

Booting Mode:
EBOOT = '0', LBOOT = '1', BMS_n = '1' (Input)
=> Link Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

MROD-In		Rev V2 2
		Date 7 Feb 2006
SHARC		Time 1:46:33 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF © ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A Dim 420 x 297 mm Page 2 of 4



Communication Link

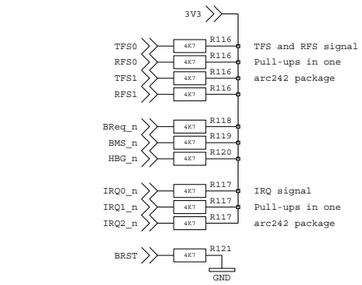
Communication Link

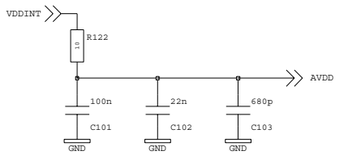
Communication Link

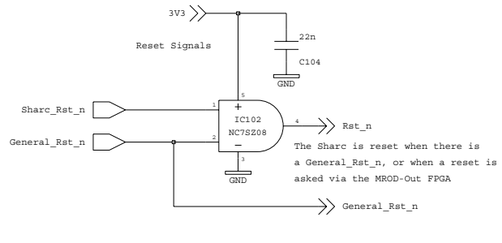
Data Link to MROD-Out Sharc-B

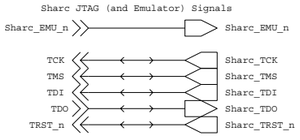
Data Link to MROD-Out Sharc-A
Also Boot Link

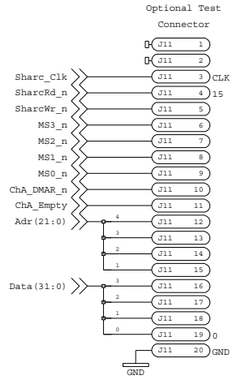
Communication Link

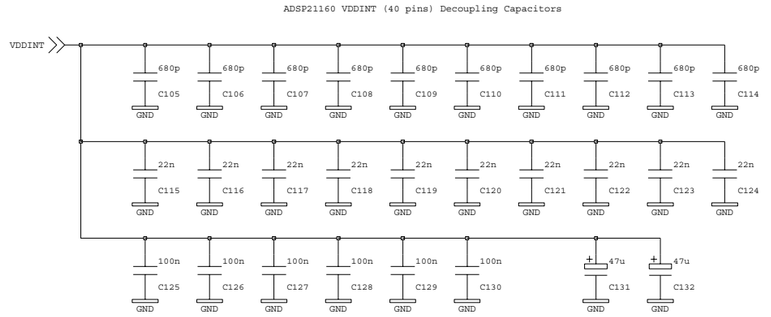


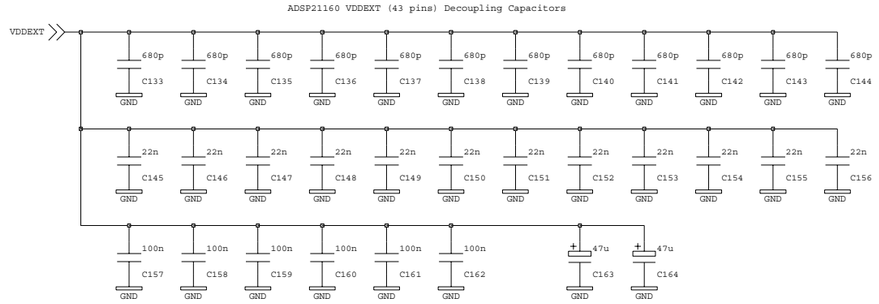






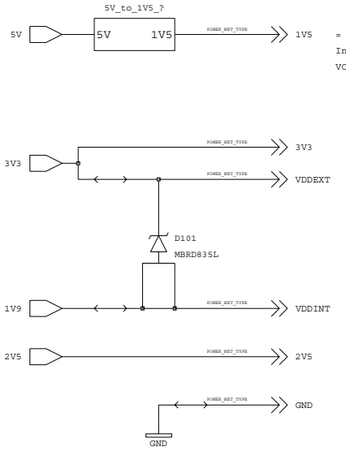


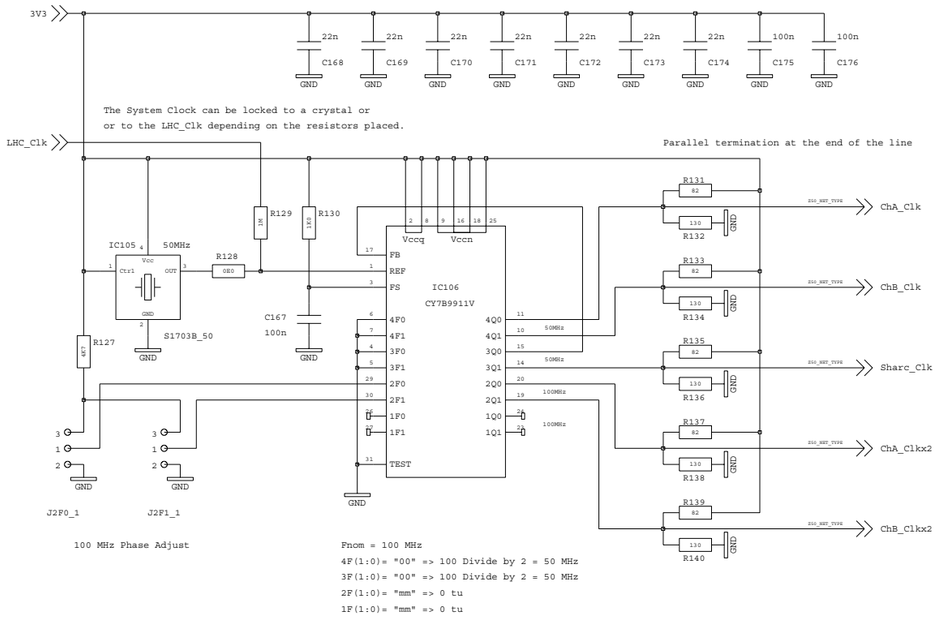


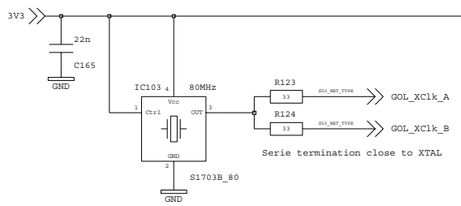


Fiducial101 Fiducial102

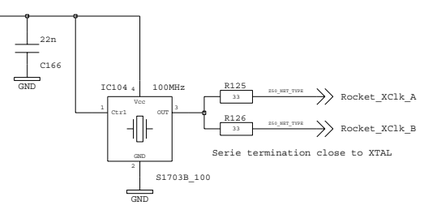
MROD-In		Rev V2 2
		Date 7 Feb 2006
SHARC Auxiliary and Decoupling		Time 1:46:57 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 3 of 4





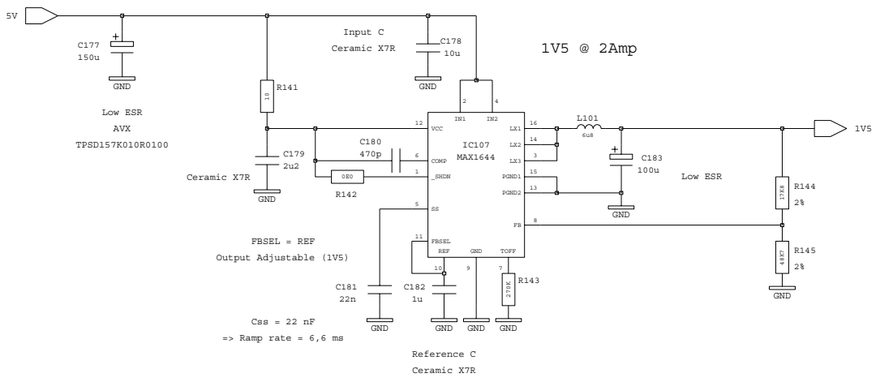


GOL Frequency
80 MHz 16 bit = 40 MHz 32 bit
= 160 MB/s

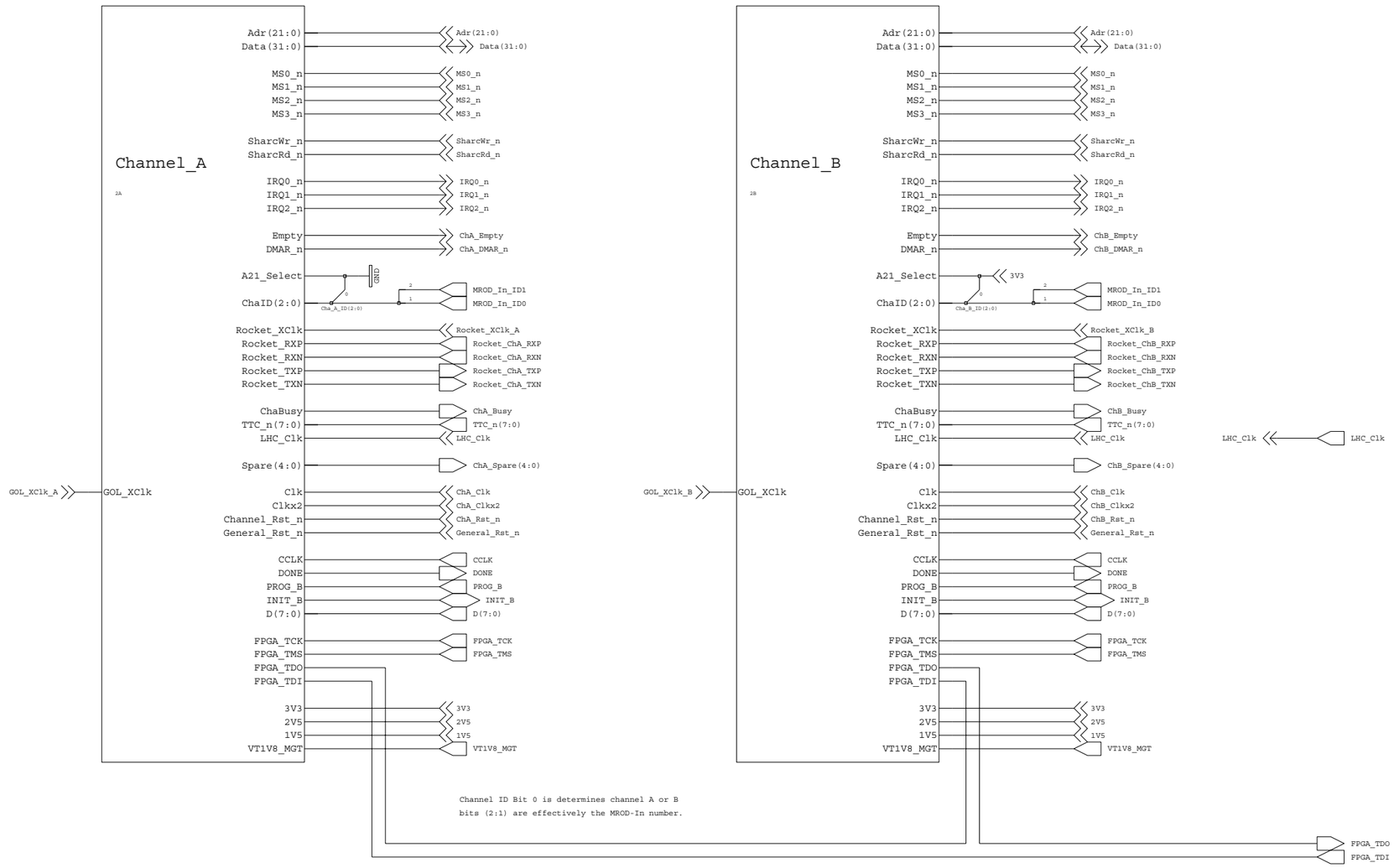


Rocket-IO Inter-FPGA Link Frequency
100 MHz 16 bit = 50 MHz 32 bit
= 200 MB/s

MROD-In	Rev V2 20
	Date 7 Feb 2006
Power and Clocks	Time 1:47:20 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	
NIKHEF	Size A3 / 4 1 4 A
© NT-Nikhef Amsterdam	Dim 420 x 297 mm
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Page 4 of 4



Power Supply			Rev V2 2
5V -> 1V5 @ 2A			Date 7 Feb 2006
Proj: MROD-X	Proj.No: 38405		Time 1:38:24 pm
Peter Jansweijer	peterj@nikhef.nl		Name tonvr
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size A3 4 1 4 A
			Dim 420 x 297 mm
			Page 1 of 1



MROD-In		Rev V2 2	
Input Channels		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:45:51 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
		Page 1 of 4	

IC201
ADSP21160N

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A																		
B																		
C																		
D																		
E																		
F																		
G																		
H																		
I																		
J																		
K																		
L																		

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	A1 DATA(14)	A2 DATA(13)	A3 DATA(10)	A4 DATA(8)	A5 DATA(4)	A6 DATA(2)	A7 TDI TDI	A8 TRST_n TRST_n	A9 RESET_n Rst_n	A10 RPBA GND	A11 IRQ0_n IRQ0_n	A12 FLAG1 ChB_Rst_n	A13 TIMEXP	A14 NC_A14	A15 NC_A15	A16 TFS1 TFS1	A17 RFS1 RFS1	A18 RCLK0	A19 DT0	A20 L0DAT(4) L0DATi(4)
B	B1 DATA(22)	B2 DATA(16)	B3 DATA(15)	B4 DATA(9)	B5 DATA(6)	B6 DATA(3)	B7 DATA(0)	B8 TCK TCK	B9 EMU_n Sharc_EMU_n	B10 IRQ2_n IRQ2_n	B11 FLAG3 ChB_Empty	B12 FLAG0 ChA_Rst_n	B13 NC_B13	B14 NC_B14	B15 DT1	B16 RCLK1	B17 RFS0 RFS0	B18 TCLK0	B19 L0DAT(5) L0DATi(5)	B20 L0DAT(2) L0DATi(2)
C	C1 DATA(24)	C2 DATA(18)	C3 DATA(17)	C4 DATA(11)	C5 DATA(7)	C6 DATA(5)	C7 DATA(1)	C8 TMS TMS	C9 TDO TDO	C10 IRQ1_n IRQ1_n	C11 FLAG2 ChA_Empty	C12 NC_C12	C13 NC_C13	C14 TCLK1	C15 DR1	C16 DR0	C17 L0DAT(7) L0DATi(7)	C18 L0DAT(6) L0DATi(6)	C19 L0ACK L0ACKi	C20 L0DAT(0) L0DATi(0)
D	D1 DATA(28)	D2 DATA(25)	D3 DATA(20)	D4 DATA(19)	D5 DATA(12)	D6 VDDEXT_D6 VDDEXT	D7 VDDINT_D7 VDDINT	D8 VDDEXT_D8 VDDEXT	D9 VDDEXT_D9 VDDEXT	D10 VDDEXT_D10 VDDEXT	D11 VDDEXT_D11 VDDEXT	D12 VDDEXT_D12 VDDEXT	D13 VDDINT_D13 VDDINT	D14 VDDEXT_D14 VDDEXT	D15 TFS0 TFS0	D16 L1DAT(7) L1DATi(7)	D17 L0CLK L0CLKi	D18 L0DAT(3) L0DATi(3)	D19 L0DAT(1) L0DATi(1)	D20 L1CLK L1CLKi
E	E1 DATA(30)	E2 DATA(29)	E3 DATA(23)	E4 DATA(21)	E5 VDDEXT_E5 VDDEXT	E6 VDDINT_E6 VDDINT	E7 VDDINT_E7 VDDINT	E8 VDDINT_E8 VDDINT	E9 VDDINT_E9 VDDINT	E10 VDDINT_E10 VDDINT	E11 GND_E11 GND	E12 VDDINT_E12 VDDINT	E13 VDDINT_E13 VDDINT	E14 VDDINT_E14 VDDINT	E15 VDDINT_E15 VDDINT	E16 VDDEXT_E16 VDDEXT	E17 L1DAT(6) L1DATi(6)	E18 L1DAT(5) L1DATi(5)	E19 L1ACK L1ACKi	E20 L1DAT(1) L1DATi(1)
F	F1 DATA(34) Data(2)	F2 DATA(33) Data(1)	F3 DATA(27)	F4 DATA(26)	F5 VDDEXT_F5 VDDEXT	F6 VDDINT_F6 VDDINT	F7 GND_F7 GND	F8 GND_F8 GND	F9 GND_F9 GND	F10 GND_F10 GND	F11 GND_F11 GND	F12 GND_F12 GND	F13 GND_F13 GND	F14 GND_F14 GND	F15 VDDINT_F15 VDDINT	F16 VDDEXT_F16 VDDEXT	F17 L1DAT(4) L1DATi(4)	F18 L1DAT(3) L1DATi(3)	F19 L1DAT(0) L1DATi(0)	F20 L2DAT(7) L2DATi(7)
G	G1 DATA(38) Data(6)	G2 DATA(35) Data(3)	G3 DATA(32) Data(0)	G4 DATA(31)	G5 VDDEXT_G5 VDDEXT	G6 VDDINT_G6 VDDINT	G7 GND_G7 GND	G8 GND_G8 GND	G9 GND_G9 GND	G10 GND_G10 GND	G11 GND_G11 GND	G12 GND_G12 GND	G13 GND_G13 GND	G14 GND_G14 GND	G15 VDDINT_G15 VDDINT	G16 VDDEXT_G16 VDDEXT	G17 L1DAT(2) L1DATi(2)	G18 L2DAT(6) L2DATi(6)	G19 L2DAT(4) L2DATi(4)	G20 L2CLK L2CLKi
H	H1 DATA(40) Data(8)	H2 DATA(39) Data(7)	H3 DATA(37) Data(5)	H4 DATA(36) Data(4)	H5 VDDEXT_H5 VDDEXT	H6 VDDINT_H6 VDDINT	H7 GND_H7 GND	H8 GND_H8 GND	H9 GND_H9 GND	H10 GND_H10 GND	H11 GND_H11 GND	H12 GND_H12 GND	H13 GND_H13 GND	H14 GND_H14 GND	H15 VDDINT_H15 VDDINT	H16 VDDEXT_H16 VDDEXT	H17 L2DAT(5) L2DATi(5)	H18 L2ACK L2ACKi	H19 L2DAT(3) L2DATi(3)	H20 L2DAT(1) L2DATi(1)
J	J1 DATA(44) Data(12)	J2 DATA(43) Data(11)	J3 DATA(42) Data(10)	J4 DATA(41) Data(9)	J5 VDDEXT_J5 VDDEXT	J6 VDDINT_J6 VDDINT	J7 GND_J7 GND	J8 GND_J8 GND	J9 GND_J9 GND	J10 GND_J10 GND	J11 GND_J11 GND	J12 GND_J12 GND	J13 GND_J13 GND	J14 GND_J14 GND	J15 VDDINT_J15 VDDINT	J16 VDDEXT_J16 VDDEXT	J17 L2DAT(2) L2DATi(2)	J18 L2DAT(0) L2DATi(0)	J19 HBG_n HBG_n	J20 HBR_n VDDEXT
K	K1 CLK_CFG_0 GND	K2 DATA(46) Data(14)	K3 DATA(45) Data(13)	K4 DATA(47) Data(15)	K5 VDDEXT_K5 VDDEXT	K6 VDDINT_K6 VDDINT	K7 GND_K7 GND	K8 GND_K8 GND	K9 GND_K9 GND	K10 GND_K10 GND	K11 GND_K11 GND	K12 GND_K12 GND	K13 GND_K13 GND	K14 GND_K14 GND	K15 VDDINT_K15 VDDINT	K16 VDDEXT_K16 VDDEXT	K17 BR6_n BReq_n	K18 BR5_n BReq_n	K19 BR4_n BReq_n	K20 BR3_n BReq_n
L	L1 CLKIN Sharc_Clk	L2 CLK_CFG_1 VDDEXT	L3 AGND GND	L4 CLK_CFG_2 GND	L5 VDDEXT_L5 VDDEXT	L6 VDDINT_L6 VDDINT	L7 GND_L7 GND	L8 GND_L8 GND	L9 GND_L9 GND	L10 GND_L10 GND	L11 GND_L11 GND	L12 GND_L12 GND	L13 GND_L13 GND	L14 GND_L14 GND	L15 VDDINT_L15 VDDINT	L16 VDDEXT_L16 VDDEXT	L17 BR2_n BReq_n	L18 BR1_n BReq_n	L19 ACK	L20 REDY
M	M1 AVDD AVDD	M2 CLK_CFG_3 GND	M3 CLKOUT	M4 NC_M4	M5 VDDEXT_M5 VDDEXT	M6 VDDINT_M6 VDDINT	M7 GND_M7 GND	M8 GND_M8 GND	M9 GND_M9 GND	M10 GND_M10 GND	M11 GND_M11 GND	M12 GND_M12 GND	M13 GND_M13 GND	M14 GND_M14 GND	M15 VDDINT_M15 VDDINT	M16 VDDEXT_M16 VDDEXT	M17 PAGE	M18 SBTS_n VDDEXT	M19 PA_n	M20 L3DAT(7) L3DATi(7)
N	N1 NC_N1	N2 NC_N2	N3 DATA(48) Data(16)	N4 DATA(51) Data(19)	N5 VDDEXT_N5 VDDEXT	N6 VDDINT_N6 VDDINT	N7 GND_N7 GND	N8 GND_N8 GND	N9 GND_N9 GND	N10 GND_N10 GND	N11 GND_N11 GND	N12 GND_N12 GND	N13 GND_N13 GND	N14 GND_N14 GND	N15 VDDINT_N15 VDDINT	N16 VDDEXT_N16 VDDEXT	N17 L3DAT(5) L3DATi(5)	N18 L3DAT(6) L3DATi(6)	N19 L3DAT(4) L3DATi(4)	N20 L3CLK L3CLKi
P	P1 DATA(49) Data(17)	P2 DATA(50) Data(18)	P3 DATA(52) Data(20)	P4 DATA(55) Data(23)	P5 VDDEXT_P5 VDDEXT	P6 VDDINT_P6 VDDINT	P7 GND_P7 GND	P8 GND_P8 GND	P9 GND_P9 GND	P10 GND_P10 GND	P11 GND_P11 GND	P12 GND_P12 GND	P13 GND_P13 GND	P14 GND_P14 GND	P15 VDDINT_P15 VDDINT	P16 VDDEXT_P16 VDDEXT	P17 L3DAT(2) L3DATi(2)	P18 L3DAT(1) L3DATi(1)	P19 L3DAT(3) L3DATi(3)	P20 L3ACK L3ACKi
R	R1 DATA(53) Data(21)	R2 DATA(54) Data(22)	R3 DATA(57) Data(25)	R4 DATA(60) Data(28)	R5 VDDEXT_R5 VDDEXT	R6 VDDINT_R6 VDDINT	R7 GND_R7 GND	R8 GND_R8 GND	R9 GND_R9 GND	R10 GND_R10 GND	R11 GND_R11 GND	R12 GND_R12 GND	R13 GND_R13 GND	R14 GND_R14 GND	R15 GND_R15 GND	R16 VDDEXT_R16 VDDEXT	R17 L4DAT(5) L4DATi(5)	R18 L4DAT(6) L4DATi(6)	R19 L4DAT(7) L4DATi(7)	R20 L3DAT(0) L3DATi(0)
T	T1 DATA(56) Data(24)	T2 DATA(58) Data(26)	T3 DATA(59) Data(27)	T4 DATA(63) Data(31)	T5 VDDEXT_T5 VDDEXT	T6 VDDINT_T6 VDDINT	T7 VDDINT_T7 VDDINT	T8 VDDINT_T8 VDDINT	T9 VDDINT_T9 VDDINT	T10 VDDINT_T10 VDDINT	T11 VDDINT_T11 VDDINT	T12 VDDINT_T12 VDDINT	T13 VDDINT_T13 VDDINT	T14 VDDINT_T14 VDDINT	T15 VDDINT_T15 VDDINT	T16 VDDEXT_T16 VDDEXT	T17 L4DAT(3) L4DATi(3)	T18 L4ACK L4ACKi	T19 L4CLK L4CLKi	T20 L4DAT(4) L4DATi(4)
U	U1 DATA(61) Data(29)	U2 DATA(62) Data(30)	U3 ADDR(3) Adr(3)	U4 ADDR(2) Adr(2)	U5 VDDEXT_U5 VDDEXT	U6 VDDEXT_U6 VDDEXT	U7 VDDEXT_U7 VDDEXT	U8 VDDEXT_U8 VDDEXT	U9 VDDEXT_U9 VDDEXT	U10 VDDEXT_U10 VDDEXT	U11 VDDEXT_U11 VDDEXT	U12 VDDEXT_U12 VDDEXT	U13 VDDEXT_U13 VDDEXT	U14 VDDEXT_U14 VDDEXT	U15 VDDEXT_U15 VDDEXT	U16 VDDEXT_U16 VDDEXT	U17 L5DAT(7) L5DATi(7)	U18 L4DAT(0) L4DATi(0)	U19 L4DAT(1) L4DATi(1)	U20 L4DAT(2) L4DATi(2)
V	V1 ADDR(4) Adr(4)	V2 ADDR(6) Adr(6)	V3 ADDR(7) Adr(7)	V4 ADDR(10) Adr(10)	V5 ADDR(14) Adr(14)	V6 ADDR(18) Adr(18)	V7 ADDR(22)	V8 ADDR(25)	V9 ADDR(28)	V10 ID0 GND	V11 ADDR(1) Adr(1)	V12 MS1_n MS1_n	V13 CS_n VDDEXT	V14 RDL_n	V15 DMAR2_n ChB_DMAR_n	V16 L5DAT(0) L5DATi(0)	V17 L5DAT(2) L5DATi(2)	V18 L5ACK L5ACKi	V19 L5DAT(4) L5DATi(4)	V20 L5DAT(6) L5DATi(6)
W	W1 ADDR(5) Adr(5)	W2 ADDR(9) Adr(9)	W3 ADDR(12) Adr(12)	W4 ADDR(15) Adr(15)	W5 ADDR(17) Adr(17)	W6 ADDR(20) Adr(20)	W7 ADDR(23)	W8 ADDR(26)	W9 ADDR(29)	W10 ID1 GND	W11 ADDR(0) Adr(0)	W12 BMS_n BMS_n	W13 MS2_n MS2_n	W14 CIF_n	W15 RDH_n SharcRd_n	W16 DMAG2_n	W17 LBOOT VDDEXT	W18 L5DAT(1) L5DATi(1)	W19 L5DAT(3) L5DATi(3)	W20 L5DAT(5) L5DATi(5)
Y	Y1 ADDR(8) Adr(8)	Y2 ADDR(11) Adr(11)	Y3 ADDR(13) Adr(13)	Y4 ADDR(16) Adr(16)	Y5 ADDR(19) Adr(19)	Y6 ADDR(21) Adr(21)	Y7 ADDR(24)	Y8 ADDR(27)	Y9 ADDR(30)	Y10 ADDR(31)	Y11 ID2 GND	Y12 BRST BRST	Y13 MS0_n MS0_n	Y14 MS3_n MS3_n	Y15 WRH_n SharcWr_n	Y16 WRL_n	Y17 DMAG1_n ChA_DMAR_n	Y18 DMAR1_n GND	Y19 EBOOT	Y20 L5CLK L5CLKi

Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

ID = "000"

Booting Mode:
EBOOT = '0', LBOOT = '1', BMS_n = '1' (Input)
=> Link Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

MROD-In

SHARC	
Proj: MROD-X	Proj.No: 38405
Peter Jansweijer	peterj@nikhef.nl

NIKHEF
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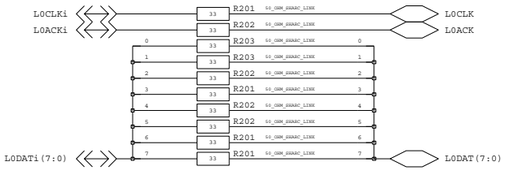
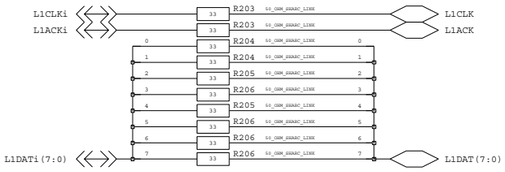
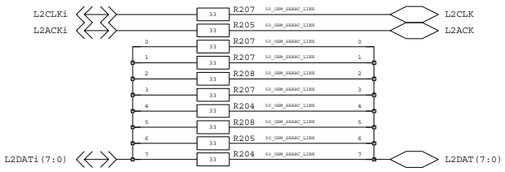
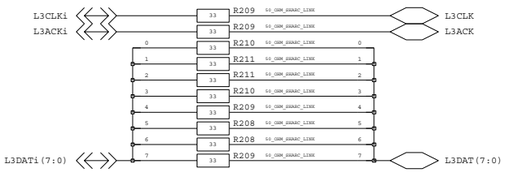
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND

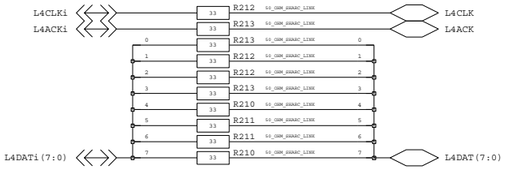
Rev	V2 2
Date	7 Feb 2006
Time	1:46:33 pm
Name	tonvr
Size	A3 4 1 4 A
Dim	420 x 297 mm
Page	2 of 4

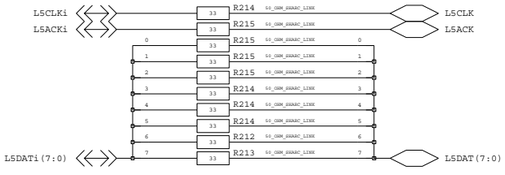




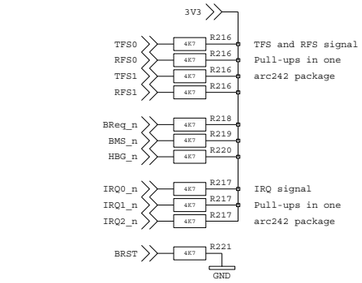


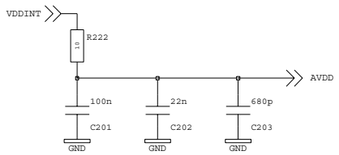


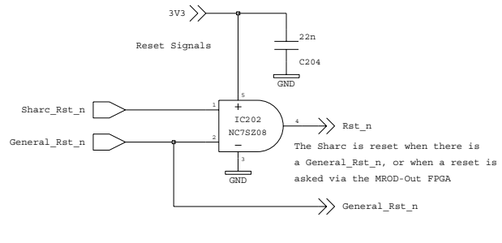


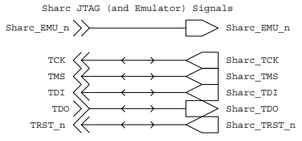


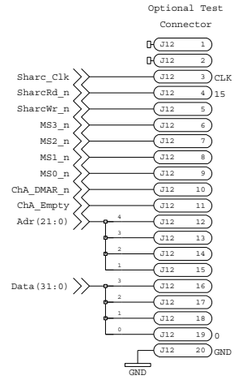
SHARC Link Serie Termination

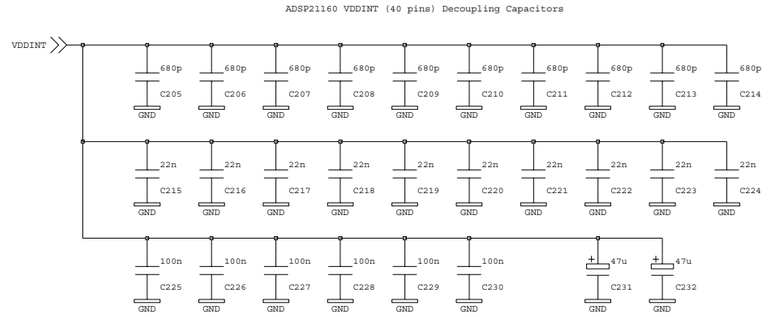


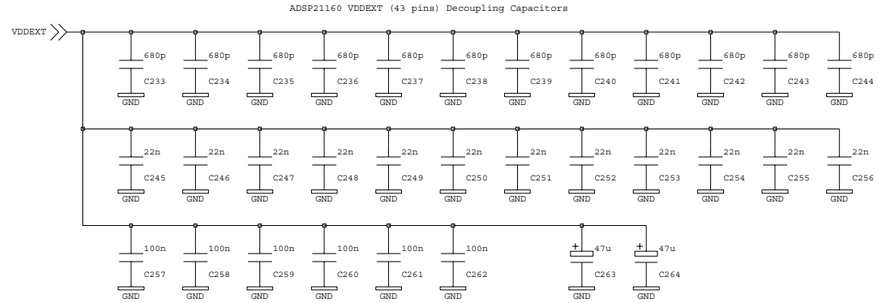






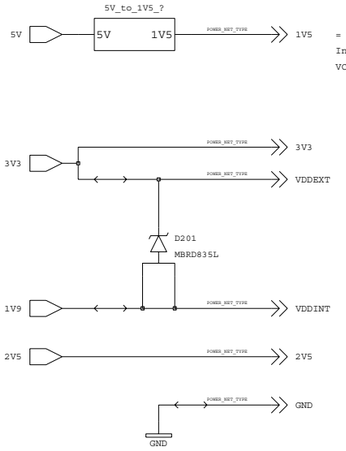






Fiducial201 Fiducial202

MROD-In		Rev V2 2
		Date 7 Feb 2006
SHARC Auxiliary and Decoupling		Time 1:46:57 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 3 of 4



= VCCINT for Xilinx Virtex-II Pro in the
Input Channels, 600 mA per Channel
VCCINT Ramp rate 200 us min. and 50 ms max.

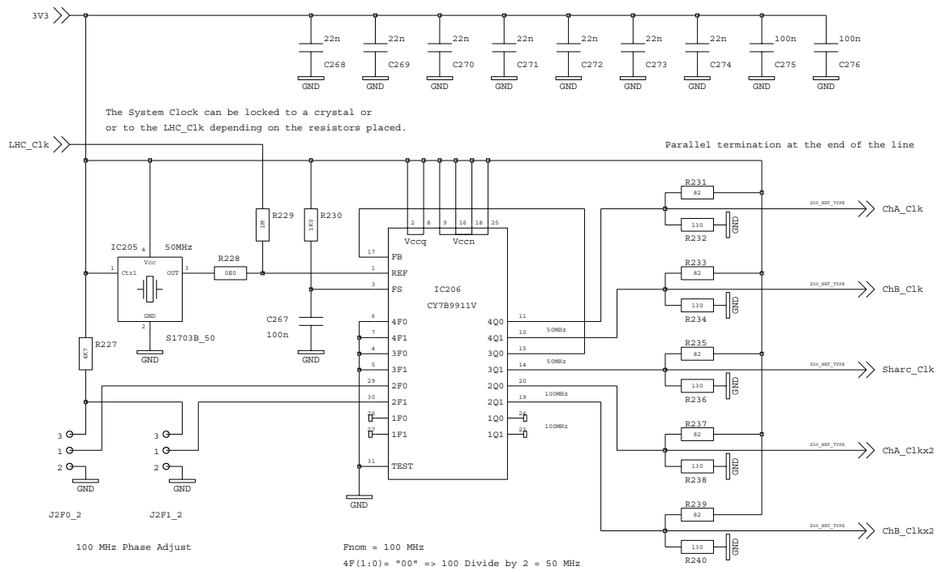
= VDDEXT for the ADSP21160N
100 mA per ADSP21160N

Note ADSP21160N Power-On Sequence!
Time between power-on VDDINT -> VDDEXT
= -50 ms to +200 ms

= VDDINT for the ADSP21160N
960 mA peak per ADSP21160N

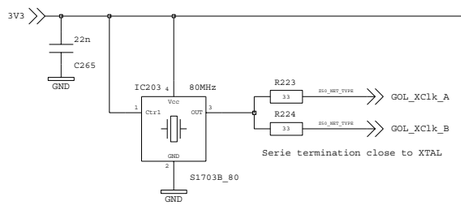
= VCCAUX for the Xilinx Virtex-II Pro in the
Input Channel, 250 mA per Channel

All GND nets on the SHARC need
to be connected to golbal GROUND.

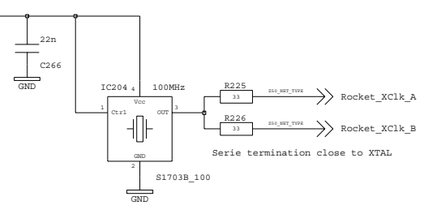


Fnom = 100 MHz
4F(1:0)= "00" => 100 Divide by 2 = 50 MHz
3F(1:0)= "00" => 100 Divide by 2 = 50 MHz
2F(1:0)= "mm" => 0 tu
1F(1:0)= "mm" => 0 tu

SHARC and Input Channel System Clock

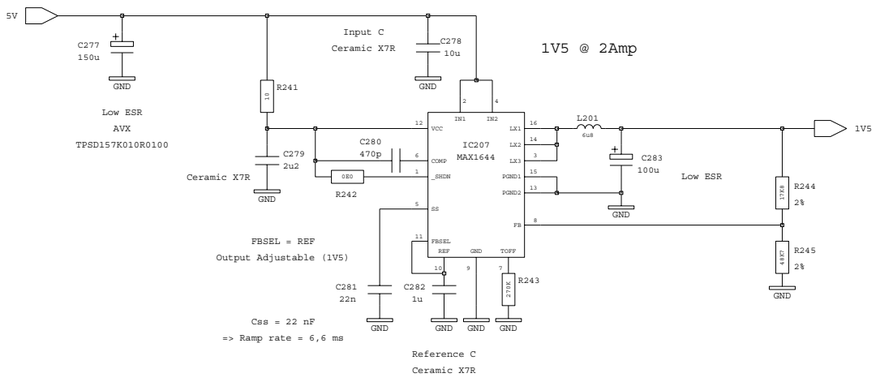


GOL Frequency
80 MHz 16 bit = 40 MHz 32 bit
= 160 MB/s

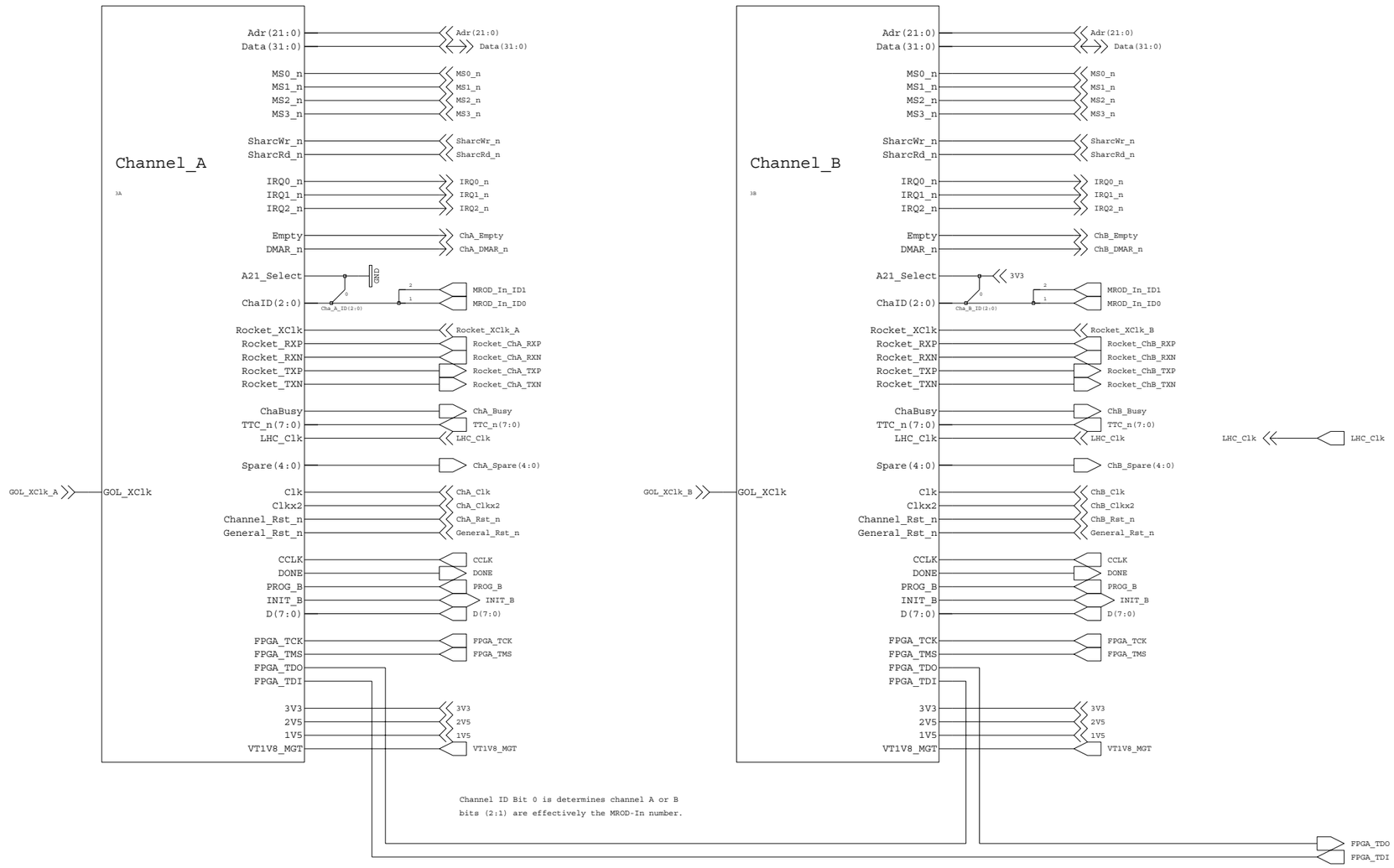


Rocket-IO Inter-FPGA Link Frequency
100 MHz 16 bit = 50 MHz 32 bit
= 200 MB/s

MROD-In	Rev V2 20
	Date 7 Feb 2006
Power and Clocks	Time 1:47:20 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	
NIKHEF	Size A3 / 4 1 4 A
© ET-Nikhef Amsterdam	Dim 420 x 297 mm
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Page 4 of 4



Power Supply			Rev V2 2
5V -> 1V5 @ 2A			Date 7 Feb 2006
Proj: MROD-X	Proj.No: 38405		Time 1:38:24 pm
Peter Jansweijer	peterj@nikhef.nl		Name tonvr
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size A3 4 1 4 A
			Dim 420 x 297 mm
			Page 1 of 1



MROD-In		Rev V2 2	
Input Channels		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:45:51 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
© ET-Nikhef Amsterdam		Page 1 of 4	

IC301
ADSP21160N

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	A1	A2 DATA(13)	A3 DATA(10)	A4 DATA(8)	A5 DATA(4)	A6 DATA(2)	A7 TDI TDI	A8 TRST_n TRST_n	A9 RESET_n Rst_n	A10 RPBA GND	A11 IRQ0_n IRQ0_n	A12 FLAG1 ChB_Rst_n	A13 TIMEXP	A14 NC_A14	A15 NC_A15	A16 TFS1 TFS1	A17 RFS1 RFS1	A18 RCLK0	A19 DT0	A20 L0DAT(4) L0DATi(4)
B	B1 DATA(22)	B2 DATA(16)	B3 DATA(15)	B4 DATA(9)	B5 DATA(6)	B6 DATA(3)	B7 DATA(0)	B8 TCK TCK	B9 EMU_n Sharc_EMU_n	B10 IRQ2_n IRQ2_n	B11 FLAG3 ChB_Empty	B12 FLAG0 ChA_Rst_n	B13 NC_B13	B14 NC_B14	B15 DT1	B16 RCLK1	B17 RFS0 RFS0	B18 TCLK0	B19 L0DAT(5) L0DATi(5)	B20 L0DAT(2) L0DATi(2)
C	C1 DATA(24)	C2 DATA(18)	C3 DATA(17)	C4 DATA(11)	C5 DATA(7)	C6 DATA(5)	C7 DATA(1)	C8 TMS TMS	C9 TDO TDO	C10 IRQ1_n IRQ1_n	C11 FLAG2 ChA_Empty	C12 NC_C12	C13 NC_C13	C14 TCLK1	C15 DR1	C16 DR0	C17 L0DAT(7) L0DATi(7)	C18 L0DAT(6) L0DATi(6)	C19 L0ACK L0ACKi	C20 L0DAT(0) L0DATi(0)
D	D1 DATA(28)	D2 DATA(25)	D3 DATA(20)	D4 DATA(19)	D5 DATA(12)	D6 VDDEXT_D6 VDDEXT	D7 VDDINT_D7 VDDINT	D8 VDDEXT_D8 VDDEXT	D9 VDDEXT_D9 VDDEXT	D10 VDDEXT_D10 VDDEXT	D11 VDDEXT_D11 VDDEXT	D12 VDDEXT_D12 VDDEXT	D13 VDDINT_D13 VDDINT	D14 VDDEXT_D14 VDDEXT	D15 TFS0 TFS0	D16 L1DAT(7) L1DATi(7)	D17 L0CLK L0CLKi	D18 L0DAT(3) L0DATi(3)	D19 L0DAT(1) L0DATi(1)	D20 L1CLK L1CLKi
E	E1 DATA(30)	E2 DATA(29)	E3 DATA(23)	E4 DATA(21)	E5 VDDEXT_E5 VDDEXT	E6 VDDINT_E6 VDDINT	E7 VDDINT_E7 VDDINT	E8 VDDINT_E8 VDDINT	E9 VDDINT_E9 VDDINT	E10 VDDINT_E10 VDDINT	E11 GND_E11 GND	E12 VDDINT_E12 VDDINT	E13 VDDINT_E13 VDDINT	E14 VDDINT_E14 VDDINT	E15 VDDINT_E15 VDDINT	E16 VDDEXT_E16 VDDEXT	E17 L1DAT(6) L1DATi(6)	E18 L1DAT(5) L1DATi(5)	E19 L1ACK L1ACKi	E20 L1DAT(1) L1DATi(1)
F	F1 DATA(34) Data(2)	F2 DATA(33) Data(1)	F3 DATA(27)	F4 DATA(26)	F5 VDDEXT_F5 VDDEXT	F6 VDDINT_F6 VDDINT	F7 GND_F7 GND	F8 GND_F8 GND	F9 GND_F9 GND	F10 GND_F10 GND	F11 GND_F11 GND	F12 GND_F12 GND	F13 GND_F13 GND	F14 GND_F14 GND	F15 VDDINT_F15 VDDINT	F16 VDDEXT_F16 VDDEXT	F17 L1DAT(4) L1DATi(4)	F18 L1DAT(3) L1DATi(3)	F19 L1DAT(0) L1DATi(0)	F20 L2DAT(7) L2DATi(7)
G	G1 DATA(38) Data(6)	G2 DATA(35) Data(3)	G3 DATA(32) Data(0)	G4 DATA(31)	G5 VDDEXT_G5 VDDEXT	G6 VDDINT_G6 VDDINT	G7 GND_G7 GND	G8 GND_G8 GND	G9 GND_G9 GND	G10 GND_G10 GND	G11 GND_G11 GND	G12 GND_G12 GND	G13 GND_G13 GND	G14 GND_G14 GND	G15 VDDINT_G15 VDDINT	G16 VDDEXT_G16 VDDEXT	G17 L1DAT(2) L1DATi(2)	G18 L2DAT(6) L2DATi(6)	G19 L2DAT(4) L2DATi(4)	G20 L2CLK L2CLKi
H	H1 DATA(40) Data(8)	H2 DATA(39) Data(7)	H3 DATA(37) Data(5)	H4 DATA(36) Data(4)	H5 VDDEXT_H5 VDDEXT	H6 VDDINT_H6 VDDINT	H7 GND_H7 GND	H8 GND_H8 GND	H9 GND_H9 GND	H10 GND_H10 GND	H11 GND_H11 GND	H12 GND_H12 GND	H13 GND_H13 GND	H14 GND_H14 GND	H15 VDDINT_H15 VDDINT	H16 VDDEXT_H16 VDDEXT	H17 L2DAT(5) L2DATi(5)	H18 L2ACK L2ACKi	H19 L2DAT(3) L2DATi(3)	H20 L2DAT(1) L2DATi(1)
J	J1 DATA(44) Data(12)	J2 DATA(43) Data(11)	J3 DATA(42) Data(10)	J4 DATA(41) Data(9)	J5 VDDEXT_J5 VDDEXT	J6 VDDINT_J6 VDDINT	J7 GND_J7 GND	J8 GND_J8 GND	J9 GND_J9 GND	J10 GND_J10 GND	J11 GND_J11 GND	J12 GND_J12 GND	J13 GND_J13 GND	J14 GND_J14 GND	J15 VDDINT_J15 VDDINT	J16 VDDEXT_J16 VDDEXT	J17 L2DAT(2) L2DATi(2)	J18 L2DAT(0) L2DATi(0)	J19 HBG_n HBG_n	J20 HBR_n VDDEXT
K	K1 CLK_CFG_0 GND	K2 DATA(46) Data(14)	K3 DATA(45) Data(13)	K4 DATA(47) Data(15)	K5 VDDEXT_K5 VDDEXT	K6 VDDINT_K6 VDDINT	K7 GND_K7 GND	K8 GND_K8 GND	K9 GND_K9 GND	K10 GND_K10 GND	K11 GND_K11 GND	K12 GND_K12 GND	K13 GND_K13 GND	K14 GND_K14 GND	K15 VDDINT_K15 VDDINT	K16 VDDEXT_K16 VDDEXT	K17 BR6_n BReq_n	K18 BR5_n BReq_n	K19 BR4_n BReq_n	K20 BR3_n BReq_n
L	L1 CLKIN Sharc_Clk	L2 CLK_CFG_1 VDDEXT	L3 AGND GND	L4 CLK_CFG_2 GND	L5 VDDEXT_L5 VDDEXT	L6 VDDINT_L6 VDDINT	L7 GND_L7 GND	L8 GND_L8 GND	L9 GND_L9 GND	L10 GND_L10 GND	L11 GND_L11 GND	L12 GND_L12 GND	L13 GND_L13 GND	L14 GND_L14 GND	L15 VDDINT_L15 VDDINT	L16 VDDEXT_L16 VDDEXT	L17 BR2_n BReq_n	L18 BR1_n BReq_n	L19 ACK	L20 REDY
M	M1 AVDD AVDD	M2 CLK_CFG_3 GND	M3 CLKOUT	M4 NC_M4	M5 VDDEXT_M5 VDDEXT	M6 VDDINT_M6 VDDINT	M7 GND_M7 GND	M8 GND_M8 GND	M9 GND_M9 GND	M10 GND_M10 GND	M11 GND_M11 GND	M12 GND_M12 GND	M13 GND_M13 GND	M14 GND_M14 GND	M15 VDDINT_M15 VDDINT	M16 VDDEXT_M16 VDDEXT	M17 PAGE	M18 SBTS_n VDDEXT	M19 PA_n	M20 L3DAT(7) L3DATi(7)
N	N1 NC_N1	N2 NC_N2	N3 DATA(48) Data(16)	N4 DATA(51) Data(19)	N5 VDDEXT_N5 VDDEXT	N6 VDDINT_N6 VDDINT	N7 GND_N7 GND	N8 GND_N8 GND	N9 GND_N9 GND	N10 GND_N10 GND	N11 GND_N11 GND	N12 GND_N12 GND	N13 GND_N13 GND	N14 GND_N14 GND	N15 VDDINT_N15 VDDINT	N16 VDDEXT_N16 VDDEXT	N17 L3DAT(5) L3DATi(5)	N18 L3DAT(6) L3DATi(6)	N19 L3DAT(4) L3DATi(4)	N20 L3CLK L3CLKi
P	P1 DATA(49) Data(17)	P2 DATA(50) Data(18)	P3 DATA(52) Data(20)	P4 DATA(55) Data(23)	P5 VDDEXT_P5 VDDEXT	P6 VDDINT_P6 VDDINT	P7 GND_P7 GND	P8 GND_P8 GND	P9 GND_P9 GND	P10 GND_P10 GND	P11 GND_P11 GND	P12 GND_P12 GND	P13 GND_P13 GND	P14 GND_P14 GND	P15 VDDINT_P15 VDDINT	P16 VDDEXT_P16 VDDEXT	P17 L3DAT(2) L3DATi(2)	P18 L3DAT(1) L3DATi(1)	P19 L3DAT(3) L3DATi(3)	P20 L3ACK L3ACKi
R	R1 DATA(53) Data(21)	R2 DATA(54) Data(22)	R3 DATA(57) Data(25)	R4 DATA(60) Data(28)	R5 VDDEXT_R5 VDDEXT	R6 VDDINT_R6 VDDINT	R7 GND_R7 GND	R8 GND_R8 GND	R9 GND_R9 GND	R10 GND_R10 GND	R11 GND_R11 GND	R12 GND_R12 GND	R13 GND_R13 GND	R14 GND_R14 GND	R15 GND_R15 GND	R16 VDDEXT_R16 VDDEXT	R17 L4DAT(5) L4DATi(5)	R18 L4DAT(6) L4DATi(6)	R19 L4DAT(7) L4DATi(7)	R20 L3DAT(0) L3DATi(0)
T	T1 DATA(56) Data(24)	T2 DATA(58) Data(26)	T3 DATA(59) Data(27)	T4 DATA(63) Data(31)	T5 VDDEXT_T5 VDDEXT	T6 VDDINT_T6 VDDINT	T7 VDDINT_T7 VDDINT	T8 VDDINT_T8 VDDINT	T9 VDDINT_T9 VDDINT	T10 VDDINT_T10 VDDINT	T11 VDDINT_T11 VDDINT	T12 VDDINT_T12 VDDINT	T13 VDDINT_T13 VDDINT	T14 VDDINT_T14 VDDINT	T15 VDDINT_T15 VDDINT	T16 VDDEXT_T16 VDDEXT	T17 L4DAT(3) L4DATi(3)	T18 L4ACK L4ACKi	T19 L4CLK L4CLKi	T20 L4DAT(4) L4DATi(4)
U	U1 DATA(61) Data(29)	U2 DATA(62) Data(30)	U3 ADDR(3) Adr(3)	U4 ADDR(2) Adr(2)	U5 VDDEXT_U5 VDDEXT	U6 VDDEXT_U6 VDDEXT	U7 VDDEXT_U7 VDDEXT	U8 VDDEXT_U8 VDDEXT	U9 VDDEXT_U9 VDDEXT	U10 VDDEXT_U10 VDDEXT	U11 VDDEXT_U11 VDDEXT	U12 VDDEXT_U12 VDDEXT	U13 VDDEXT_U13 VDDEXT	U14 VDDEXT_U14 VDDEXT	U15 VDDEXT_U15 VDDEXT	U16 VDDEXT_U16 VDDEXT	U17 L5DAT(7) L5DATi(7)	U18 L4DAT(0) L4DATi(0)	U19 L4DAT(1) L4DATi(1)	U20 L4DAT(2) L4DATi(2)
V	V1 ADDR(4) Adr(4)	V2 ADDR(6) Adr(6)	V3 ADDR(7) Adr(7)	V4 ADDR(10) Adr(10)	V5 ADDR(14) Adr(14)	V6 ADDR(18) Adr(18)	V7 ADDR(22)	V8 ADDR(25)	V9 ADDR(28)	V10 ID0 GND	V11 ADDR(1) Adr(1)	V12 MS1_n MS1_n	V13 CS_n VDDEXT	V14 RDL_n	V15 DMAR2_n ChB_DMAR_n	V16 L5DAT(0) L5DATi(0)	V17 L5DAT(2) L5DATi(2)	V18 L5ACK L5ACKi	V19 L5DAT(4) L5DATi(4)	V20 L5DAT(6) L5DATi(6)
W	W1 ADDR(5) Adr(5)	W2 ADDR(9) Adr(9)	W3 ADDR(12) Adr(12)	W4 ADDR(15) Adr(15)	W5 ADDR(17) Adr(17)	W6 ADDR(20) Adr(20)	W7 ADDR(23)	W8 ADDR(26)	W9 ADDR(29)	W10 ID1 GND	W11 ADDR(0) Adr(0)	W12 BMS_n BMS_n	W13 MS2_n MS2_n	W14 CIP_n	W15 RDH_n SharcRd_n	W16 DMAG2_n	W17 LBOOT VDDEXT	W18 L5DAT(1) L5DATi(1)	W19 L5DAT(3) L5DATi(3)	W20 L5DAT(5) L5DATi(5)
Y	Y1 ADDR(8) Adr(8)	Y2 ADDR(11) Adr(11)	Y3 ADDR(13) Adr(13)	Y4 ADDR(16) Adr(16)	Y5 ADDR(19) Adr(19)	Y6 ADDR(21) Adr(21)	Y7 ADDR(24)	Y8 ADDR(27)	Y9 ADDR(30)	Y10 ADDR(31)	Y11 ID2 GND	Y12 BRST BRST	Y13 MS0_n MS0_n	Y14 MS3_n MS3_n	Y15 WRH_n SharcWr_n	Y16 WRL_n	Y17 DMAG1_n DMAG1_n	Y18 DMAR1_n ChA_DMAR_n	Y19 EBOOT GND	Y20 L5CLK L5CLKi

Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

ID = "000"

Booting Mode:
EBOOT = '0', LBOOT = '1', BMS_n = '1' (Input)
=> Link Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

MROD-In

SHARC

Proj: MROD-X | Proj.No: 38405

Peter Jansweijer | peterj@nikhef.nl

NIKHEF

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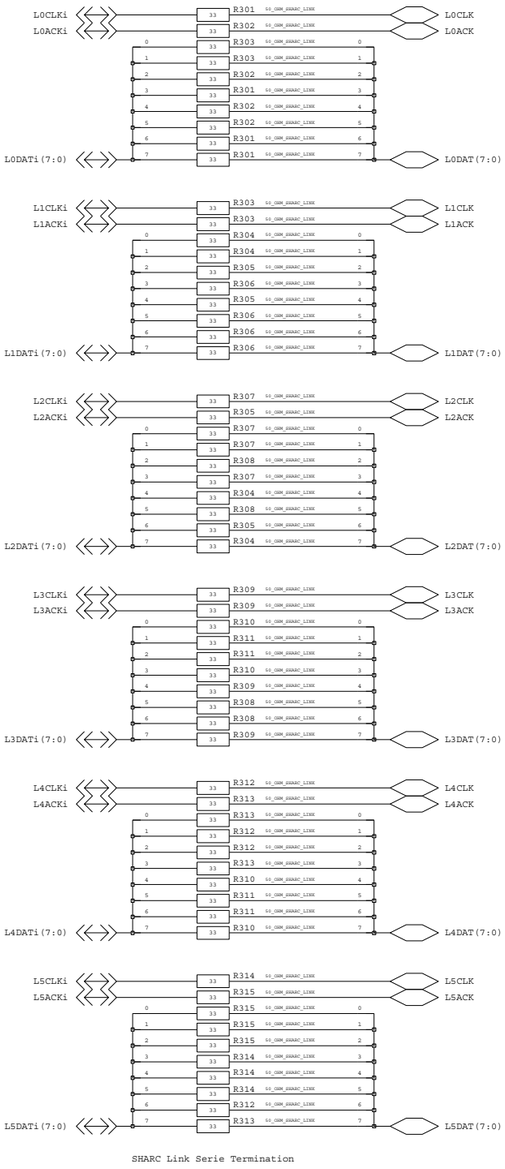
NATIONAAL INSTITUUT VOOR KERN-
FYSICA EN HOGE ENERGIE-FYSICA
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND

Rev	V2 2
Date	7 Feb 2006
Time	1:46:33 pm
Name	tonvr
Size	A3 4 1 4 A
Dim	420 x 297 mm
Page	2 of 4



Communication Link

Communication Link

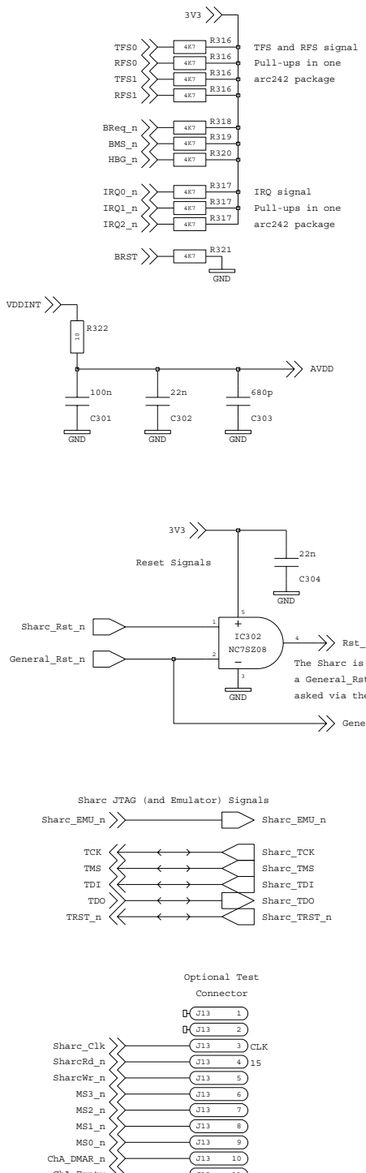
Communication Link

Data Link to MROD-Out Sharc-B

Data Link to MROD-Out Sharc-A
Also Boot Link

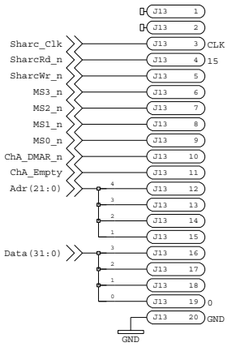
Communication Link

SHARC Link Serie Termination

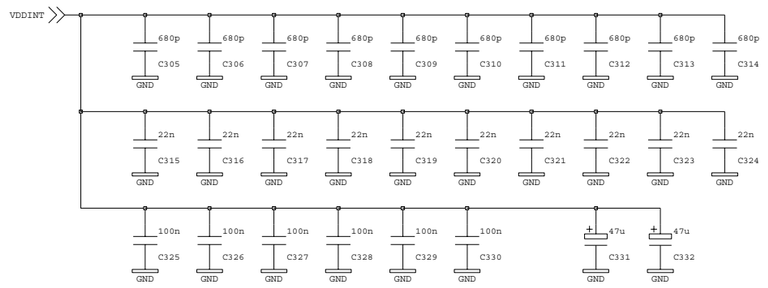


Sharc JTAG (and Emulator) Signals

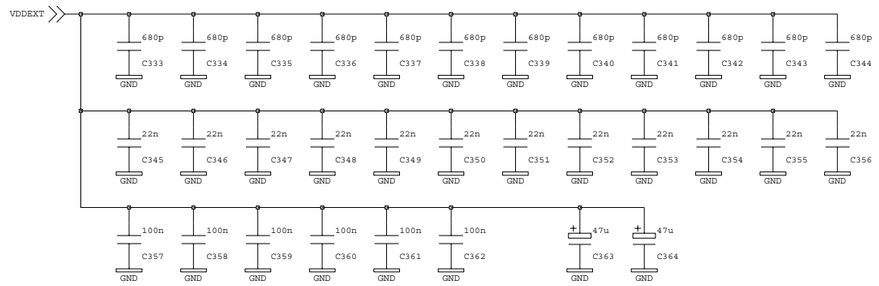
Optional Test
Connector



ADSP21160 VDDINT (40 pins) Decoupling Capacitors

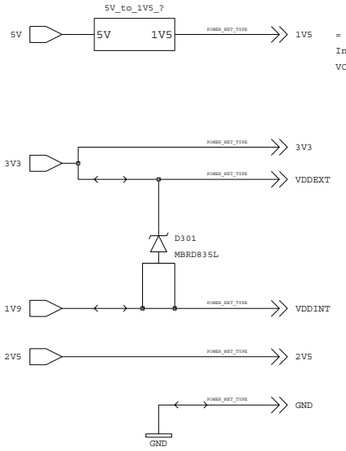


ADSP21160 VDDEXT (43 pins) Decoupling Capacitors



Fiducial301 Fiducial302

MROD-In		Rev V2 2	
		Date 7 Feb 2006	
SHARC Auxiliary and Decoupling		Time 1:46:57 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 3 of 4	



= VCCINT for Xilinx Virtex-II Pro in the
Input Channels, 600 mA per Channel
VCCINT Ramp rate 200 us min. and 50 ms max.

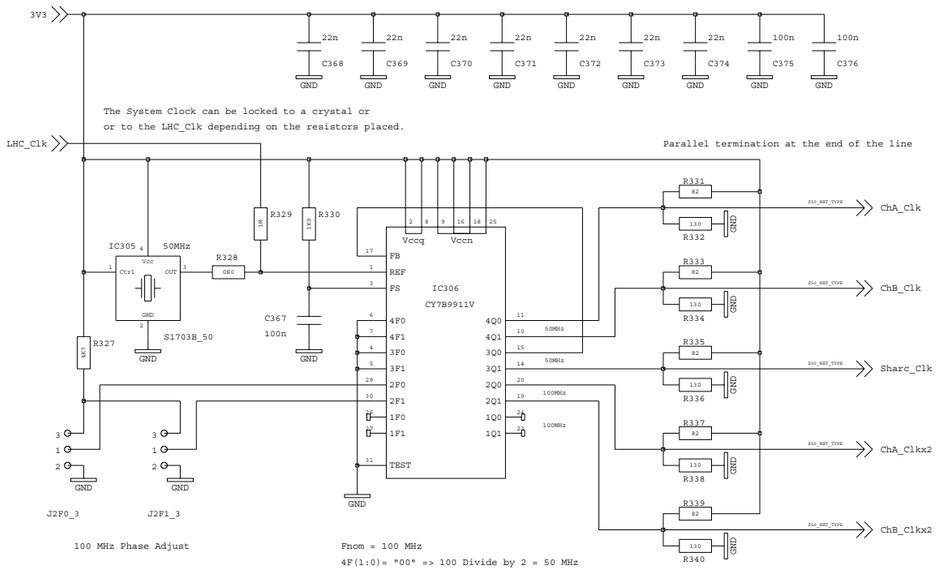
= VDDEXT for the ADSP21160N
100 mA per ADSP21160N

Note ADSP21160N Power-On Sequence!
Time between power-on VDDINT -> VDDEXT
= -50 ms to +200 ms

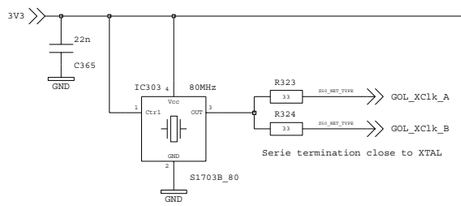
= VDDINT for the ADSP21160N
960 mA peak per ADSP21160N

= VCCAUX for the Xilinx Virtex-II Pro in the
Input Channel, 250 mA per Channel

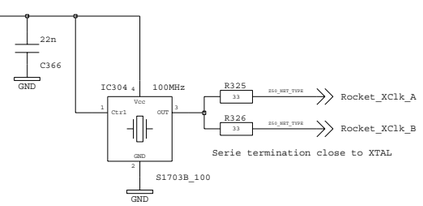
All GND nets on the SHARC need
to be connected to golbal GROUND.



SHARC and Input Channel System Clock

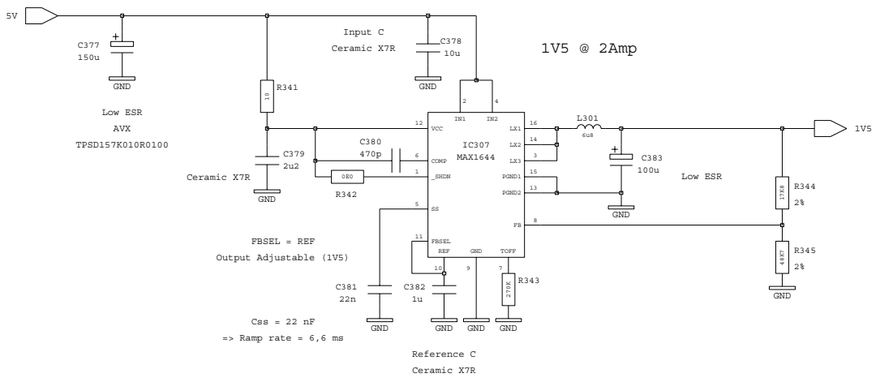


GOL Frequency
80 MHz 16 bit = 40 MHz 32 bit
= 160 MB/s

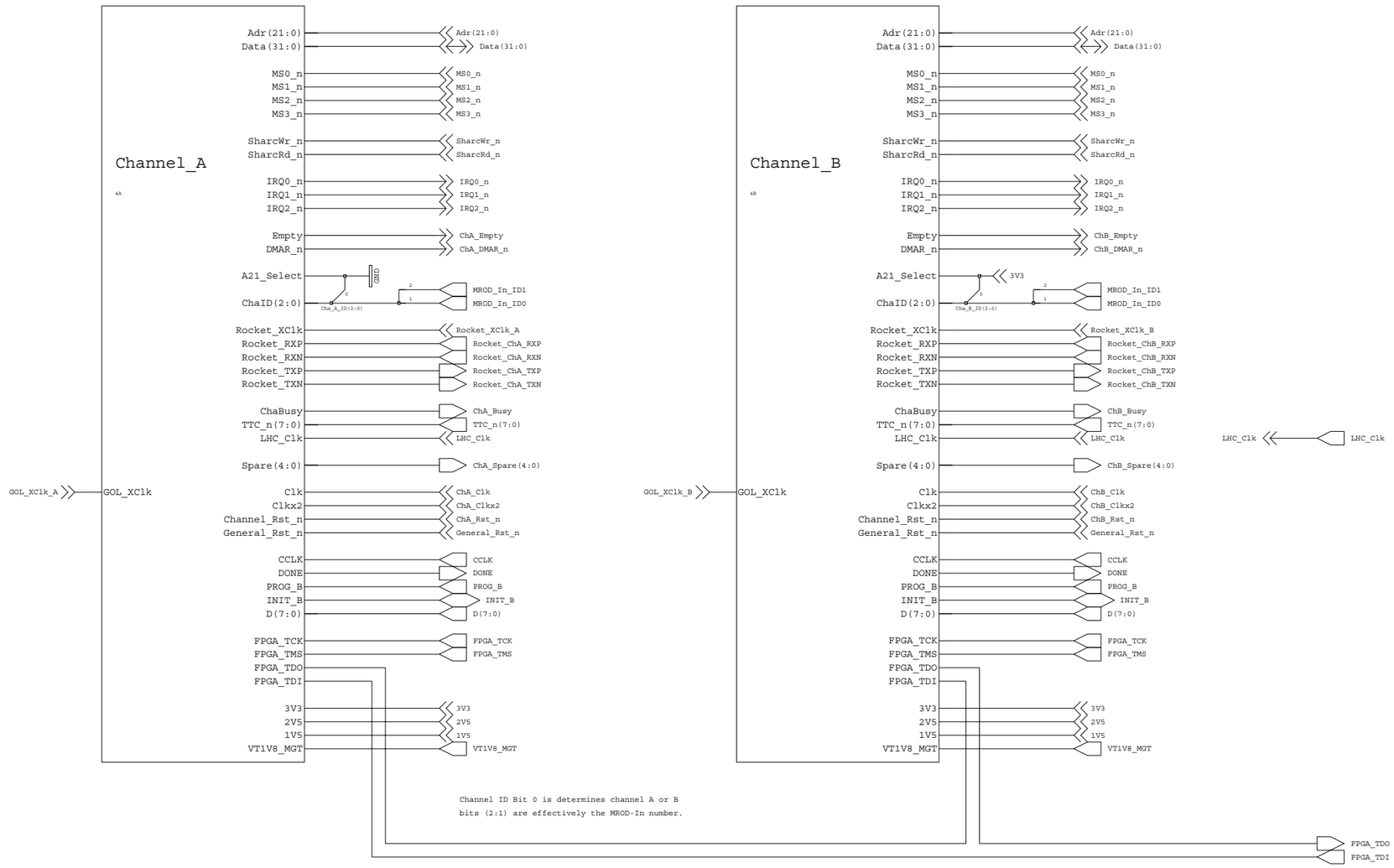


Rocket-IO Inter-FPGA Link Frequency
100 MHz 16 bit = 50 MHz 32 bit
= 200 MB/s

MROD-In		Rev V2 20	
		Date 7 Feb 2006	
Power and Clocks		Time 1:47:20 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
© ET-Nikhef Amsterdam		Page 4 of 4	



Power Supply			Rev V2 2
5V -> 1V5 @ 2A			Date 7 Feb 2006
Proj: MROD-X	Proj.No: 38405		Time 1:38:24 pm
Peter Jansweijer	peterj@nikhef.nl		Name tonvr
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size A3 4 1 4 A
			Dim 420 x 297 mm
			Page 1 of 1



MROD-In		Rev V2 2	
Input Channels		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:45:51 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
		Page 1 of 4	

IC401
ADSP21160N

A1 DATA(14)	A2 DATA(13)	A3 DATA(10)	A4 DATA(8)	A5 DATA(4)	A6 DATA(2)	A7 TDI TDI	A8 TRST_n TRST_n	A9 RESET_n Rst_n	A10 RPBA GND	A11 IRQ0_n IRQ0_n	A12 FLAG1 ChB_Rst_n	A13 TIMEXP	A14 NC_A14	A15 NC_A15	A16 TFS1 TFS1	A17 RFS1 RFS1	A18 RCLK0	A19 DT0	A20 L0DAT(4) L0DATi(4)
B1 DATA(22)	B2 DATA(16)	B3 DATA(15)	B4 DATA(9)	B5 DATA(6)	B6 DATA(3)	B7 DATA(0)	B8 TCK TCK	B9 EMU_n Sharc_EMU_n	B10 IRQ2_n IRQ2_n	B11 FLAG3 ChB_Empty	B12 FLAG0 ChA_Rst_n	B13 NC_B13	B14 NC_B14	B15 DT1	B16 RCLK1	B17 RFS0 RFS0	B18 TCLK0	B19 L0DAT(5) L0DATi(5)	B20 L0DAT(2) L0DATi(2)
C1 DATA(24)	C2 DATA(18)	C3 DATA(17)	C4 DATA(11)	C5 DATA(7)	C6 DATA(5)	C7 DATA(1)	C8 TMS TMS	C9 TDO TDO	C10 IRQ1_n IRQ1_n	C11 FLAG2 ChA_Empty	C12 NC_C12	C13 NC_C13	C14 TCLK1	C15 DR1	C16 DR0	C17 L0DAT(7) L0DATi(7)	C18 L0DAT(6) L0DATi(6)	C19 L0ACK L0ACKi	C20 L0DAT(0) L0DATi(0)
D1 DATA(28)	D2 DATA(25)	D3 DATA(20)	D4 DATA(19)	D5 DATA(12)	D6 VDDEXT_D6 VDDEXT	D7 VDDINT_D7 VDDINT	D8 VDDEXT_D8 VDDEXT	D9 VDDEXT_D9 VDDEXT	D10 VDDEXT_D10 VDDEXT	D11 VDDEXT_D11 VDDEXT	D12 VDDEXT_D12 VDDEXT	D13 VDDINT_D13 VDDINT	D14 VDDEXT_D14 VDDEXT	D15 TFS0 TFS0	D16 L1DAT(7) L1DATi(7)	D17 L0CLK L0CLKi	D18 L0DAT(3) L0DATi(3)	D19 L0DAT(1) L0DATi(1)	D20 L1CLK L1CLKi
E1 DATA(30)	E2 DATA(29)	E3 DATA(23)	E4 DATA(21)	E5 VDDEXT_E5 VDDEXT	E6 VDDINT_E6 VDDINT	E7 VDDINT_E7 VDDINT	E8 VDDINT_E8 VDDINT	E9 VDDINT_E9 VDDINT	E10 VDDINT_E10 VDDINT	E11 GND_E11 GND	E12 VDDINT_E12 VDDINT	E13 VDDINT_E13 VDDINT	E14 VDDINT_E14 VDDINT	E15 VDDINT_E15 VDDINT	E16 VDDEXT_E16 VDDEXT	E17 L1DAT(6) L1DATi(6)	E18 L1DAT(5) L1DATi(5)	E19 L1ACK L1ACKi	E20 L1DAT(1) L1DATi(1)
F1 DATA(34) Data(2)	F2 DATA(33) Data(1)	F3 DATA(27)	F4 DATA(26)	F5 VDDEXT_F5 VDDEXT	F6 VDDINT_F6 VDDINT	F7 GND_F7 GND	F8 GND_F8 GND	F9 GND_F9 GND	F10 GND_F10 GND	F11 GND_F11 GND	F12 GND_F12 GND	F13 GND_F13 GND	F14 GND_F14 GND	F15 VDDINT_F15 VDDINT	F16 VDDEXT_F16 VDDEXT	F17 L1DAT(4) L1DATi(4)	F18 L1DAT(3) L1DATi(3)	F19 L1DAT(0) L1DATi(0)	F20 L2DAT(7) L2DATi(7)
G1 DATA(38) Data(6)	G2 DATA(35) Data(3)	G3 DATA(32) Data(0)	G4 DATA(31)	G5 VDDEXT_G5 VDDEXT	G6 VDDINT_G6 VDDINT	G7 GND_G7 GND	G8 GND_G8 GND	G9 GND_G9 GND	G10 GND_G10 GND	G11 GND_G11 GND	G12 GND_G12 GND	G13 GND_G13 GND	G14 GND_G14 GND	G15 VDDINT_G15 VDDINT	G16 VDDEXT_G16 VDDEXT	G17 L1DAT(2) L1DATi(2)	G18 L2DAT(6) L2DATi(6)	G19 L2DAT(4) L2DATi(4)	G20 L2CLK L2CLKi
H1 DATA(40) Data(8)	H2 DATA(39) Data(7)	H3 DATA(37) Data(5)	H4 DATA(36) Data(4)	H5 VDDEXT_H5 VDDEXT	H6 VDDINT_H6 VDDINT	H7 GND_H7 GND	H8 GND_H8 GND	H9 GND_H9 GND	H10 GND_H10 GND	H11 GND_H11 GND	H12 GND_H12 GND	H13 GND_H13 GND	H14 GND_H14 GND	H15 VDDINT_H15 VDDINT	H16 VDDEXT_H16 VDDEXT	H17 L2DAT(5) L2DATi(5)	H18 L2ACK L2ACKi	H19 L2DAT(3) L2DATi(3)	H20 L2DAT(1) L2DATi(1)
J1 DATA(44) Data(12)	J2 DATA(43) Data(11)	J3 DATA(42) Data(10)	J4 DATA(41) Data(9)	J5 VDDEXT_J5 VDDEXT	J6 VDDINT_J6 VDDINT	J7 GND_J7 GND	J8 GND_J8 GND	J9 GND_J9 GND	J10 GND_J10 GND	J11 GND_J11 GND	J12 GND_J12 GND	J13 GND_J13 GND	J14 GND_J14 GND	J15 VDDINT_J15 VDDINT	J16 VDDEXT_J16 VDDEXT	J17 L2DAT(2) L2DATi(2)	J18 L2DAT(0) L2DATi(0)	J19 HBG_n HBG_n	J20 HBR_n VDDEXT
K1 CLK_CFG_0 GND	K2 DATA(46) Data(14)	K3 DATA(45) Data(13)	K4 DATA(47) Data(15)	K5 VDDEXT_K5 VDDEXT	K6 VDDINT_K6 VDDINT	K7 GND_K7 GND	K8 GND_K8 GND	K9 GND_K9 GND	K10 GND_K10 GND	K11 GND_K11 GND	K12 GND_K12 GND	K13 GND_K13 GND	K14 GND_K14 GND	K15 VDDINT_K15 VDDINT	K16 VDDEXT_K16 VDDEXT	K17 BR6_n BReq_n	K18 BR5_n BReq_n	K19 BR4_n BReq_n	K20 BR3_n BReq_n
L1 CLKIN Sharc_Clk	L2 CLK_CFG_1 VDDEXT	L3 AGND GND	L4 CLK_CFG_2 GND	L5 VDDEXT_L5 VDDEXT	L6 VDDINT_L6 VDDINT	L7 GND_L7 GND	L8 GND_L8 GND	L9 GND_L9 GND	L10 GND_L10 GND	L11 GND_L11 GND	L12 GND_L12 GND	L13 GND_L13 GND	L14 GND_L14 GND	L15 VDDINT_L15 VDDINT	L16 VDDEXT_L16 VDDEXT	L17 BR2_n BReq_n	L18 BR1_n BReq_n	L19 ACK	L20 REDY
M1 AVDD AVDD	M2 CLK_CFG_3 GND	M3 CLKOUT	M4 NC_M4	M5 VDDEXT_M5 VDDEXT	M6 VDDINT_M6 VDDINT	M7 GND_M7 GND	M8 GND_M8 GND	M9 GND_M9 GND	M10 GND_M10 GND	M11 GND_M11 GND	M12 GND_M12 GND	M13 GND_M13 GND	M14 GND_M14 GND	M15 VDDINT_M15 VDDINT	M16 VDDEXT_M16 VDDEXT	M17 PAGE	M18 SBTS_n VDDEXT	M19 PA_n	M20 L3DAT(7) L3DATi(7)
N1 NC_N1	N2 NC_N2	N3 DATA(48) Data(16)	N4 DATA(51) Data(19)	N5 VDDEXT_N5 VDDEXT	N6 VDDINT_N6 VDDINT	N7 GND_N7 GND	N8 GND_N8 GND	N9 GND_N9 GND	N10 GND_N10 GND	N11 GND_N11 GND	N12 GND_N12 GND	N13 GND_N13 GND	N14 GND_N14 GND	N15 VDDINT_N15 VDDINT	N16 VDDEXT_N16 VDDEXT	N17 L3DAT(5) L3DATi(5)	N18 L3DAT(6) L3DATi(6)	N19 L3DAT(4) L3DATi(4)	N20 L3CLK L3CLKi
P1 DATA(49) Data(17)	P2 DATA(50) Data(18)	P3 DATA(52) Data(20)	P4 DATA(55) Data(23)	P5 VDDEXT_P5 VDDEXT	P6 VDDINT_P6 VDDINT	P7 GND_P7 GND	P8 GND_P8 GND	P9 GND_P9 GND	P10 GND_P10 GND	P11 GND_P11 GND	P12 GND_P12 GND	P13 GND_P13 GND	P14 GND_P14 GND	P15 VDDINT_P15 VDDINT	P16 VDDEXT_P16 VDDEXT	P17 L3DAT(2) L3DATi(2)	P18 L3DAT(1) L3DATi(1)	P19 L3DAT(3) L3DATi(3)	P20 L3ACK L3ACKi
R1 DATA(53) Data(21)	R2 DATA(54) Data(22)	R3 DATA(57) Data(25)	R4 DATA(60) Data(28)	R5 VDDEXT_R5 VDDEXT	R6 VDDINT_R6 VDDINT	R7 GND_R7 GND	R8 GND_R8 GND	R9 GND_R9 GND	R10 GND_R10 GND	R11 GND_R11 GND	R12 GND_R12 GND	R13 GND_R13 GND	R14 GND_R14 GND	R15 GND_R15 GND	R16 VDDEXT_R16 VDDEXT	R17 L4DAT(5) L4DATi(5)	R18 L4DAT(6) L4DATi(6)	R19 L4DAT(7) L4DATi(7)	R20 L3DAT(0) L3DATi(0)
T1 DATA(56) Data(24)	T2 DATA(58) Data(26)	T3 DATA(59) Data(27)	T4 DATA(63) Data(31)	T5 VDDEXT_T5 VDDEXT	T6 VDDINT_T6 VDDINT	T7 VDDINT_T7 VDDINT	T8 VDDINT_T8 VDDINT	T9 VDDINT_T9 VDDINT	T10 VDDINT_T10 VDDINT	T11 VDDINT_T11 VDDINT	T12 VDDINT_T12 VDDINT	T13 VDDINT_T13 VDDINT	T14 VDDINT_T14 VDDINT	T15 VDDINT_T15 VDDINT	T16 VDDEXT_T16 VDDEXT	T17 L4DAT(3) L4DATi(3)	T18 L4ACK L4ACKi	T19 L4CLK L4CLKi	T20 L4DAT(4) L4DATi(4)
U1 DATA(61) Data(29)	U2 DATA(62) Data(30)	U3 ADDR(3) Adr(3)	U4 ADDR(2) Adr(2)	U5 VDDEXT_U5 VDDEXT	U6 VDDEXT_U6 VDDEXT	U7 VDDEXT_U7 VDDEXT	U8 VDDEXT_U8 VDDEXT	U9 VDDEXT_U9 VDDEXT	U10 VDDEXT_U10 VDDEXT	U11 VDDEXT_U11 VDDEXT	U12 VDDEXT_U12 VDDEXT	U13 VDDEXT_U13 VDDEXT	U14 VDDEXT_U14 VDDEXT	U15 VDDEXT_U15 VDDEXT	U16 VDDEXT_U16 VDDEXT	U17 L5DAT(7) L5DATi(7)	U18 L4DAT(0) L4DATi(0)	U19 L4DAT(1) L4DATi(1)	U20 L4DAT(2) L4DATi(2)
V1 ADDR(4) Adr(4)	V2 ADDR(6) Adr(6)	V3 ADDR(7) Adr(7)	V4 ADDR(10) Adr(10)	V5 ADDR(14) Adr(14)	V6 ADDR(18) Adr(18)	V7 ADDR(22)	V8 ADDR(25)	V9 ADDR(28)	V10 ID0 GND	V11 ADDR(1) Adr(1)	V12 MS1_n MS1_n	V13 CS_n VDDEXT	V14 RDL_n	V15 DMAR2_n ChB_DMAR_n	V16 L5DAT(0) L5DATi(0)	V17 L5DAT(2) L5DATi(2)	V18 L5ACK L5ACKi	V19 L5DAT(4) L5DATi(4)	V20 L5DAT(6) L5DATi(6)
W1 ADDR(5) Adr(5)	W2 ADDR(9) Adr(9)	W3 ADDR(12) Adr(12)	W4 ADDR(15) Adr(15)	W5 ADDR(17) Adr(17)	W6 ADDR(20) Adr(20)	W7 ADDR(23)	W8 ADDR(26)	W9 ADDR(29)	W10 ID1 GND	W11 ADDR(0) Adr(0)	W12 BMS_n BMS_n	W13 MS2_n MS2_n	W14 CIP_n	W15 RDH_n SharcRd_n	W16 DMAG2_n	W17 LBOOT VDDEXT	W18 L5DAT(1) L5DATi(1)	W19 L5DAT(3) L5DATi(3)	W20 L5DAT(5) L5DATi(5)
Y1 ADDR(8) Adr(8)	Y2 ADDR(11) Adr(11)	Y3 ADDR(13) Adr(13)	Y4 ADDR(16) Adr(16)	Y5 ADDR(19) Adr(19)	Y6 ADDR(21) Adr(21)	Y7 ADDR(24)	Y8 ADDR(27)	Y9 ADDR(30)	Y10 ADDR(31)	Y11 ID2 GND	Y12 BRST BRST	Y13 MS0_n MS0_n	Y14 MS3_n MS3_n	Y15 WRH_n SharcWr_n	Y16 WRL_n	Y17 DMAG1_n	Y18 DMAR1_n ChA_DMAR_n	Y19 EBOOT GND	Y20 L5CLK L5CLKi

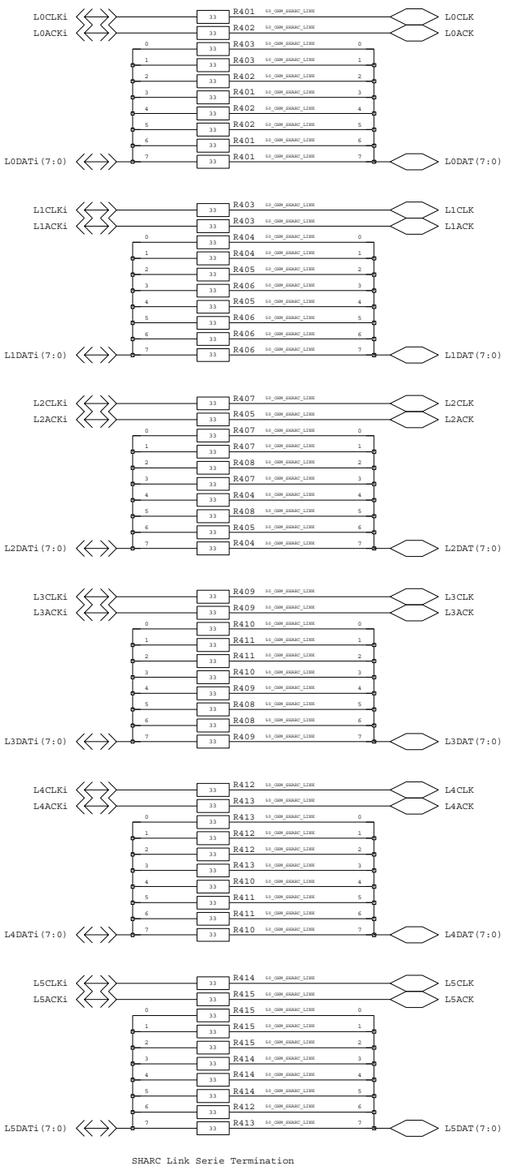
Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

ID = "000"

Booting Mode:
EBOOT = '0', LBOOT = '1', BMS_n = '1' (Input)
=> Link Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

MROD-In		Rev V2 2
		Date 7 Feb 2006
SHARC		Time 1:46:33 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF © ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A Dim 420 x 297 mm Page 2 of 4



Communication Link

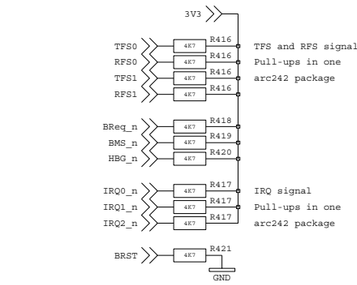
Communication Link

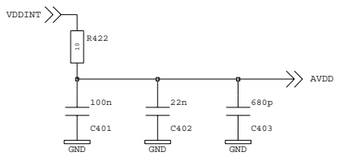
Communication Link

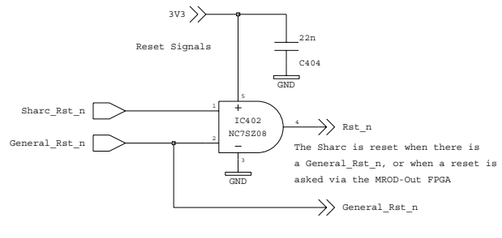
Data Link to MROD-Out Sharc-B

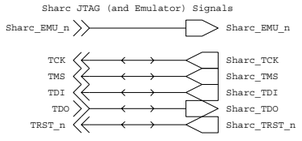
Data Link to MROD-Out Sharc-A
Also Boot Link

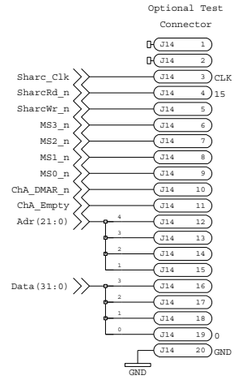
Communication Link

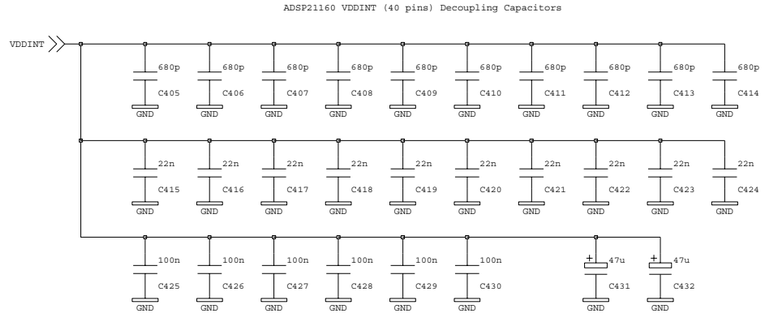


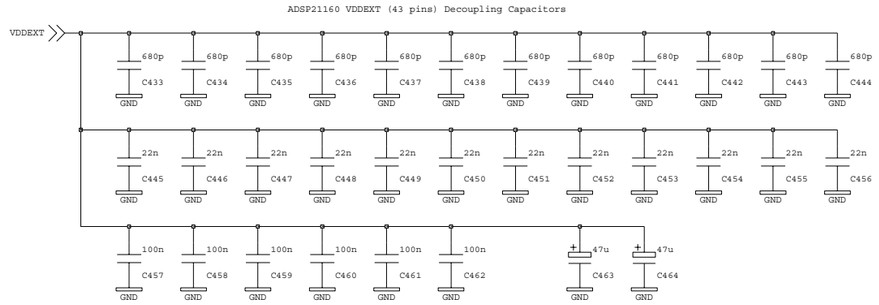






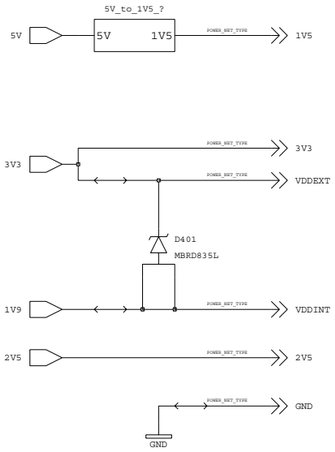






Fiducial401 Fiducial402

MROD-In		Rev V2 2	
SHARC Auxiliary and Decoupling		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:46:57 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 3 of 4	



= VCCINT for Xilinx Virtex-II Pro in the
Input Channels, 600 mA per Channel
VCCINT Ramp rate 200 us min. and 50 ms max.

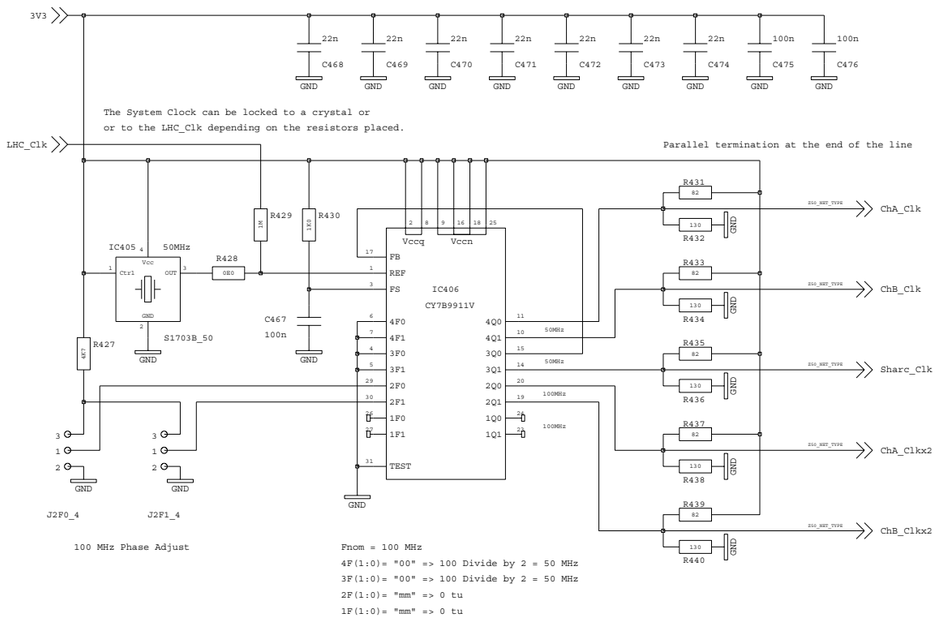
= VDDEXT for the ADSP21160N
100 mA per ADSP21160N

Note ADSP21160N Power-On Sequence!
Time between power-on VDDINT -> VDDEXT
= -50 ms to +200 ms

= VDDINT for the ADSP21160N
960 mA peak per ADSP21160N

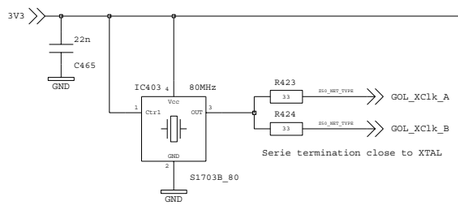
= VCCAUX for the Xilinx Virtex-II Pro in the
Input Channel, 250 mA per Channel

All GND nets on the SHARC need
to be connected to golbal GROUND.

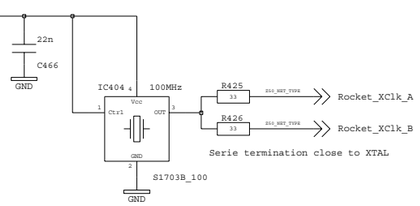


Fnom = 100 MHz
4F(1:0)= "00" => 100 Divide by 2 = 50 MHz
3F(1:0)= "00" => 100 Divide by 2 = 50 MHz
2F(1:0)= "mm" => 0 tu
1F(1:0)= "mm" => 0 tu

SHARC and Input Channel System Clock

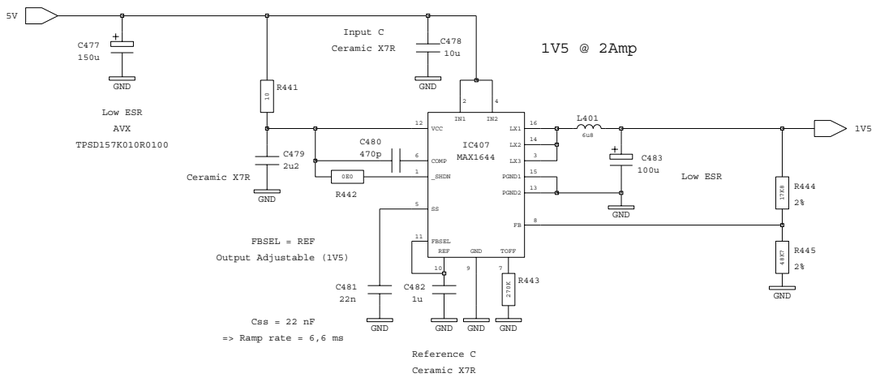


GOL Frequency
80 MHz 16 bit = 40 MHz 32 bit
= 160 MB/s

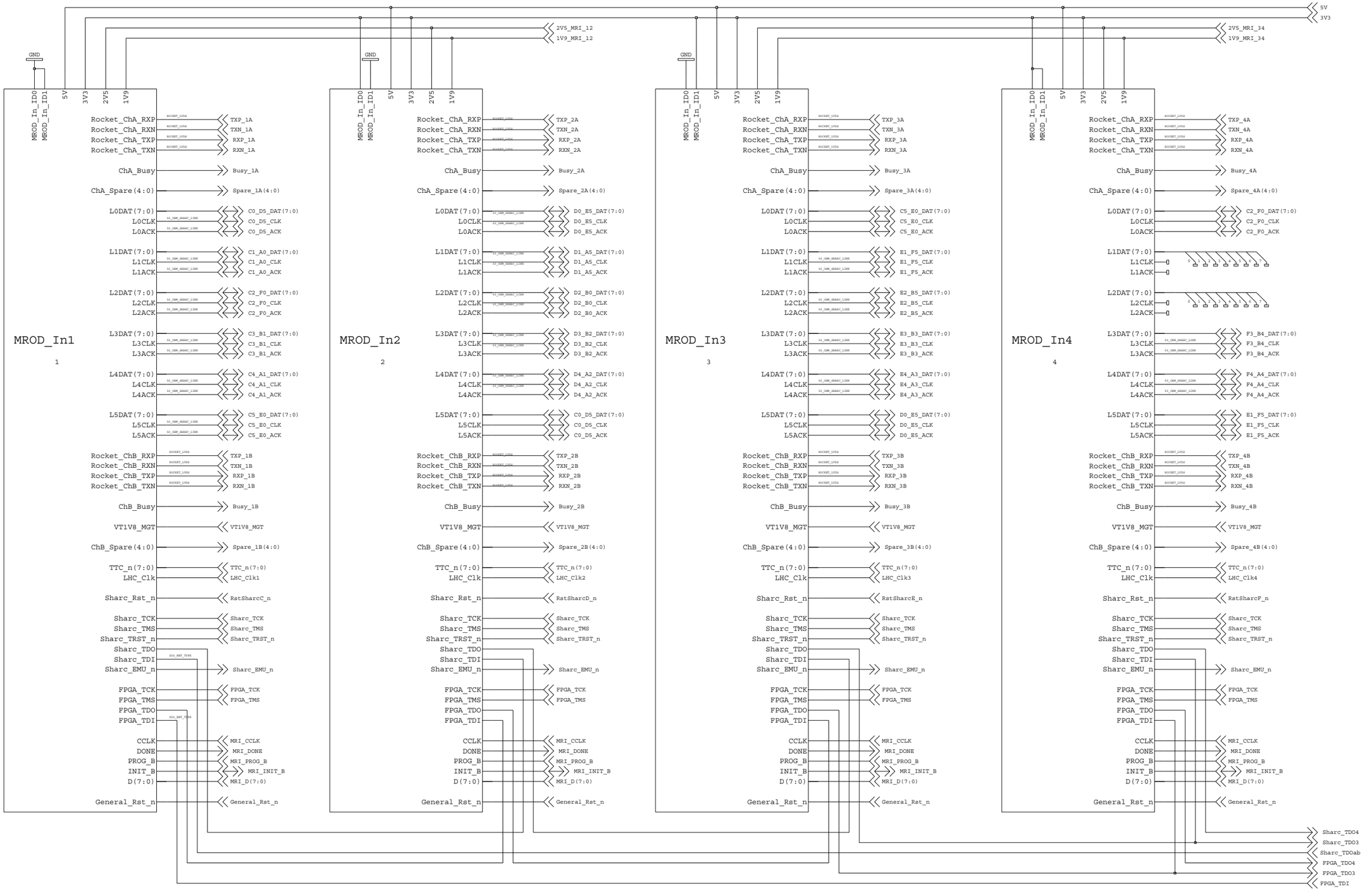


Rocket-IO Inter-FPGA Link Frequency
100 MHz 16 bit = 50 MHz 32 bit
= 200 MB/s

MROD-In		Rev V2 20	
		Date 7 Feb 2006	
Power and Clocks		Time 1:47:20 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 4 of 4	



Power Supply			Rev V2 2
5V -> 1V5 @ 2A			Date 7 Feb 2006
Proj: MROD-X	Proj.No: 38405		Time 1:38:24 pm
Peter Jansweijer	peterj@nikhef.nl		Name tonvr
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Size A3 4 1 4 A
			Dim 420 x 297 mm
			Page 1 of 1



MROD-Out		Rev V2 3	
MROD-Ins		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:25:06 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 1 of 19	

IC501
ADSP21160N

A1 DATA(14) ShareD(14)	A2 DATA(13) ShareD(13)	A3 DATA(10) ShareD(10)	A4 DATA(8) ShareD(8)	A5 DATA(4) ShareD(4)	A6 DATA(2) ShareD(2)	A7 TDI Sharc_TDI	A8 TRST_n Sharc_TRST_n	A9 RESET_n RstSharcAB_n	A10 RPBA RPBA	A11 IRQ0_n IRQ0a_n	A12 FLAG1 Flag1a	A13 TIMEXP	A14 NC_A14	A15 NC_A15	A16 TFS1 TFS1a	A17 RFS1 RFS1a	A18 RCLK0	A19 DT0	A20 L0DAT(4) L0DATa(4)
B1 DATA(22) ShareD(22)	B2 DATA(16) ShareD(16)	B3 DATA(15) ShareD(15)	B4 DATA(9) ShareD(9)	B5 DATA(6) ShareD(6)	B6 DATA(3) ShareD(3)	B7 DATA(0) ShareD(0)	B8 TCK Sharc_TCK	B9 EMU_n Sharc_EMU_n	B10 IRQ2_n IRQ2a_n	B11 FLAG3 Flag3a	B12 FLAG0 Flag0a	B13 NC_B13	B14 NC_B14	B15 DT1	B16 RCLK1	B17 RFS0 RFS0a	B18 TCLK0	B19 L0DAT(5) L0DATa(5)	B20 L0DAT(2) L0DATa(2)
C1 DATA(24) ShareD(24)	C2 DATA(18) ShareD(18)	C3 DATA(17) ShareD(17)	C4 DATA(11) ShareD(11)	C5 DATA(7) ShareD(7)	C6 DATA(5) ShareD(5)	C7 DATA(1) ShareD(1)	C8 TMS Sharc_TMS	C9 TDO Sharc_TDOa	C10 IRQ1_n IRQ1a_n	C11 FLAG2 Flag2a	C12 NC_C12	C13 NC_C13	C14 TCLK1	C15 DR1	C16 DR0	C17 L0DAT(7) L0DATa(7)	C18 L0DAT(4) L0DATa(6)	C19 L0ACK L0ACKa	C20 L0DAT(0) L0DATa(0)
D1 DATA(28) ShareD(28)	D2 DATA(25) ShareD(25)	D3 DATA(20) ShareD(20)	D4 DATA(19) ShareD(19)	D5 DATA(12) ShareD(12)	D6 VDDEXT_D6 VDDEXT	D7 VDDINT_D7 VDDINT	D8 VDDEXT_D8 VDDEXT	D9 VDDEXT_D9 VDDEXT	D10 VDDEXT_D10 VDDEXT	D11 VDDEXT_D11 VDDEXT	D12 VDDEXT_D12 VDDEXT	D13 VDDINT_D13 VDDINT	D14 VDDEXT_D14 VDDEXT	D15 TFS0 TFS0a	D16 L1DAT(7) L1DATa(7)	D17 LOCLK LOCLKa	D18 L0DAT(3) L0DATa(3)	D19 L0DAT(1) L0DATa(1)	D20 L1CLK L1CLKa
E1 DATA(30) ShareD(30)	E2 DATA(29) ShareD(29)	E3 DATA(23) ShareD(23)	E4 DATA(21) ShareD(21)	E5 VDDEXT_E5 VDDEXT	E6 VDDINT_E6 VDDINT	E7 VDDINT_E7 VDDINT	E8 VDDINT_E8 VDDINT	E9 VDDINT_E9 VDDINT	E10 VDDINT_E10 VDDINT	E11 GND_E11 GND	E12 VDDINT_E12 VDDINT	E13 VDDINT_E13 VDDINT	E14 VDDINT_E14 VDDINT	E15 VDDINT_F15 VDDINT	E16 VDDEXT_E16 VDDEXT	E17 L1DAT(6) L1DATa(6)	E18 L1DAT(5) L1DATa(5)	E19 L1ACK L1ACKa	E20 L1DAT(1) L1DATa(1)
F1 DATA(34) ShareD(34)	F2 DATA(33) ShareD(33)	F3 DATA(27) ShareD(27)	F4 DATA(26) ShareD(26)	F5 VDDEXT_F5 VDDEXT	F6 VDDINT_F6 VDDINT	F7 GND_F7 GND	F8 GND_F8 GND	F9 GND_F9 GND	F10 GND_F10 GND	F11 GND_F11 GND	F12 GND_F12 GND	F13 GND_F13 GND	F14 GND_F14 GND	F15 VDDINT_F15 VDDINT	F16 VDDEXT_F16 VDDEXT	F17 L1DAT(4) L1DATa(4)	F18 L1DAT(3) L1DATa(3)	F19 L1DAT(0) L1DATa(0)	F20 L2DAT(7) L2DATa(7)
G1 DATA(38) ShareD(38)	G2 DATA(35) ShareD(35)	G3 DATA(32) ShareD(32)	G4 DATA(31) ShareD(31)	G5 VDDEXT_G5 VDDEXT	G6 VDDINT_G6 VDDINT	G7 GND_G7 GND	G8 GND_G8 GND	G9 GND_G9 GND	G10 GND_G10 GND	G11 GND_G11 GND	G12 GND_G12 GND	G13 GND_G13 GND	G14 GND_G14 GND	G15 VDDINT_G15 VDDINT	G16 VDDEXT_G16 VDDEXT	G17 L1DAT(2) L1DATa(2)	G18 L2DAT(6) L2DATa(6)	G19 L2DAT(4) L2DATa(4)	G20 L2CLK L2CLKa
H1 DATA(40) ShareD(40)	H2 DATA(39) ShareD(39)	H3 DATA(37) ShareD(37)	H4 DATA(36) ShareD(36)	H5 VDDEXT_H5 VDDEXT	H6 VDDINT_H6 VDDINT	H7 GND_H7 GND	H8 GND_H8 GND	H9 GND_H9 GND	H10 GND_H10 GND	H11 GND_H11 GND	H12 GND_H12 GND	H13 GND_H13 GND	H14 GND_H14 GND	H15 VDDINT_H15 VDDINT	H16 VDDEXT_H16 VDDEXT	H17 L2DAT(5) L2DATa(5)	H18 L2ACK L2ACKa	H19 L2SAT(3) L2SATa(3)	H20 L2DAT(1) L2DATa(1)
J1 DATA(44) ShareD(44)	J2 DATA(43) ShareD(43)	J3 DATA(42) ShareD(42)	J4 DATA(41) ShareD(41)	J5 VDDEXT_J5 VDDEXT	J6 VDDINT_J6 VDDINT	J7 GND_J7 GND	J8 GND_J8 GND	J9 GND_J9 GND	J10 GND_J10 GND	J11 GND_J11 GND	J12 GND_J12 GND	J13 GND_J13 GND	J14 GND_J14 GND	J15 VDDINT_J15 VDDINT	J16 VDDEXT_J16 VDDEXT	J17 L2DAT(2) L2DATa(2)	J18 L2DAT(0) L2DATa(0)	J19 HBG_n HBG_n	J20 HBR_n HBR_n
K1 CLK_CFG_0 GND	K2 DATA(46) ShareD(46)	K3 DATA(45) ShareD(45)	K4 DATA(47) ShareD(47)	K5 VDDEXT_K5 VDDEXT	K6 VDDINT_K6 VDDINT	K7 GND_K7 GND	K8 GND_K8 GND	K9 GND_K9 GND	K10 GND_K10 GND	K11 GND_K11 GND	K12 GND_K12 GND	K13 GND_K13 GND	K14 GND_K14 GND	K15 VDDINT_K15 VDDINT	K16 VDDEXT_K16 VDDEXT	K17 BR6_n BR6_n	K18 BR5_n BR5_n	K19 BR4_n BR4_n	K20 BR3_n BR3_n
L1 CLKIN Sharc_Clk	L2 CLK_CFG_1 VDDEXT	L3 AGND GND	L4 CLK_CFG_2 GND	L5 VDDEXT_L5 VDDEXT	L6 VDDINT_L6 VDDINT	L7 GND_L7 GND	L8 GND_L8 GND	L9 GND_L9 GND	L10 GND_L10 GND	L11 GND_L11 GND	L12 GND_L12 GND	L13 GND_L13 GND	L14 GND_L14 GND	L15 VDDINT_L15 VDDINT	L16 VDDEXT_L16 VDDEXT	L17 BR2_n BR2_n	L18 BR1_n BR1_n	L19 ACK ACK	L20 REDY Redy_a
M1 AVDD AVDDa	M2 CLK_CFG_3 GND	M3 CLKOUT	M4 NC_M4	M5 VDDEXT_M5 VDDEXT	M6 VDDINT_M6 VDDINT	M7 GND_M7 GND	M8 GND_M8 GND	M9 GND_M9 GND	M10 GND_M10 GND	M11 GND_M11 GND	M12 GND_M12 GND	M13 GND_M13 GND	M14 GND_M14 GND	M15 VDDINT_M15 VDDINT	M16 VDDEXT_M16 VDDEXT	M17 PAGE PAGE	M18 SBTS_n SBTS_n	M19 PA_n PA_n	M20 L3DAT(7) L3DATa(7)
N1 NC_N1	N2 NC_N2	N3 DATA(48) ShareD(48)	N4 DATA(51) ShareD(51)	N5 VDDEXT_N5 VDDEXT	N6 VDDINT_N6 VDDINT	N7 GND_N7 GND	N8 GND_N8 GND	N9 GND_N9 GND	N10 GND_N10 GND	N11 GND_N11 GND	N12 GND_N12 GND	N13 GND_N13 GND	N14 GND_N14 GND	N15 VDDINT_N15 VDDINT	N16 VDDEXT_N16 VDDEXT	N17 L3DAT(5) L3DATa(5)	N18 L3DAT(6) L3DATa(6)	N19 L3DAT(4) L3DATa(4)	N20 L3CLK L3CLKa
P1 DATA(49) ShareD(49)	P2 DATA(50) ShareD(50)	P3 DATA(52) ShareD(52)	P4 DATA(55) ShareD(55)	P5 VDDEXT_P5 VDDEXT	P6 VDDINT_P6 VDDINT	P7 GND_P7 GND	P8 GND_P8 GND	P9 GND_P9 GND	P10 GND_P10 GND	P11 GND_P11 GND	P12 GND_P12 GND	P13 GND_P13 GND	P14 GND_P14 GND	P15 VDDINT_P15 VDDINT	P16 VDDEXT_P16 VDDEXT	P17 L3DAT(2) L3DATa(2)	P18 L3DAT(1) L3DATa(1)	P19 L3DAT(3) L3DATa(3)	P20 L3ACK L3ACKa
R1 DATA(53) ShareD(53)	R2 DATA(54) ShareD(54)	R3 DATA(57) ShareD(57)	R4 DATA(60) ShareD(60)	R5 VDDEXT_R5 VDDEXT	R6 VDDINT_R6 VDDINT	R7 GND_R7 GND	R8 GND_R8 GND	R9 GND_R9 GND	R10 GND_R10 GND	R11 GND_R11 GND	R12 GND_R12 GND	R13 GND_R13 GND	R14 GND_R14 GND	R15 GND_R15 GND	R16 VDDEXT_R16 VDDEXT	R17 L4DAT(5) L4DATa(5)	R18 L4DAT(6) L4DATa(6)	R19 L4DAT(7) L4DATa(7)	R20 L3DAT(0) L3DATa(0)
T1 DATA(56) ShareD(56)	T2 DATA(58) ShareD(58)	T3 DATA(59) ShareD(59)	T4 DATA(63) ShareD(63)	T5 VDDEXT_T5 VDDEXT	T6 VDDINT_T6 VDDINT	T7 VDDINT_T7 VDDINT	T8 VDDINT_T8 VDDINT	T9 VDDINT_T9 VDDINT	T10 VDDINT_T10 VDDINT	T11 VDDINT_T11 VDDINT	T12 VDDINT_T12 VDDINT	T13 VDDINT_T13 VDDINT	T14 VDDINT_T14 VDDINT	T15 VDDINT_T15 VDDINT	T16 VDDEXT_T16 VDDEXT	T17 L4DAT(3) L4DATa(3)	T18 L4ACK L4ACKa	T19 L4CLK L4CLKa	T20 L4DAT(4) L4DATa(4)
U1 DATA(61) ShareD(61)	U2 DATA(62) ShareD(62)	U3 ADDR(3) SharcAdr(3)	U4 ADDR(2) SharcAdr(2)	U5 VDDEXT_U5 VDDEXT	U6 VDDEXT_U6 VDDEXT	U7 VDDEXT_U7 VDDEXT	U8 VDDEXT_U8 VDDEXT	U9 VDDEXT_U9 VDDEXT	U10 VDDEXT_U10 VDDEXT	U11 VDDEXT_U11 VDDEXT	U12 VDDEXT_U12 VDDEXT	U13 VDDEXT_U13 VDDEXT	U14 VDDEXT_U14 VDDEXT	U15 VDDEXT_U15 VDDEXT	U16 VDDEXT_U16 VDDEXT	U17 L5DAT(7) L5DATa(7)	U18 L4DAT(0) L4DATa(0)	U19 L4DAT(1) L4DATa(1)	U20 L4DAT(2) L4DATa(2)
V1 ADDR(4) SharcAdr(4)	V2 ADDR(6) SharcAdr(6)	V3 ADDR(7) SharcAdr(7)	V4 ADDR(10) SharcAdr(10)	V5 ADDR(14) SharcAdr(14)	V6 ADDR(18) SharcAdr(18)	V7 ADDR(22) SharcAdr(22)	V8 ADDR(25) SharcAdr(25)	V9 ADDR(28) SharcAdr(28)	V10 IDO VDDEXT	V11 ADDR(1) SharcAdr(1)	V12 MS1_n MS1_n	V13 CS_n CSa_n	V14 RDL_n RDL_n	V15 DMAR2_n DMAR2_n	V16 L5DAT(0) L5DATa(0)	V17 L5DAT(2) L5DATa(2)	V18 L5ACK L5ACKa	V19 L5DAT(4) L5DATa(4)	V20 L5DAT(6) L5DATa(6)
W1 ADDR(5) SharcAdr(5)	W2 ADDR(9) SharcAdr(9)	W3 ADDR(12) SharcAdr(12)	W4 ADDR(15) SharcAdr(15)	W5 ADDR(17) SharcAdr(17)	W6 ADDR(20) SharcAdr(20)	W7 ADDR(23) SharcAdr(23)	W8 ADDR(26) SharcAdr(26)	W9 ADDR(29) SharcAdr(29)	W10 ID1 GND	W11 ADDR(0) SharcAdr(0)	W12 BMS_n BMSa_n	W13 MS2_n MS2_n	W14 CIP_n CIP_n	W15 RDH_n RDH_n	W16 DMAG2_n DMAG2_n	W17 LBOOT GND	W18 L5DAT(1) L5DATa(1)	W19 L5DAT(3) L5DATa(3)	W20 L5DAT(5) L5DATa(5)
Y1 ADDR(8) SharcAdr(8)	Y2 ADDR(11) SharcAdr(11)	Y3 ADDR(13) SharcAdr(13)	Y4 ADDR(16) SharcAdr(16)	Y5 ADDR(19) SharcAdr(19)	Y6 ADDR(21) SharcAdr(21)	Y7 ADDR(24) SharcAdr(24)	Y8 ADDR(27) SharcAdr(27)	Y9 ADDR(30) SharcAdr(30)	Y10 ADDR(31) SharcAdr(31)	Y11 IID2 GND	Y12 BRST BRST	Y13 MS0_n MS0_n	Y14 MS3_n MS3_n	Y15 WRH_n WRH_n	Y16 WRL_n WRL_n	Y17 DMAG1_n DMAG1_n	Y18 DMAR1_n DMAR1_n	Y19 EBOOT GND	Y20 L5CLK L5CLKa

Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

SHARC A

ID = "001"

Booting Mode:
EBOOT = '0', LBOOT = '0', BMS_n = '1' (Input)
=> Host Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

MROD-Out		Rev V2 3
		Date 7 Feb 2006
SHARC-A		Time 1:25:29 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 2 of 19

IC502
ADSP21160N

A1 DATA(14) ShareD(14)	A2 DATA(13) ShareD(13)	A3 DATA(10) ShareD(10)	A4 DATA(8) ShareD(8)	A5 DATA(4) ShareD(4)	A6 DATA(2) ShareD(2)	A7 TDI Sharc_TDOa	A8 TRST_n Sharc_TRST_n	A9 RESET_n RstSharcAB_n	A10 RPBA RPBA	A11 IRQ0_n IRQ0b_n	A12 FLAG1 Flag1b	A13 TIMEXP	A14 NC_A14	A15 NC_A15	A16 TFS1 TFS1b	A17 RFS1 RFS1b	A18 RCLK0	A19 DT0 L0DATb(4)	A20 L0DAT(4) L0DATb(4)
B1 DATA(22) ShareD(22)	B2 DATA(16) ShareD(16)	B3 DATA(15) ShareD(15)	B4 DATA(9) ShareD(9)	B5 DATA(6) ShareD(6)	B6 DATA(3) ShareD(3)	B7 DATA(0) ShareD(0)	B8 TCK Sharc_TCK	B9 EMU_n Sharc_EMU_n	B10 IRQ2_n IRQ2b_n	B11 FLAG3 Flag3b	B12 FLAG0 Flag0b	B13 NC_B13	B14 NC_B14	B15 DT1	B16 RCLK1	B17 RFS0 RFS0b	B18 TCLK0 L0DATb(5)	B19 L0DAT(5)	B20 L0DAT(2) L0DATb(2)
C1 DATA(24) ShareD(24)	C2 DATA(18) ShareD(18)	C3 DATA(17) ShareD(17)	C4 DATA(11) ShareD(11)	C5 DATA(7) ShareD(7)	C6 DATA(5) ShareD(5)	C7 DATA(1) ShareD(1)	C8 TMS Sharc_TMS	C9 TDO Sharc_TDOb	C10 IRQ1_n IRQ1b_n	C11 FLAG2 Flag2b	C12 NC_C12	C13 NC_C13	C14 TCLK1	C15 DR1	C16 DR0 L0DATb(7)	C17 L0DAT(7) L0CLKb	C18 L0DAT(4) L0DATb(6)	C19 L0ACK L0ACKb	C20 L0DAT(0) L0DATb(0)
D1 DATA(28) ShareD(28)	D2 DATA(25) ShareD(25)	D3 DATA(20) ShareD(20)	D4 DATA(19) ShareD(19)	D5 DATA(12) ShareD(12)	D6 VDDEXT_D6 VDDEXT	D7 VDDINT_D7 VDDINT	D8 VDDEXT_D8 VDDEXT	D9 VDDEXT_D9 VDDEXT	D10 VDDEXT_D10 VDDEXT	D11 VDDEXT_D11 VDDEXT	D12 VDDEXT_D12 VDDEXT	D13 VDDINT_D13 VDDINT	D14 VDDEXT_D14 VDDEXT	D15 TFS0 TFS0b	D16 L1DAT(7) L1DATb(7)	D17 L0CLK L0CLKb	D18 L0DAT(3) L0DATb(3)	D19 L0DAT(1) L0DATb(1)	D20 L1CLK L1CLKb
E1 DATA(30) ShareD(30)	E2 DATA(29) ShareD(29)	E3 DATA(23) ShareD(23)	E4 DATA(21) ShareD(21)	E5 VDDEXT_E5 VDDEXT	E6 VDDINT_E6 VDDINT	E7 VDDINT_E7 VDDINT	E8 VDDINT_E8 VDDINT	E9 VDDINT_E9 VDDINT	E10 VDDINT_E10 VDDINT	E11 GND_E11 GND	E12 VDDINT_E12 VDDINT	E13 VDDINT_E13 VDDINT	E14 VDDINT_E14 VDDINT	E15 VDDINT_E15 VDDINT	E16 VDDEXT_E16 VDDEXT	E17 L1DAT(6) L1DATb(6)	E18 L1DAT(5) L1DATb(5)	E19 L1ACK L1ACKb	E20 L1DAT(1) L1DATb(1)
F1 DATA(34) ShareD(34)	F2 DATA(33) ShareD(33)	F3 DATA(27) ShareD(27)	F4 DATA(26) ShareD(26)	F5 VDDEXT_F5 VDDEXT	F6 VDDINT_F6 VDDINT	F7 GND_F7 GND	F8 GND_F8 GND	F9 GND_F9 GND	F10 GND_F10 GND	F11 GND_F11 GND	F12 GND_F12 GND	F13 GND_F13 GND	F14 GND_F14 GND	F15 VDDINT_F15 VDDINT	F16 VDDEXT_F16 VDDEXT	F17 L1DAT(4) L1DATb(4)	F18 L1DAT(3) L1DATb(3)	F19 L1DAT(0) L1DATb(0)	F20 L2DAT(7) L2DATb(7)
G1 DATA(38) ShareD(38)	G2 DATA(35) ShareD(35)	G3 DATA(32) ShareD(32)	G4 DATA(31) ShareD(31)	G5 VDDEXT_G5 VDDEXT	G6 VDDINT_G6 VDDINT	G7 GND_G7 GND	G8 GND_G8 GND	G9 GND_G9 GND	G10 GND_G10 GND	G11 GND_G11 GND	G12 GND_G12 GND	G13 GND_G13 GND	G14 GND_G14 GND	G15 VDDINT_G15 VDDINT	G16 VDDEXT_G16 VDDEXT	G17 L1DAT(2) L1DATb(2)	G18 L2DAT(6) L2DATb(6)	G19 L2DAT(4) L2DATb(4)	G20 L2CLK L2CLKb
H1 DATA(40) ShareD(40)	H2 DATA(39) ShareD(39)	H3 DATA(37) ShareD(37)	H4 DATA(36) ShareD(36)	H5 VDDEXT_H5 VDDEXT	H6 VDDINT_H6 VDDINT	H7 GND_H7 GND	H8 GND_H8 GND	H9 GND_H9 GND	H10 GND_H10 GND	H11 GND_H11 GND	H12 GND_H12 GND	H13 GND_H13 GND	H14 GND_H14 GND	H15 VDDINT_H15 VDDINT	H16 VDDEXT_H16 VDDEXT	H17 L2DAT(5) L2DATb(5)	H18 L2ACK L2ACKb	H19 L2DAT(3) L2DATb(3)	H20 L2DAT(1) L2DATb(1)
J1 DATA(44) ShareD(44)	J2 DATA(43) ShareD(43)	J3 DATA(42) ShareD(42)	J4 DATA(41) ShareD(41)	J5 VDDEXT_J5 VDDEXT	J6 VDDINT_J6 VDDINT	J7 GND_J7 GND	J8 GND_J8 GND	J9 GND_J9 GND	J10 GND_J10 GND	J11 GND_J11 GND	J12 GND_J12 GND	J13 GND_J13 GND	J14 GND_J14 GND	J15 VDDINT_J15 VDDINT	J16 VDDEXT_J16 VDDEXT	J17 L2DAT(2) L2DATb(2)	J18 L2DAT(0) L2DATb(0)	J19 HBG_n HBG_n	J20 HBR_n HBR_n
K1 CLK_CFG_0 GND	K2 DATA(46) ShareD(46)	K3 DATA(45) ShareD(45)	K4 DATA(47) ShareD(47)	K5 VDDEXT_K5 VDDEXT	K6 VDDINT_K6 VDDINT	K7 GND_K7 GND	K8 GND_K8 GND	K9 GND_K9 GND	K10 GND_K10 GND	K11 GND_K11 GND	K12 GND_K12 GND	K13 GND_K13 GND	K14 GND_K14 GND	K15 VDDINT_K15 VDDINT	K16 VDDEXT_K16 VDDEXT	K17 BR6_n BR6_n	K18 BR5_n BR5_n	K19 BR4_n BR4_n	K20 BR3_n BR3_n
L1 CLKIN Sharc_Clk	L2 CLK_CFG_1 VDDEXT	L3 AGND GND	L4 CLK_CFG_2 GND	L5 VDDEXT_L5 VDDEXT	L6 VDDINT_L6 VDDINT	L7 GND_L7 GND	L8 GND_L8 GND	L9 GND_L9 GND	L10 GND_L10 GND	L11 GND_L11 GND	L12 GND_L12 GND	L13 GND_L13 GND	L14 GND_L14 GND	L15 VDDINT_L15 VDDINT	L16 VDDEXT_L16 VDDEXT	L17 BR2_n BR2_n	L18 BR1_n BR1_n	L19 ACK ACK	L20 REDY Redy_b
M1 AVDD AVDDb	M2 CLK_CFG_3 GND	M3 CLKOUT	M4 NC_M4	M5 VDDEXT_M5 VDDEXT	M6 VDDINT_M6 VDDINT	M7 GND_M7 GND	M8 GND_M8 GND	M9 GND_M9 GND	M10 GND_M10 GND	M11 GND_M11 GND	M12 GND_M12 GND	M13 GND_M13 GND	M14 GND_M14 GND	M15 VDDINT_M15 VDDINT	M16 VDDEXT_M16 VDDEXT	M17 PAGE PAGE	M18 SBTS_n SBTS_n	M19 PA_n PA_n	M20 L3DAT(7) L3DATb(7)
N1 NC_N1	N2 NC_N2	N3 DATA(48) ShareD(48)	N4 DATA(51) ShareD(51)	N5 VDDEXT_N5 VDDEXT	N6 VDDINT_N6 VDDINT	N7 GND_N7 GND	N8 GND_N8 GND	N9 GND_N9 GND	N10 GND_N10 GND	N11 GND_N11 GND	N12 GND_N12 GND	N13 GND_N13 GND	N14 GND_N14 GND	N15 VDDINT_N15 VDDINT	N16 VDDEXT_N16 VDDEXT	N17 L3DAT(5) L3DATb(5)	N18 L3DAT(4) L3DATb(6)	N19 L3DAT(4) L3DATb(4)	N20 L3CLK L3CLKb
P1 DATA(49) ShareD(49)	P2 DATA(50) ShareD(50)	P3 DATA(52) ShareD(52)	P4 DATA(55) ShareD(55)	P5 VDDEXT_P5 VDDEXT	P6 VDDINT_P6 VDDINT	P7 GND_P7 GND	P8 GND_P8 GND	P9 GND_P9 GND	P10 GND_P10 GND	P11 GND_P11 GND	P12 GND_P12 GND	P13 GND_P13 GND	P14 GND_P14 GND	P15 VDDINT_P15 VDDINT	P16 VDDEXT_P16 VDDEXT	P17 L3DAT(2) L3DATb(2)	P18 L3DAT(1) L3DATb(1)	P19 L3DAT(3) L3DATb(3)	P20 L3ACK L3ACKb
R1 DATA(53) ShareD(53)	R2 DATA(54) ShareD(54)	R3 DATA(57) ShareD(57)	R4 DATA(60) ShareD(60)	R5 VDDEXT_R5 VDDEXT	R6 VDDINT_R6 VDDINT	R7 GND_R7 GND	R8 GND_R8 GND	R9 GND_R9 GND	R10 GND_R10 GND	R11 GND_R11 GND	R12 GND_R12 GND	R13 GND_R13 GND	R14 GND_R14 GND	R15 GND_R15 GND	R16 VDDEXT_R16 VDDEXT	R17 L4DAT(5) L4DATb(5)	R18 L4DAT(6) L4DATb(6)	R19 L4DAT(7) L4DATb(7)	R20 L3DAT(0) L3DATb(0)
T1 DATA(56) ShareD(56)	T2 DATA(58) ShareD(58)	T3 DATA(59) ShareD(59)	T4 DATA(63) ShareD(63)	T5 VDDEXT_T5 VDDEXT	T6 VDDINT_T6 VDDINT	T7 VDDINT_T7 VDDINT	T8 VDDINT_T8 VDDINT	T9 VDDINT_T9 VDDINT	T10 VDDINT_T10 VDDINT	T11 VDDINT_T11 VDDINT	T12 VDDINT_T12 VDDINT	T13 VDDINT_T13 VDDINT	T14 VDDINT_T14 VDDINT	T15 VDDINT_T15 VDDINT	T16 VDDEXT_T16 VDDEXT	T17 L4DAT(3) L4DATb(3)	T18 L4ACK L4ACKb	T19 L4CLK L4CLKb	T20 L4DAT(4) L4DATb(4)
U1 DATA(61) ShareD(61)	U2 DATA(62) ShareD(62)	U3 ADDR(3) SharcAdr(3)	U4 ADDR(2) SharcAdr(2)	U5 VDDEXT_U5 VDDEXT	U6 VDDEXT_U6 VDDEXT	U7 VDDEXT_U7 VDDEXT	U8 VDDEXT_U8 VDDEXT	U9 VDDEXT_U9 VDDEXT	U10 VDDEXT_U10 VDDEXT	U11 VDDEXT_U11 VDDEXT	U12 VDDEXT_U12 VDDEXT	U13 VDDEXT_U13 VDDEXT	U14 VDDEXT_U14 VDDEXT	U15 VDDEXT_U15 VDDEXT	U16 VDDEXT_U16 VDDEXT	U17 L5DAT(7) L5DATb(7)	U18 L4DAT(0) L4DATb(0)	U19 L4DAT(1) L4DATb(1)	U20 L4DAT(2) L4DATb(2)
V1 ADDR(4) SharcAdr(4)	V2 ADDR(6) SharcAdr(6)	V3 ADDR(7) SharcAdr(7)	V4 ADDR(10) SharcAdr(10)	V5 ADDR(14) SharcAdr(14)	V6 ADDR(18) SharcAdr(18)	V7 ADDR(22) SharcAdr(22)	V8 ADDR(25) SharcAdr(25)	V9 ADDR(28) SharcAdr(28)	V10 IDO GND	V11 ADDR(1) SharcAdr(1)	V12 MS1_n MS1_n	V13 CS_n CSb_n	V14 RDL_n RDL_n	V15 DMAR2_n DMAR2_n	V16 L5DAT(0) L5DATb(0)	V17 L5DAT(2) L5DATb(2)	V18 L5ACK L5ACKb	V19 L5DAT(4) L5DATb(4)	V20 L5DAT(6) L5DATb(6)
W1 ADDR(5) SharcAdr(5)	W2 ADDR(9) SharcAdr(9)	W3 ADDR(12) SharcAdr(12)	W4 ADDR(15) SharcAdr(15)	W5 ADDR(17) SharcAdr(17)	W6 ADDR(20) SharcAdr(20)	W7 ADDR(23) SharcAdr(23)	W8 ADDR(26) SharcAdr(26)	W9 ADDR(29) SharcAdr(29)	W10 ID1 VDDEXT	W11 ADDR(0) SharcAdr(0)	W12 BMS_n BMSb_n	W13 MS2_n MS2_n	W14 CIP_n CIP_n	W15 RDH_n RDH_n	W16 DMAG2_n DMAG2_n	W17 LBOOT GND	W18 L5DAT(1) L5DATb(1)	W19 L5DAT(3) L5DATb(3)	W20 L5DAT(5) L5DATb(5)
Y1 ADDR(8) SharcAdr(8)	Y2 ADDR(11) SharcAdr(11)	Y3 ADDR(13) SharcAdr(13)	Y4 ADDR(16) SharcAdr(16)	Y5 ADDR(19) SharcAdr(19)	Y6 ADDR(21) SharcAdr(21)	Y7 ADDR(24) SharcAdr(24)	Y8 ADDR(27) SharcAdr(27)	Y9 ADDR(30) SharcAdr(30)	Y10 ADDR(31) SharcAdr(31)	Y11 ID2 GND	Y12 BRST BRST	Y13 MS0_n MS0_n	Y14 MS3_n MS3_n	Y15 WRH_n WRH_n	Y16 WRL_n WRL_n	Y17 DMAG1_n DMAG1_n	Y18 DMAR1_n DMAR1_n	Y19 EBOOT GND	Y20 L5CLK L5CLKb

Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

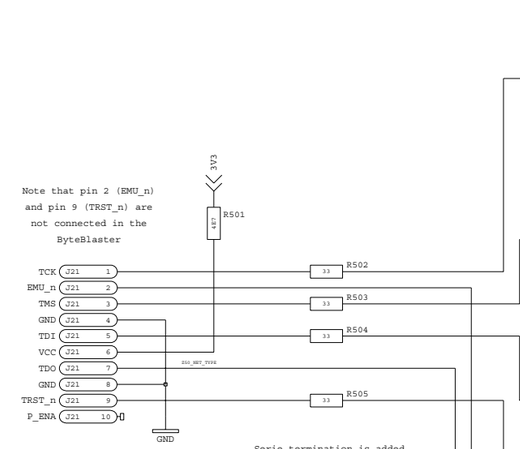
SHARC B

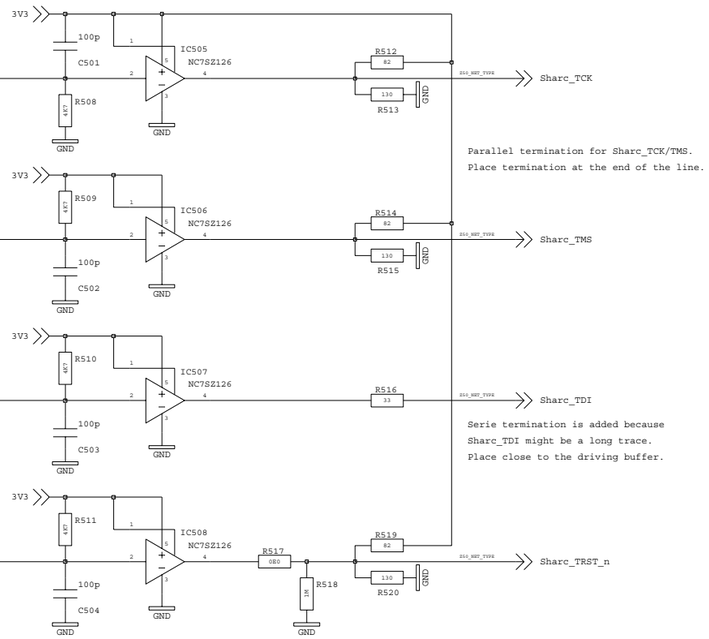
ID = "010"

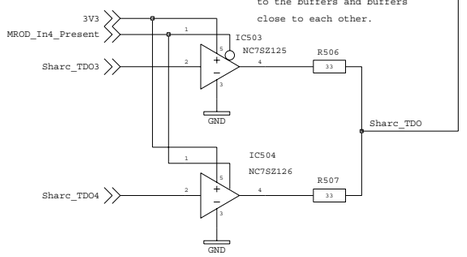
Booting Mode:
EBOOT = '0', LBOOT = '0', BMS_n = '1' (Input)
=> Host Port Booting

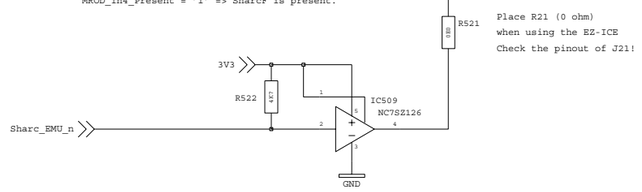
SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

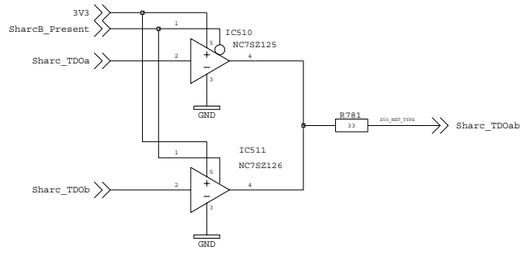
MROD-Out	Rev V2 3
	Date 7 Feb 2006
SHARC-B	Time 1:25:46 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	
	Size A3 / 4 1 4 A
NIKHEF	Dim 420 x 297 mm
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA, KRUISLAAN 409, 020-592 2000, 1098 SJ AMSTERDAM NEDERLAND	Page 3 of 19
© ET-Nikhef Amsterdam	

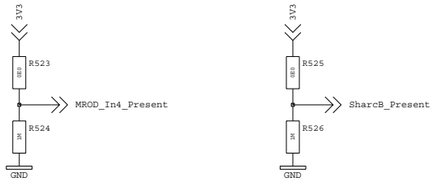




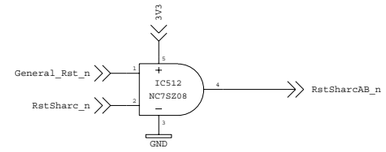


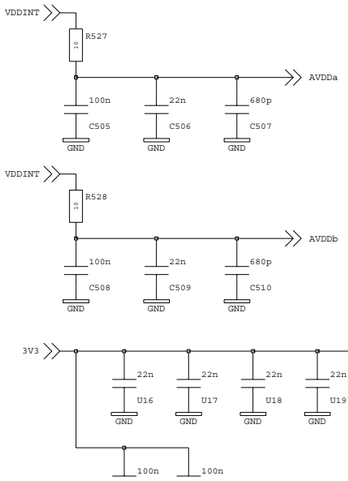


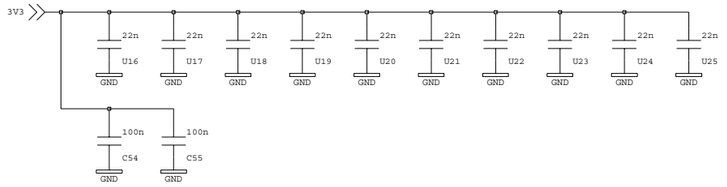




Both Sharcs are reset when there is
a General_Rst_n, or when a reset is
asked via the bit Set/Clr register
in VME64x CSR space.

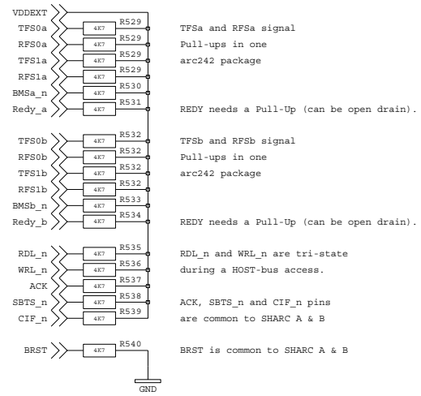






Fiducial501 Fiducial502

Fiducial503 Fiducial504



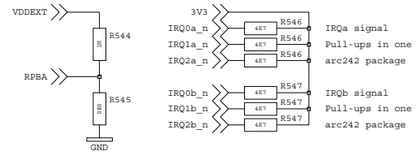
BR_n pins are common to SHARC A & B
Unused BR_n lines need Pull_Up (see datasheet)
Note that BR2_n and BR1_n pull-ups can be installed
when only SHARC A is mounted on the board.

PAGE and PA_n are common to SHARC A & B
No need for Pull-Ups.

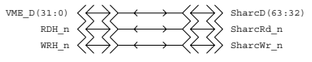
MS0_n .. MS3_n, RDH_n, RDL_n, WRH_n and WRL_n
are common to SHARC A & B and have internal Pull-Ups

HBR_n and HBG_n are common to SHARC A & B
No need for Pull-Ups.
HBR_n is always driven by the FPGA.
HBG_n is always driven by the Bus Master

DMAR1_n and DMAR2_n are common to SHARC A & B
No need for Pull-Ups.
The are always driven by the FPGA.
DMAG1_n and DMAG2_n are common to SHARC A & B
No need for Pull-Ups, they are driven by the Bus Master.

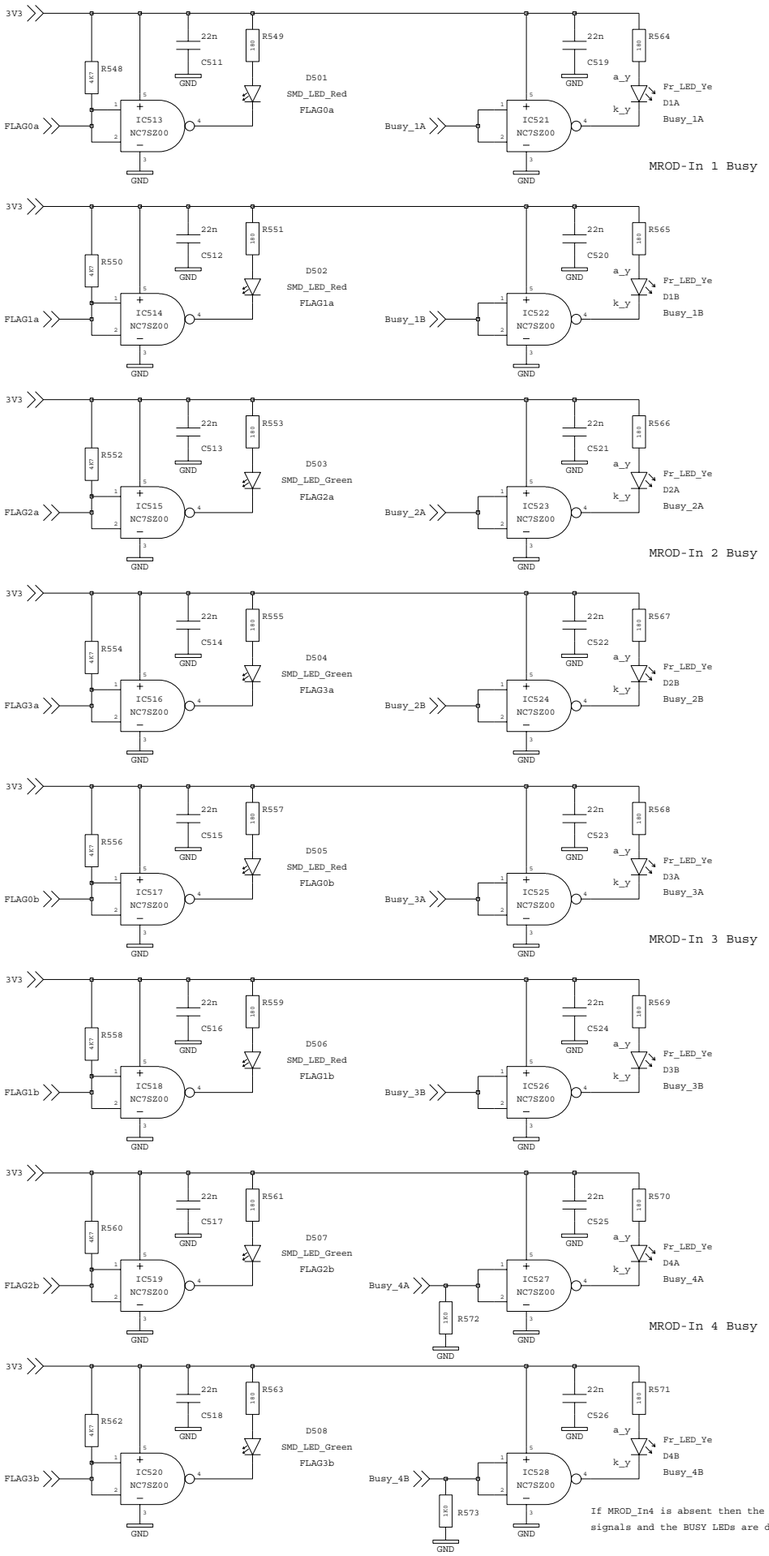


Rotating Priority Bus Arbitration
select is set to "Fixed Priority"
by default (SHARC A has priority).

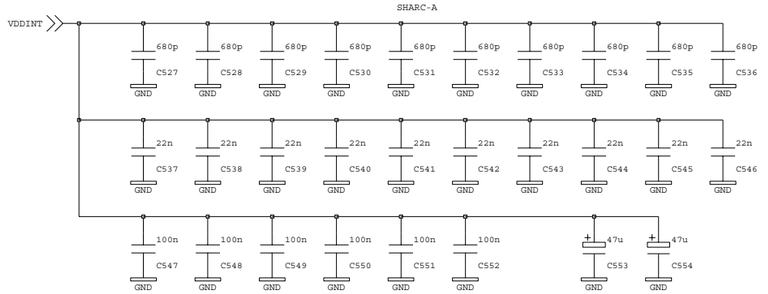


MROD-Out	Rev V2 3
	Date 7 Feb 2006
SHARC JTAG and Auxiliary connections	Time 1:26:10 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	
NIKHEF	Size A3 / 4 1 4 A
© ET-Nikhef Amsterdam	Dim 420 x 297 mm
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Page 4 of 19

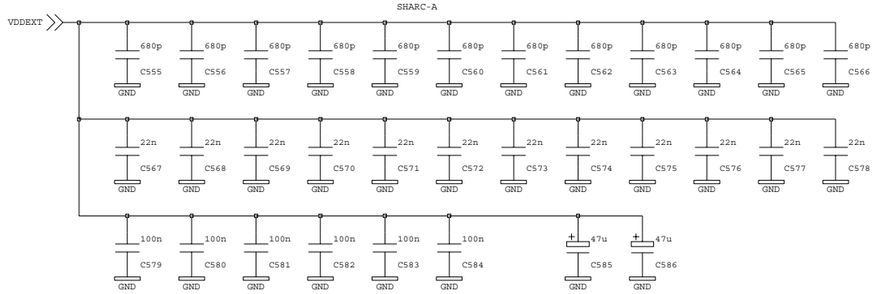
Sharc Flag pin is an Input by default after Power-Up.
This means the LEDs light up during and after Power-Up.



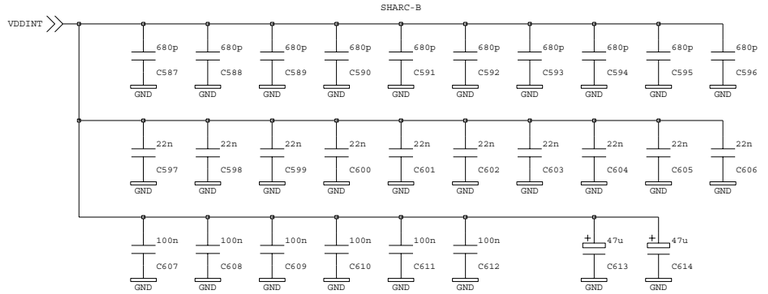
ADSP21160 VDDINT (40 pins) Decoupling Capacitors
SHARC-A



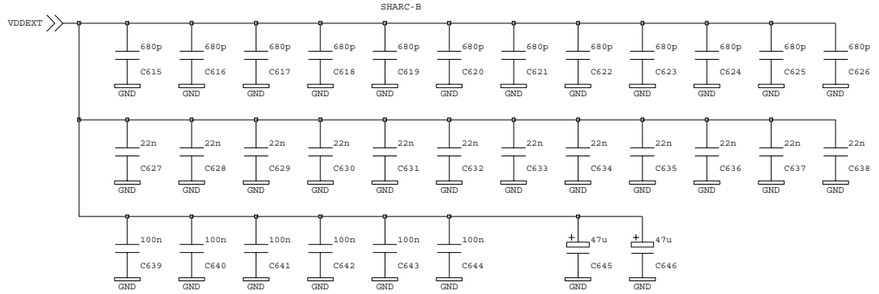
ADSP21160 VDDEXT (43 pins) Decoupling Capacitors
SHARC-A



ADSP21160 VDDINT (40 pins) Decoupling Capacitors
SHARC-B



ADSP21160 VDDEXT (43 pins) Decoupling Capacitors
SHARC-B



MROD-Out

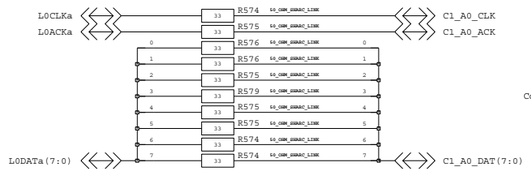
SHARC Power Supply Decoupling and LEDs

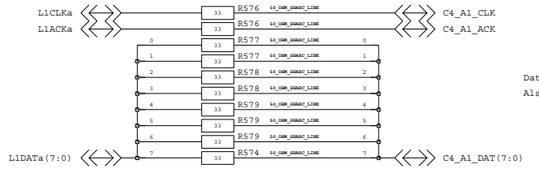
Proj: MROD-X	Proj.No: 38405
Peter Jansweijer	peterj@nikhef.nl

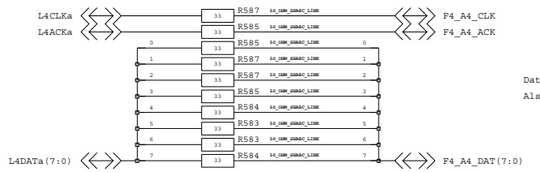
NIKHEF

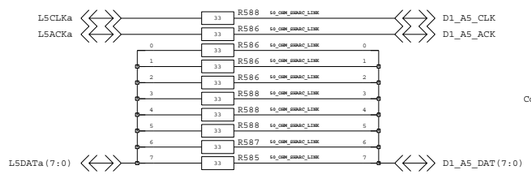
NATIONAAL INSTITUUT VOOR KERN-
FYSICA EN HOGE ENERGIE-FYSICA
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND

Rev	V2 3
Date	7 Feb 2006
Time	1:26:41 pm
Name	tonvr
Size	A3 4 1 4 A
Dim	420 x 297 mm
Page	5 of 19

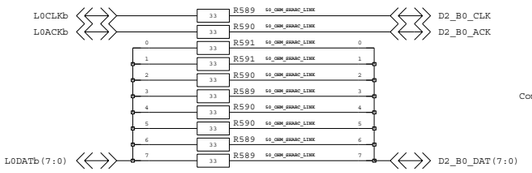


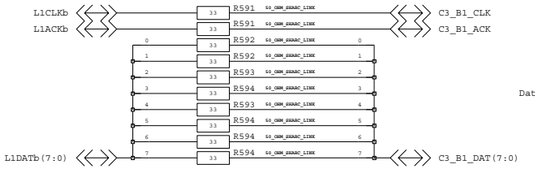


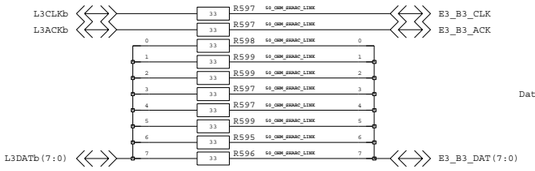


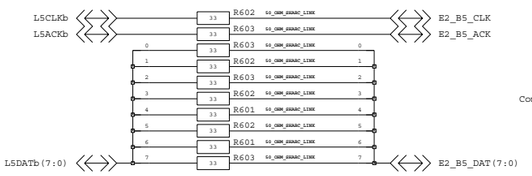


SHARC A Link Serie Termination









SHARC B Link Serie Termination

MROD-Out		Rev V2 3
		Date 7 Feb 2006
Sharc AB Link termination		Time 1:26:56 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 6 of 19

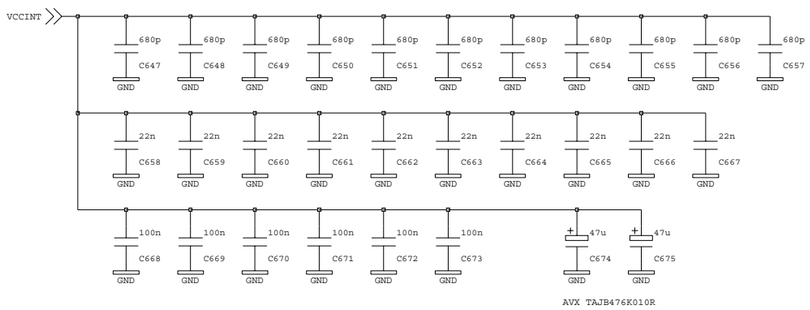
IC529
XC2VP20FF896

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A		A2 VCCAUX	A3 VRP_2	A4 RXN_2A	A5 RXP_2A	A6 TXP_2A	A7 TXN_2A	A8 Busy_2A	A9 GND	A10	A11 RXN_2B	A12 RXP_2B	A13 TXP_2B	A14 TXN_2B	A15 VCCAUX	A16 VCCAUX	A17 RXN_1A	A18 RXP_1A	A19 TXP_1A	A20 TXN_1A	A21	A22 GND	A23 Busy_1B	A24 RXN_1B	A25 RXP_1B	A26 TXP_1B	A27 TXN_1B	A28 VRP_7	A29 VCCAUX	
B	B1 VCCAUX	B2 GND	B3 VRN_2	B4 AVCCAUXRX9	B5 VTRXPAD9	B6 AVCCAUXTX9	B7 VTTXPAD9	B8 LocalBAR(0)	B9	B10	B11 AVCCAUXRX7	B12 VTRXPAD7	B13 AVCCAUXTX7	B14 VTTXPAD7	B15 Rst_n	B16 Rocket_XC1k	B17 AVCCAUXRX6	B18 VTRXPAD6	B19 AVCCAUXTX6	B20 VTTXPAD6	B21	B22	B23 VME_D(8)	B24 AVCCAUXRX4	B25 VTRXPAD4	B26 AVCCAUXTX4	B27 VTTXPAD4	B28 VRN_7	B29 GND	B30 VCCAUX
C	C1 Module_En	C2 SYSFAIL_En	C3 GND	C4 LEDs(0)	C5 LEDs(1)	C6 GNDA9	C7	C8 LocalBAR(1)	C9	C10	C11	C12 GNDA7	C13 Busy_2B	C14 GND	C15	C16	C17 GND	C18 Busy_1A	C19 GNDA6	C20	C21	C22	C23 VME_D(9)	C24 VME_D(0)	C25 GNDA4	C26 Spare_1A(3)	C27 Spare_1A(2)	C28 GND	C29 Spare_1A(1)	C30 Spare_1A(0)
D	D1	D2	D3 LEDs(2)	D4 GND	D5 LEDs(3)	D6	D7	D8 LocalBAR(2)	D9 GND	D10 IRQ0a_n	D11 IRQ1a_n	D12 GND	D13 IRQ2a_n	D14 CSa_n	D15 FLAG0a	D16 VME_D(4)	D17 VME_D(12)	D18 VME_D(3)	D19 GND	D20 VME_D(11)	D21 VME_D(2)	D22 GND	D23 VME_D(10)	D24 VME_D(1)	D25 DXN	D26	D27 GND	D28 Spare_1A(4)	D29	D30
E	E1	E2	E3	E4	E5 GND	E6 VRN_1	E7 VRP_1	E8 LocalBAR(3)	E9 Spare_2A(0)	E10 Spare_2B(4)	E11 Spare_2B(1)	E12	E13	E14 Redy_a	E15 FLAG1a	E16 VME_D(7)	E17 VME_D(15)	E18	E19	E20 VME_D(6)	E21 VME_D(14)	E22 VME_D(5)	E23 VME_D(13)	E24 VRN_0	E25 VRP_0	E26 GND	E27	E28	E29	E30
F	F1	F2	F3	F4	F5 TDO	F6 GND	F7	F8 LocalBAR(4)	F9 Spare_2A(1)	F10	F11	F12	F13 GND	F14	F15 SharcRd_n	F16	F17	F18 GND	F19	F20	F21 LWORD_n	F22 DS0_n	F23 DS1_n	F24 BERR_n	F25 GND	F26 TDI	F27	F28	F29	F30
G	G1	G2	G3	G4	G5 ASP_Con_n	G6 DS2401	G7 TCK	G8 Spare_2A(4)	G9 Spare_2A(2)	G10	G11 Spare_2B(2)	G12 RstSharcD_n	G13	G14	G15 SharcWr_n	G16 AS_n	G17 SMBData	G18 T_Alert_n	G19 RstSharcC_n	G20 AM10_Rst_n	G21 DTACK_OE_n	G22 DTACK_n	G23 WRITE_n	G24 PROG_B	G25	G26	G27	G28	G29	G30
H	H1 GND	H2 Spare_3B(0)	H3	H4	H5	H6	H7 VBATT	H8 TMS	H9 Spare_2A(3)	H10	H11 Spare_2B(3)	H12 Spare_2B(0)	H13	H14	H15 FLAG2a	H16 SWDEN_n	H17	H18 SMBClk	H19 LEAB_n	H20 DENO_n	H21 DENIN1_n	H22 DENIN0_n	H23 HSWAP_EN	H24 DXP	H25	H26	H27	H28	H29	H30 GND
I	I1	I2	J3 Spare_3B(4)	J4 Spare_3B(3)	J5	J6	J7 Spare_3B(2)	J8 Spare_3B(1)	J9 VCCO_2	J10 VCCO_1	J11 VCCO_1	J12 VCCO_1	J13 VCCO_1	J14	J15 FLAG3a	J16 R_W_n	J17	J18 VCCO_0	J19 VCCO_0	J20 VCCO_0	J21 VCCO_0	J22 VCCO_7	J23 Spare_1B(1)	J24 Spare_1B(2)	J25	J26	J27 Spare_1B(3)	J28 Spare_1B(4)	J29	J30
J	K1 Spare_3A(3)	K2 Spare_3A(2)	K3 Spare_3A(1)	K4 Spare_3A(0)	K5	K6	K7	K8	K9 VCCO_2	K10 VCCO_1	K11 VCCO_1	K12 VCCO_1	K13 VCCO_1	K14 VCCO_1	K15 VCCO_1	K16 VCCO_0	K17 VCCO_0	K18 VCCO_0	K19 VCCO_0	K20 VCCO_0	K21 VCCO_0	K22 VCCO_7	K23 IACKIN_n	K24 GA_n(4)	K25 GA_n(3)	K26 GA_n(2)	K27 GA_n(1)	K28 GA_n(0)	K29 GAP_n	K30 Spare_1B(0)
K	L1 HBR_n	L2 HBG_n	L3 GND	L4	L5 Spare_3A(4)	L6 GND	L7	L8	L9 VCCO_2	L10 VCCO_2	L11 GND	L12 VCCINT	L13 VCCINT	L14 VCCINT	L15 VCCINT	L16 VCCINT	L17 VCCINT	L18 VCCINT	L19 VCCINT	L20 GND	L21 VCCO_7	L22 VCCO_7	L23 AM(2)	L24 AM(3)	L25 GND	L26 AM(4)	L27 AM(5)	L28 GND	L29 IACKOUT_n	L30 IACK_n
L	M1 Ack	M2 MS0_n	M3 MS1_n	M4 MS2_n	M5 MS3_n	M6 DMAR1_n	M7 DMAR2_n	M8	M9 VCCO_2	M10 VCCO_2	M11 VCCINT	M12 GND	M13 GND	M14 GND	M15 GND	M16 GND	M17 GND	M18 GND	M19 GND	M20 VCCINT	M21 VCCO_7	M22 VCCO_7	M23 VME_IRQ_n(2)	M24 VME_IRQ_n(3)	M25 VME_IRQ_n(4)	M26 VME_IRQ_n(5)	M27 VME_IRQ_n(6)	M28 VME_IRQ_n(7)	M29 AM(0)	M30 AM(1)
M	N1 RstSharc_n	N2 SharcAdr(0)	N3 SharcAdr(1)	N4 SharcAdr(2)	N5 SharcAdr(3)	N6 SharcAdr(4)	N7 SharcAdr(5)	N8	N9 VCCO_2	N10 VCCO_2	N11 VCCINT	N12 GND	N13 GND	N14 GND	N15 GND	N16 GND	N17 GND	N18 GND	N19 GND	N20 VCCINT	N21 VCCO_7	N22 VCCO_7	N23 VME_A(17)	N24 VME_A(18)	N25 VME_A(19)	N26 VME_A(20)	N27 VME_A(21)	N28 VME_A(22)	N29 VME_A(23)	N30 VME_IRQ_n(1)
N	P1 SharcAdr(6)	P2 SharcAdr(7)	P3 SharcAdr(8)	P4 SharcAdr(9)	P5 SharcAdr(10)	P6 GND	P7 SharcAdr(11)	P8 SharcAdr(12)	P9 SharcAdr(13)	P10 VCCO_2	P11 VCCINT	P12 GND	P13 GND	P14 GND	P15 GND	P16 GND	P17 GND	P18 GND	P19 GND	P20 VCCINT	P21 VCCO_7	P22 VME_A(5)	P23 VME_A(12)	P24 VME_A(6)	P25 GND	P26 VME_A(13)	P27 VME_A(7)	P28 VME_A(14)	P29 VME_A(15)	P30 VME_A(16)
P	R1 VCCAUX	R2 SharcAdr(14)	R3 SharcAdr(15)	R4 SharcAdr(16)	R5 SharcAdr(17)	R6 SharcAdr(18)	R7 SharcAdr(19)	R8 SharcAdr(20)	R9 SharcAdr(21)	R10 VCCO_2	R11 VCCINT	R12 GND	R13 GND	R14 GND	R15 GND	R16 GND	R17 GND	R18 GND	R19 GND	R20 VCCINT	R21 VCCO_7	R22 VME_A(1)	R23 VME_A(8)	R24 VME_A(2)	R25 VME_A(9)	R26 VME_A(3)	R27 VME_A(10)	R28 VME_A(4)	R29 VME_A(11)	R30 VCCAUX
R	T1 VCCAUX	T2 SharcAdr(22)	T3 LRL(3)	T4 LRL(2)	T5 LRL(1)	T6 LRL(0)	T7 LDOWN_n	T8 LFP_n	T9 UWEN_n	T10 VCCO_3	T11 VCCINT	T12 GND	T13 GND	T14 GND	T15 GND	T16 GND	T17 GND	T18 GND	T19 GND	T20 VCCINT	T21 VCCO_6	T22 VME_A(31)	T23 VME_A(30)	T24 VME_A(29)	T25 VME_A(28)	T26 VME_A(27)	T27 VME_A(26)	T28 VME_A(25)	T29 VME_A(24)	T30 VCCAUX
T	U1 URESET_n	U2 UTRST_n	U3 UCTRL_n	U4 UD(31)	U5 UD(30)	U6 GND	U7 UD(29)	U8 UD(28)	U9 UD(27)	U10 VCCO_3	U11 VCCINT	U12 GND	U13 GND	U14 GND	U15 GND	U16 GND	U17 GND	U18 GND	U19 GND	U20 VCCINT	U21 VCCO_6	U22 VME_D(23)	U23 VME_D(22)	U24 VME_D(21)	U25 GND	U26 VME_D(20)	U27 VME_D(19)	U28 VME_D(18)	U29 VME_D(17)	U30 VME_D(16)
U	V1 UD(26)	V2 UD(25)	V3 UD(24)	V4 UD(23)	V5 UD(22)	V6 UD(21)	V7 UD(20)	V8 UD(19)	V9 VCCO_3	V10 VCCO_3	V11 VCCINT	V12 GND	V13 GND	V14 GND	V15 GND	V16 GND	V17 GND	V18 GND	V19 GND	V20 VCCINT	V21 VCCO_6	V22 VCCO_6	V23 SDRAM_DQ(3)	V24 SDRAM_DQ(2)	V25 SDRAM_DQ(1)	V26 SDRAM_DQ(0)	V27 VME_D(27)	V28 VME_D(26)	V29 VME_D(25)	V30 VME_D(24)
V	W1 UD(18)	W2 UD(17)	W3 UD(16)	W4 UD(15)	W5 UD(14)	W6 UD(13)	W7 UD(12)	W8 UD(11)	W9 VCCO_3	W10 VCCO_3	W11 VCCINT	W12 GND	W13 GND	W14 GND	W15 GND	W16 GND	W17 GND	W18 GND	W19 GND	W20 VCCINT	W21 VCCO_6	W22 VCCO_6	W23 SDRAM_DQ(7)	W24 SDRAM_DQ(6)	W25 SDRAM_DQ(5)	W26 SDRAM_DQ(4)	W27 VME_D(31)	W28 VME_D(30)	W29 VME_D(29)	W30 VME_D(28)
W	Y1 UD(10)	Y2 UD(9)	Y3 GND	Y4 UD(8)	Y5 UD(7)	Y6 GND	Y7	Y8	Y9 VCCO_3	Y10 VCCO_3	Y11 GND	Y12 VCCINT	Y13 VCCINT	Y14 VCCINT	Y15 VCCINT	Y16 VCCINT	Y17 VCCINT	Y18 VCCINT	Y19 VCCINT	Y20 GND	Y21 VCCO_6	Y22 VCCO_6	Y23 SDRAM_A(11)	Y24 SDRAM_CS_n	Y25 GND	Y26 SDRAM_RAS_n	Y27 SDRAM_CAS_n	Y28 GND	Y29 SDRAM_WE_n	Y30 SDRAM_DQM(0)
Y	AA1 UD(6)	AA2 UD(5)	AA3 UD(4)	AA4 UD(3)	AA5 UD(2)	AA6 UD(1)	AA7	AA8	AA9 VCCO_3	AA10 VCCO_4	AA11 VCCO_4	AA12 VCCO_4	AA13 VCCO_4	AA14 VCCO_4	AA15 VCCO_4	AA16 VCCO_5	AA17 VCCO_5	AA18 VCCO_5	AA19 VCCO_5	AA20 VCCO_5	AA21 VCCO_5	AA22 VCCO_6	AA23 SDRAM_DQ(16)	AA24 SDRAM_DQM(2)	AA25 SDRAM_A(2)	AA26 SDRAM_A(1)	AA27 SDRAM_A(0)	AA28 SDRAM_A(10)	AA29 SDRAM_BA(1)	AA30 SDRAM_BA(0)
AA	AB1 Spare_4B(2)	AB2 Spare_4B(1)	AB3 Spare_4B(0)	AB4 UD(0)	AB5	AB6	AB7	AB8	AB9 VCCO_3	AB10 VCCO_4	AB11 VCCO_4	AB12 VCCO_4	AB13 VCCO_4	AB14	AB15 FLAG3b	AB16 TestCon(11)	AB17 TestCon(12)	AB18 VCCO_5	AB19 VCCO_5	AB20 VCCO_5	AB21 VCCO_5	AB22 VCCO_6	AB23 SDRAM_DQ(24)	AB24 SDRAM_DQ(23)	AB25 SDRAM_DQ(22)	AB26 SDRAM_DQ(21)	AB27 SDRAM_DQ(20)	AB28 SDRAM_DQ(19)	AB29 SDRAM_DQ(18)	AB30 SDRAM_DQ(17)
AB	AC1 GND	AC2 Spare_4B(3)	AC3 Spare_4B(4)	AC4	AC5	AC6	AC7 CCLK	AC8 DONE	AC9 D0	AC10 Spare_4A(3)	AC11 Spare_4A(1)	AC12 Spare_4A(0)	AC13	AC14	AC15 FLAG2b	AC16 TestCon(10)	AC17 TestCon(13)	AC18 TestCon(14)	AC19 TestCon(4)	AC20 TestCon(3)	AC21 TestCon(1)	AC22 D7	AC23 M2	AC24 M1	AC25 SDRAM_DQ(29)	AC26 SDRAM_DQ(28)	AC27 SDRAM_DQ(27)	AC28 SDRAM_DQ(26)	AC29 SDRAM_DQ(25)	AC30 GND
AC	AD1	AD2	AD3	AD4	AD5	AD6	AD7 PWRDWN_B	AD8	AD9 D1	AD10 Spare_4A(4)	AD11 Spare_4A(2)	AD12 RstSharcE_n	AD13	AD14	AD15 FLAG1b	AD16 TestCon(9)	AD17 TestCon(7)	AD18 TestCon(15)	AD19 RstSharcF_n	AD20 TestCon(2)	AD21 TestCon(0)	AD22 D6	AD23	AD24 M0	AD25 SDRAM_A(5)	AD26 SDRAM_A(4)	AD27 SDRAM_A(3)	AD28 SDRAM_DQM(3)	AD29 SDRAM_DQ(31)	AD30 SDRAM_DQ(30)
AD	AE1	AE2	AE3	AE4	AE5	AE6 GND	AE7	AE8	AE9	AE10	AE11	AE12	AE13 GND	AE14 Redy_b	AE15 FLAG0b	AE16 TestCon(8)	AE17 TestCon(6)	AE18 GND	AE19	AE20	AE21 TTC_n(7)	AE22 ROD_Busy	AE23	AE24	AE25 GND	AE26 SDRAM_CKE	AE27 SDRAM_A(9)	AE28 SDRAM_A(8)	AE29 SDRAM_A(7)	AE30 SDRAM_A(6)
AE	AF1	AF2	AF3	AF4	AF5 GND	AF6	AF7 INIT_B	AF8 IRQ2b_n	AF9 IRQ1b_n	AF10	AF11	AF12	AF13	AF14 CSb_n	AF15 SDRAM_CLKin	AF16 SDRAM_CLK	AF17 TestCon(5)	AF18	AF19	AF20	AF21 TTC_n(6)	AF22 TTC_n(5)	AF23 TTC_n(4)	AF24 RDWR_B	AF25 SDRAM_DQ(10)	AF26 GND	AF27 SDRAM_DQ(9)	AF28 SDRAM_DQ(8)	AF29 SDRAM_DQM(1)	AF30 SDRAM_A(12)
AF	AG1	AG2	AG3	AG4 GND	AG5	AG6 DOUT	AG7 D2	AG8 VRP_4	AG9 GND	AG10 IRQ0b_n	AG11	AG12 GND	AG13	AG14 Busy_3A	AG15 SLINK_CLK	AG16 LHC_Clk	AG17 Busy_4B	AG18	AG19 GND	AG20	AG21 TTC_n(2)	AG22 GND	AG23 VRN_5	AG24 D5	AG25 CS_B	AG26 SDRAM_DQ(12)	AG27 GND	AG28 SDRAM_DQ(11)	AG29 SDRAM_DQ(14)	AG30 SDRAM_DQ(13)
AG	AH1	AH2	AH3 GND	AH4	AH5	AH6 GNDA16	AH7 D3	AH8 VRN_4	AH9	AH10	AH11	AH12 GNDA18	AH13	AH14 GND	AH15 SLINK_CLKin	AH16 C1kx2	AH17 GND	AH18	AH19 GNDA19	AH20	AH21	AH22 TTC_n(3)	AH23 VRP_5	AH24 D4	AH25 GNDA21	AH26	AH27	AH28 GND	AH29	AH30 SDRAM_DQ(15)
AH	AJ1 VCCAUX	AJ2 GND	AJ3 VRP_3	AJ4 AVCCAUXRX16	AJ5 VTRXPAD16	AJ6 AVCCAUXTX16	AJ7 VTTXPAD16	AJ8	AJ9	AJ10	AJ11 AVCCAUXRX18	AJ12 VTRXPAD18	AJ13 AVCCAUXTX18	AJ14 VTTXPAD18	AJ15	AJ16 C1k	AJ17 AVCCAUXRX19	AJ18 VTRXPAD19	AJ19 AVCCAUXTX19	AJ20 VTTXPAD19	AJ21	AJ22 TTC_n(1)	AJ23 TTC_n(0)	AJ24 AVCCAUXRX21	AJ25 VTRXPAD21	AJ26 AVCCAUXTX21	AJ27 VTTXPAD21	AJ28 VRP_6	AJ29 GND	AJ30 VCCAUX
AJ		AK2 VCCAUX	AK3 VRN_3	AK4 RXN_3B	AK5 RXP_3B	AK6 TXP_3B	AK7 TXN_3B	AK8 Busy_3B	AK9 GND	AK10	AK11 RXN_3A	AK12 RXP_3A	AK13 TXP_3A	AK14 TXN_3A	AK15 VCCAUX	AK16 VCCAUX	AK17 RXN_4B	AK18 RXP_4B	AK19 TXP_4B	AK20 TXN_4B	AK21	AK22 GND	AK23 Busy_4A	AK24 RXN_4A	AK25 RXP_4A	AK26 TXP_4A	AK27 TXN_4A	AK28 VRN_6	AK29 VCCAUX	

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

MROD-Out		Rev V2 4
		Date 7 Feb 2006
Output FPGA		Time 1:27:21 pm
Proj: MROD-X	Proj.No: 38405	Name tonvr
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 7 of 19

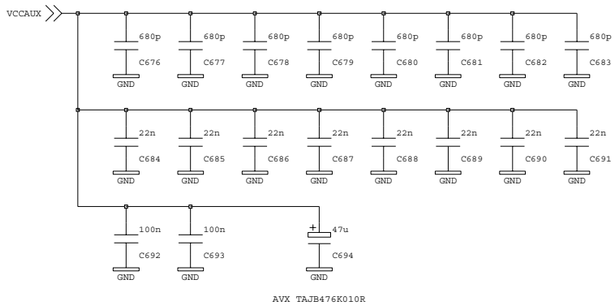
XC2VP20 VCCINT Decoupling Capacitors
Min. Power-On Current XC2VP20
IccINT = 600 mA



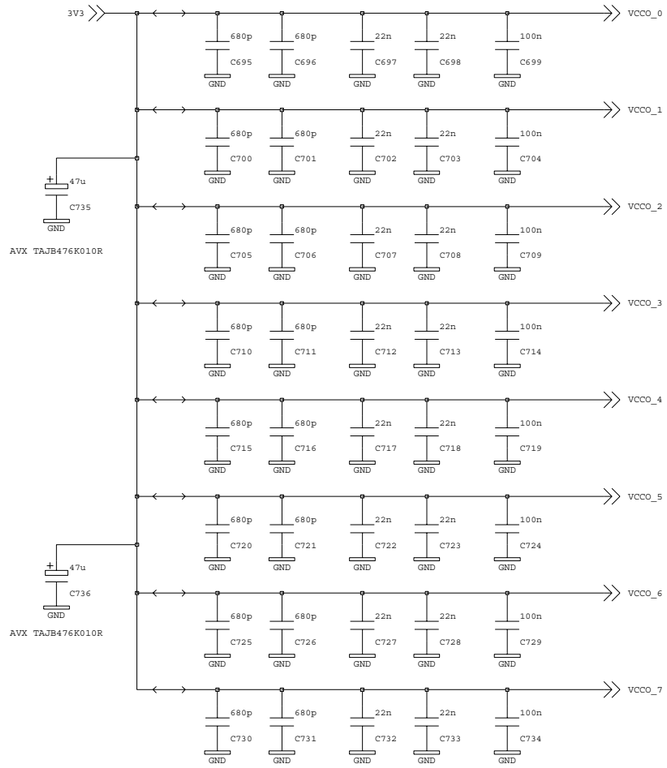
AVX TAJB476K010R

Power Inputs
For Xilinx Virtex-II Pro, power supplies
can be turned on in any sequence.
VCCINT Ramp rate 200 us min. and 50 ms max.
VCCAUX and VCCO can ramp up at any rate

XC2VP20 VCCAUX Decoupling Capacitors
Min. Power-On Current XC2VP20
IccAUX = 250 mA (min)



AVX TAJB476K010R



AVX TAJB476K010R

MROD-Out		Rev V2 3	
Output FPGA Power Supply Decoupling		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:27:36 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
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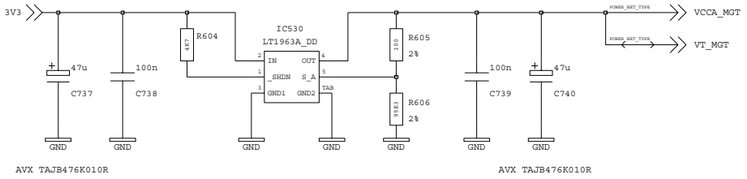
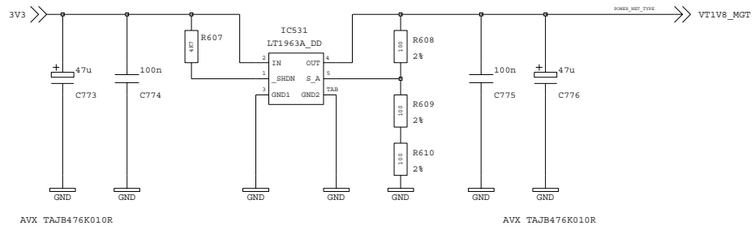
2V5 @ 1,5A



=> MGT Power (estimated 21 + 44 = 65 mA)

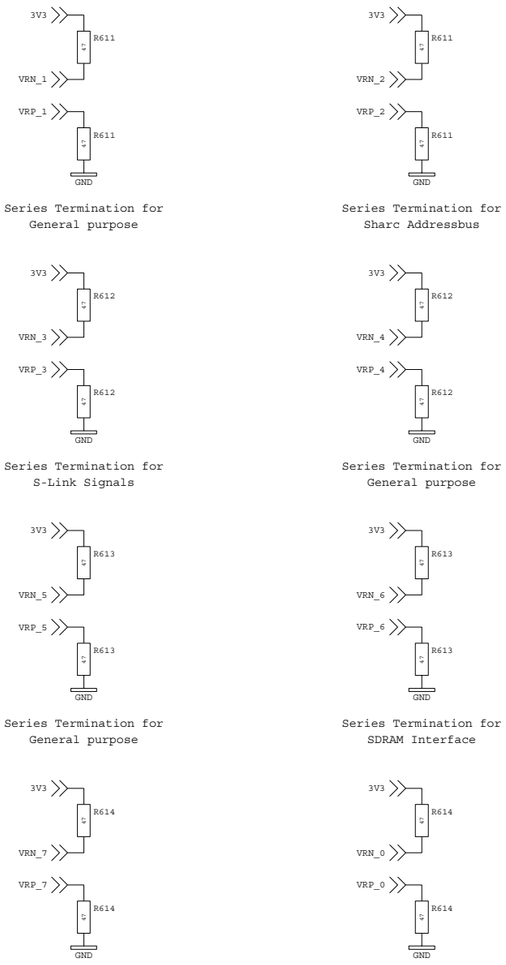
=> MGT Termination (estimated 2 * 11 mA = 22 mA)

1V8 @ 1,5A

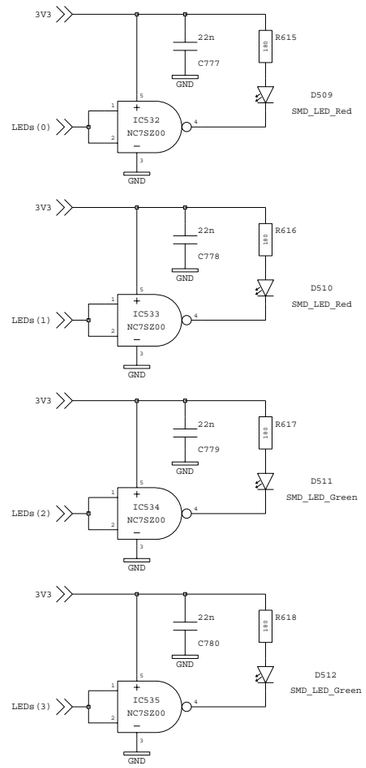


=> MGT RX Termination (estimated 8 * 11 mA = 88 mA)

Note: VT1V8_MGT is common to all MROD-Ins



MROD-Out		Rev V2 3	
Outp FPGA MGT Pwr Decoupling, Termination		Date 7 Feb 2006	
Proj: MROD-X	Proj.No: 38405	Time 1:29:37 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm	
		Page 9 of 19	



Fiducial1505 Fiducial1506

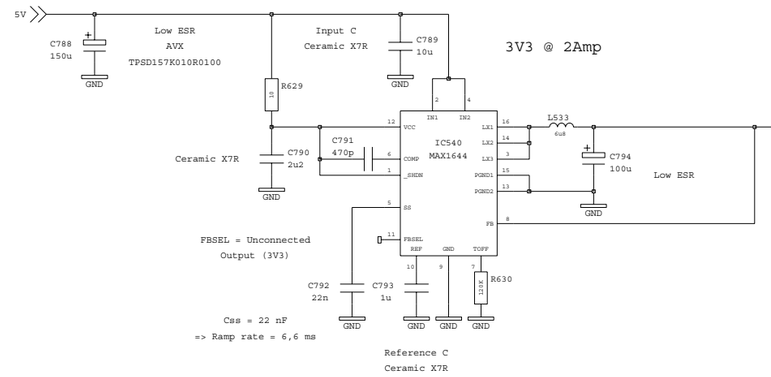
Fiducial1507 Fiducial1508

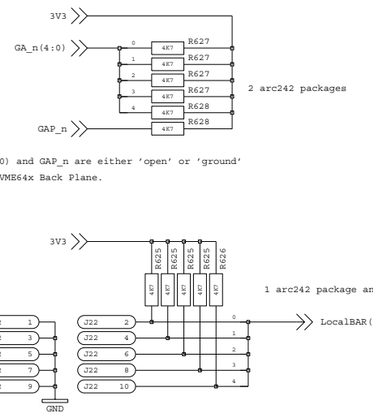
Board Fiducials

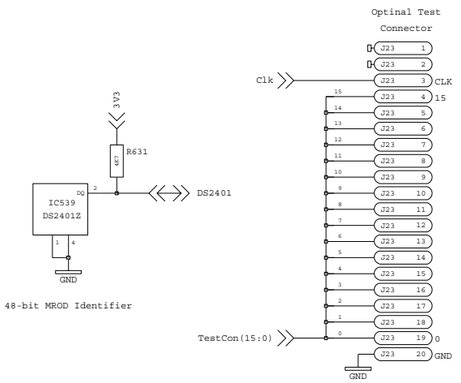
Fiducial1511 Fiducial1512

Fiducial1513 Fiducial1514

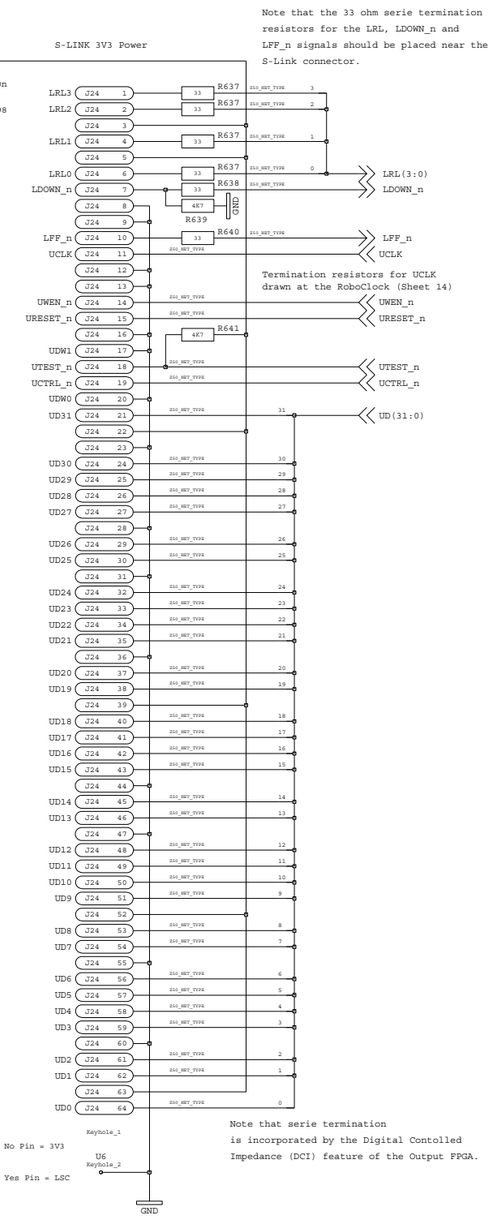
Fiducial1509 Fiducial1510

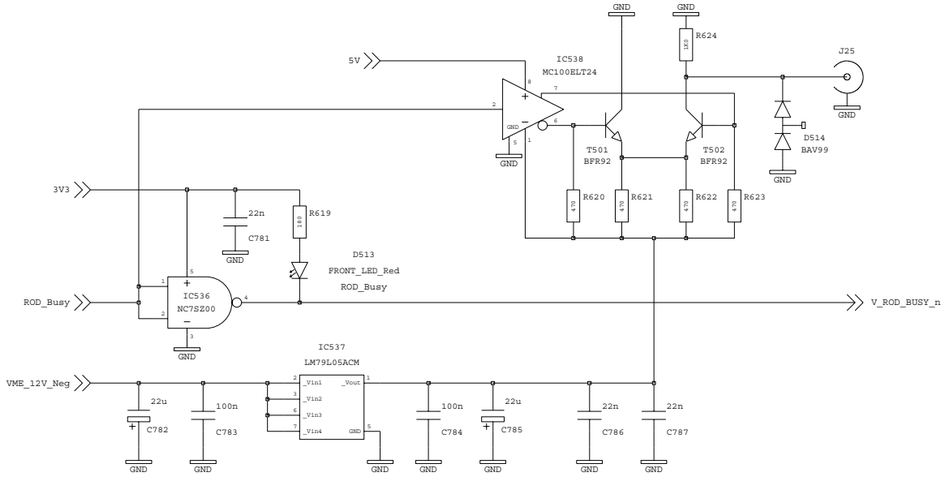






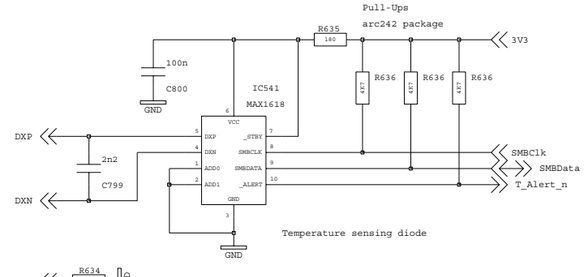
Module_En and SYSFAIL_En Terminals,
for test purposes only.





PWRDWN_B is unsupported (should be pulled high)

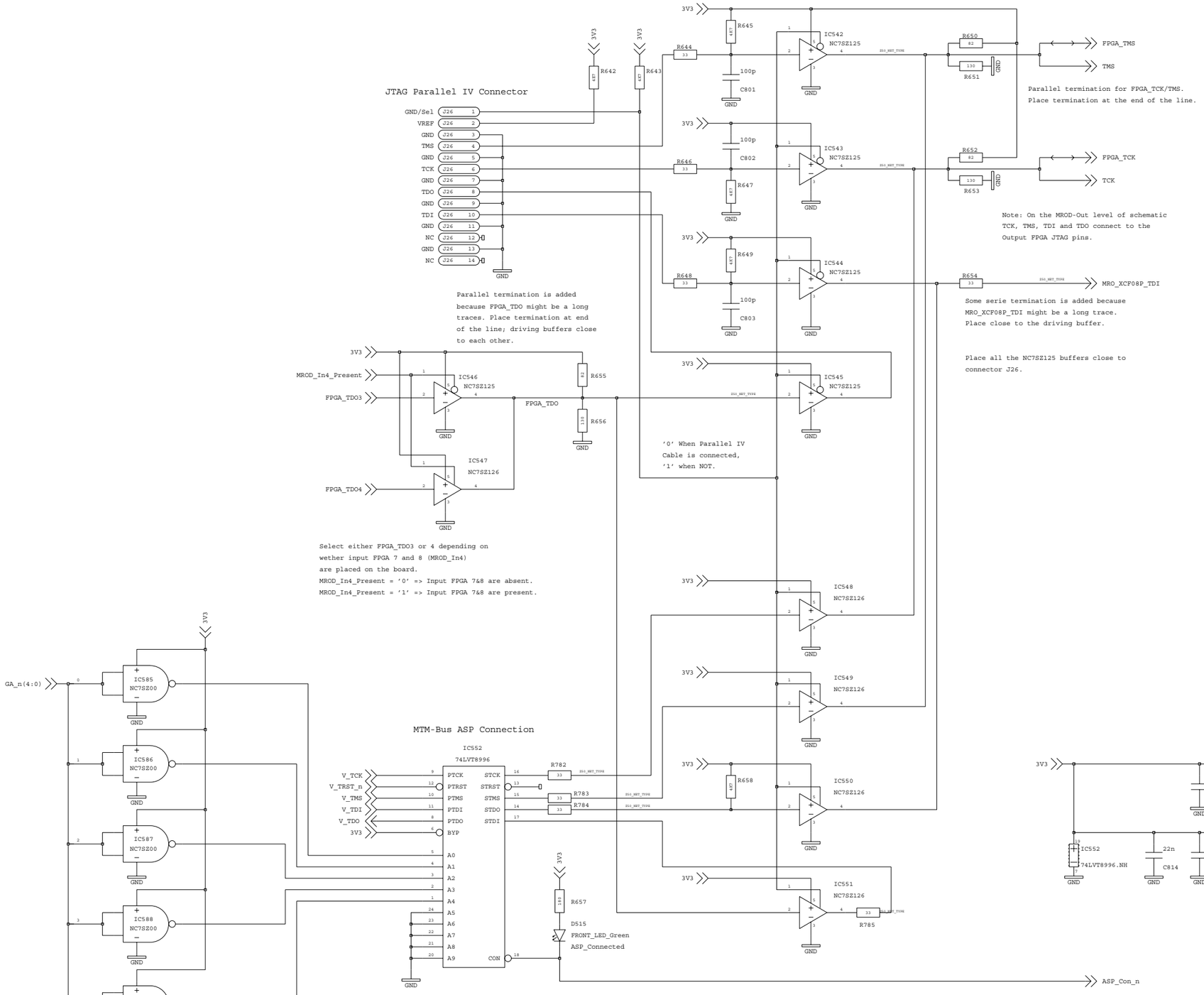
HSWAP_EN = '0' => User IOs have pull-up
resistors during configuration



VBATT is decriptor key memory backup supply

Other (Output) FPGA Control signals

MROD-Out	Rev V2 8
	Date 7 Feb 2006
	Time 1:29:59 pm
S-Link and Outp. FPGA Auxiliary Connections	Name tonvr
Proj: MROD-X / Proj.No: 38405	
Peter Jansweijer / peterj@nikhef.nl	Size A3 4 1 4 A
NIKHEF	Dim 420 x 297 mm
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA, KRUISLAAN 409, 020-592 2000, 1098 SJ AMSTERDAM NEDERLAND	Page 10 of 19



MROD-Out	Rev V2 4
	Date 7 Feb 2006
FPGA JTAG Chain	Time 1:32:17 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	
NIKHEF	Size A3 / 4 1 4 A
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
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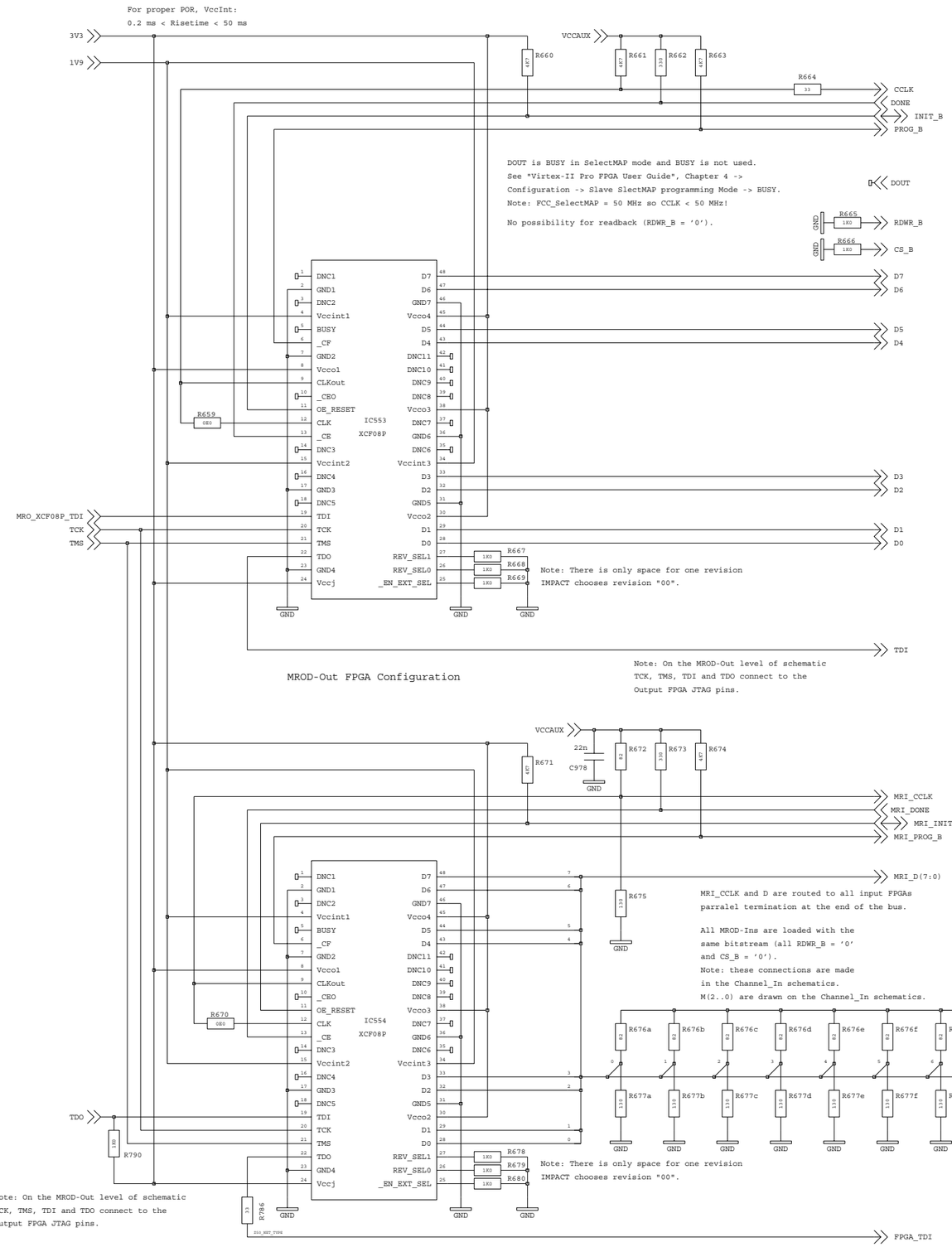
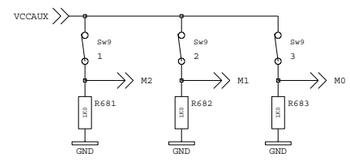
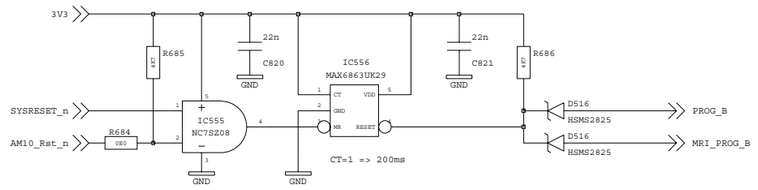




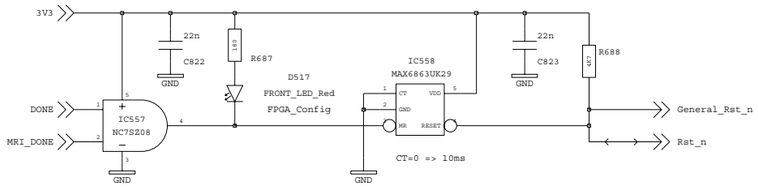
M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

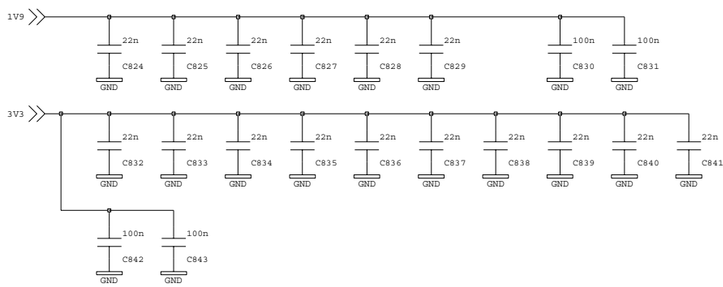
Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap
configuration. See Xilinx PROM Errata,
Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA
to Master SelectMap and all other MROD-In FPGAs
to Slave SelectMap.
Note: MROD-In M(2..0) are drawn on the Channel_In schematics.



A reset also issues a re-configuration of all FPGAs

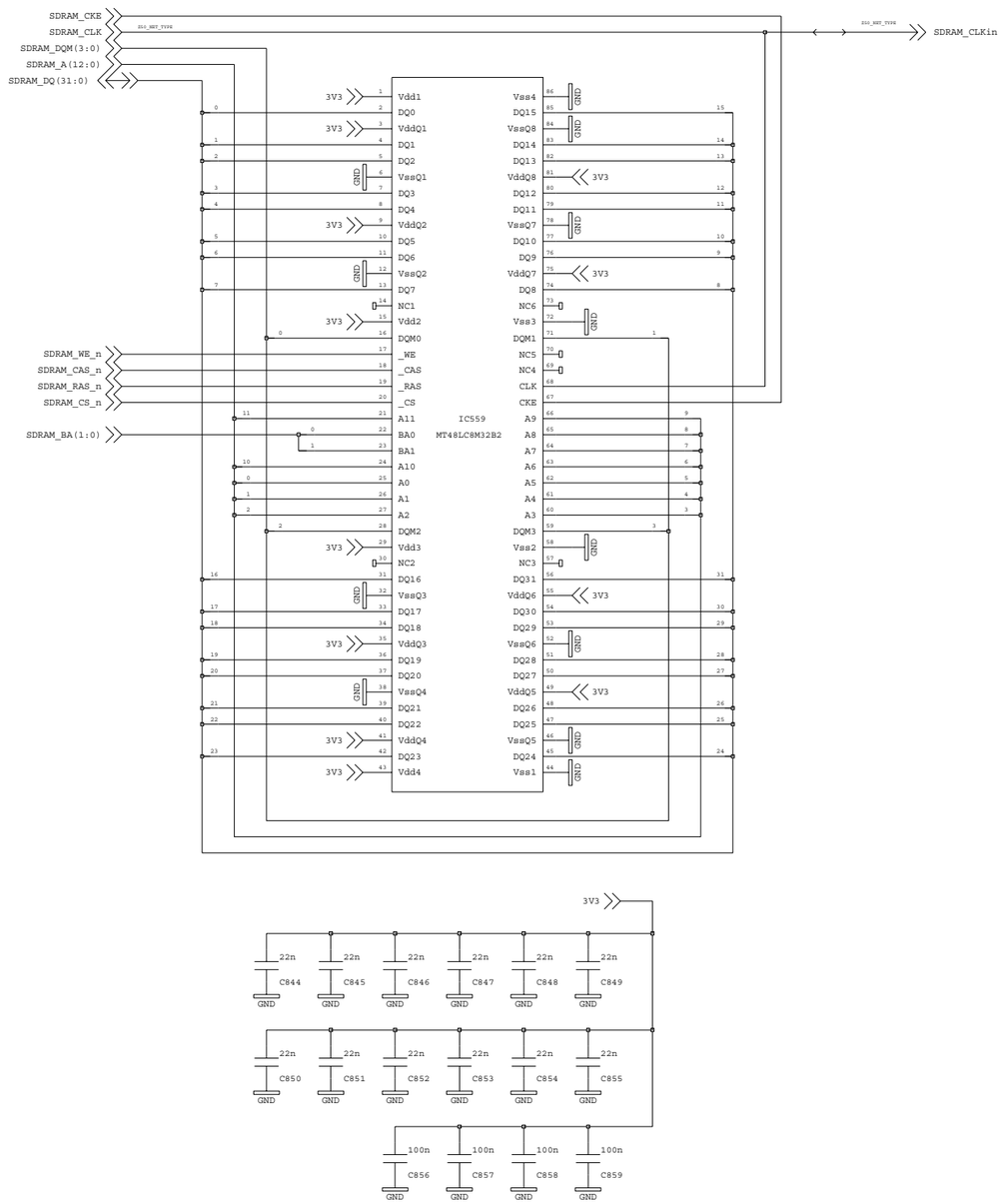


After re-configuration 'General_Rst_n' is kept active for 10 ms.

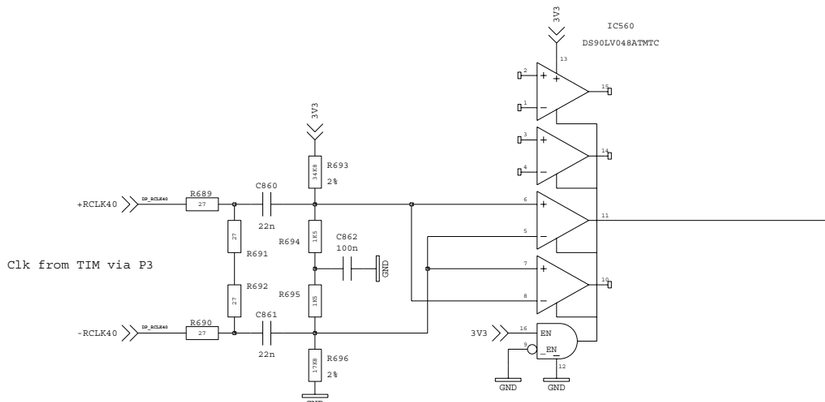


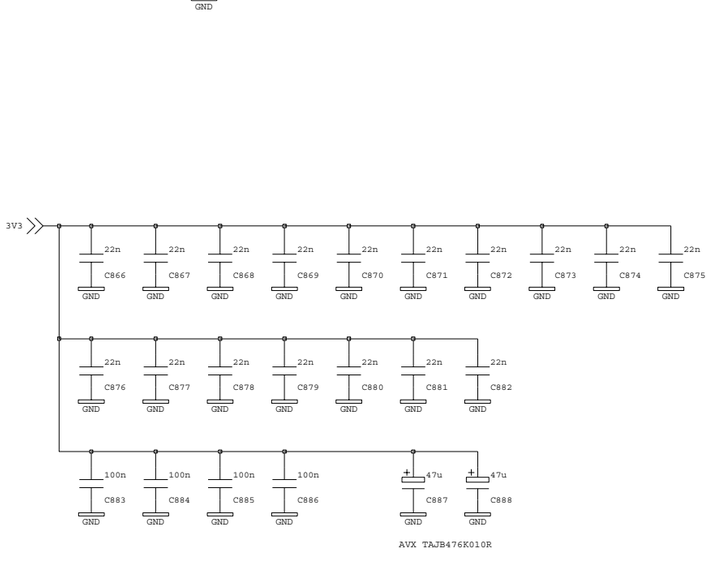
MROD-Out		Rev V2 9
		Date 7 Feb 2006
FPGA Configuration And Resets		Time 1:33:23 pm
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 12 of 19

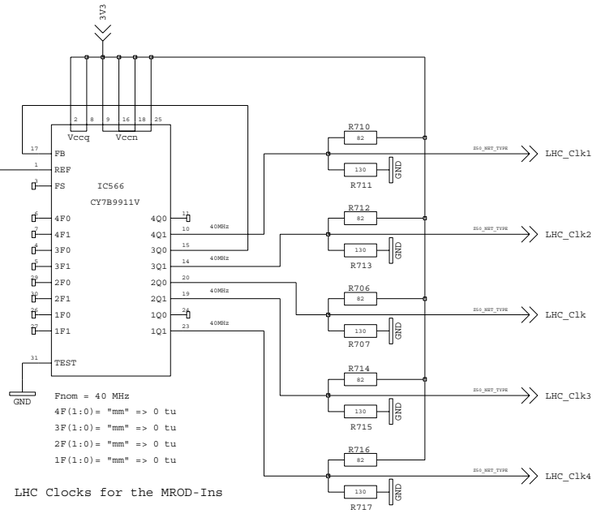
SDRAM_A(12) is not connected

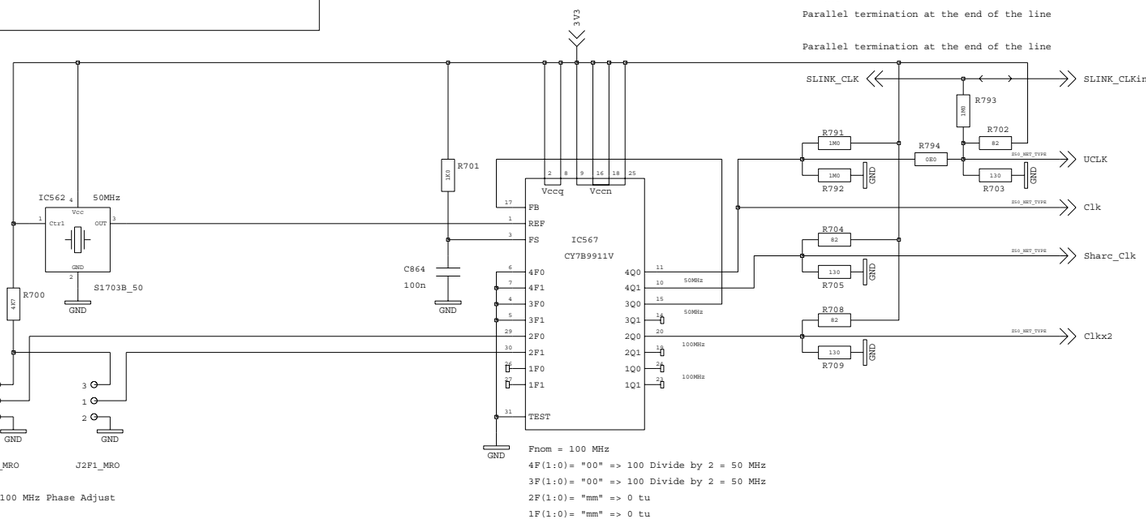


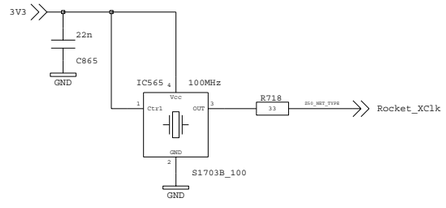
MROD-Out		Rev V2 3	
		Date 7 Feb 2006	
SDRAM		Time 1:33:40 pm	
Proj: MROD-X	Proj.No: 38405	Name tonvr	
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
		Page 13 of 19	











MROD-Out

Rev	V2 12
Date	7 Feb 2006
Time	1:34:07 pm
Name	Ton van Reen
Clocks	
Proj: MROD-X	Proj.No: 38405
Peter Jansweijer	peterj@nikhef.nl
Size	A3 4 1 4 A
Dim	420 x 297 mm
Page	14 of 19

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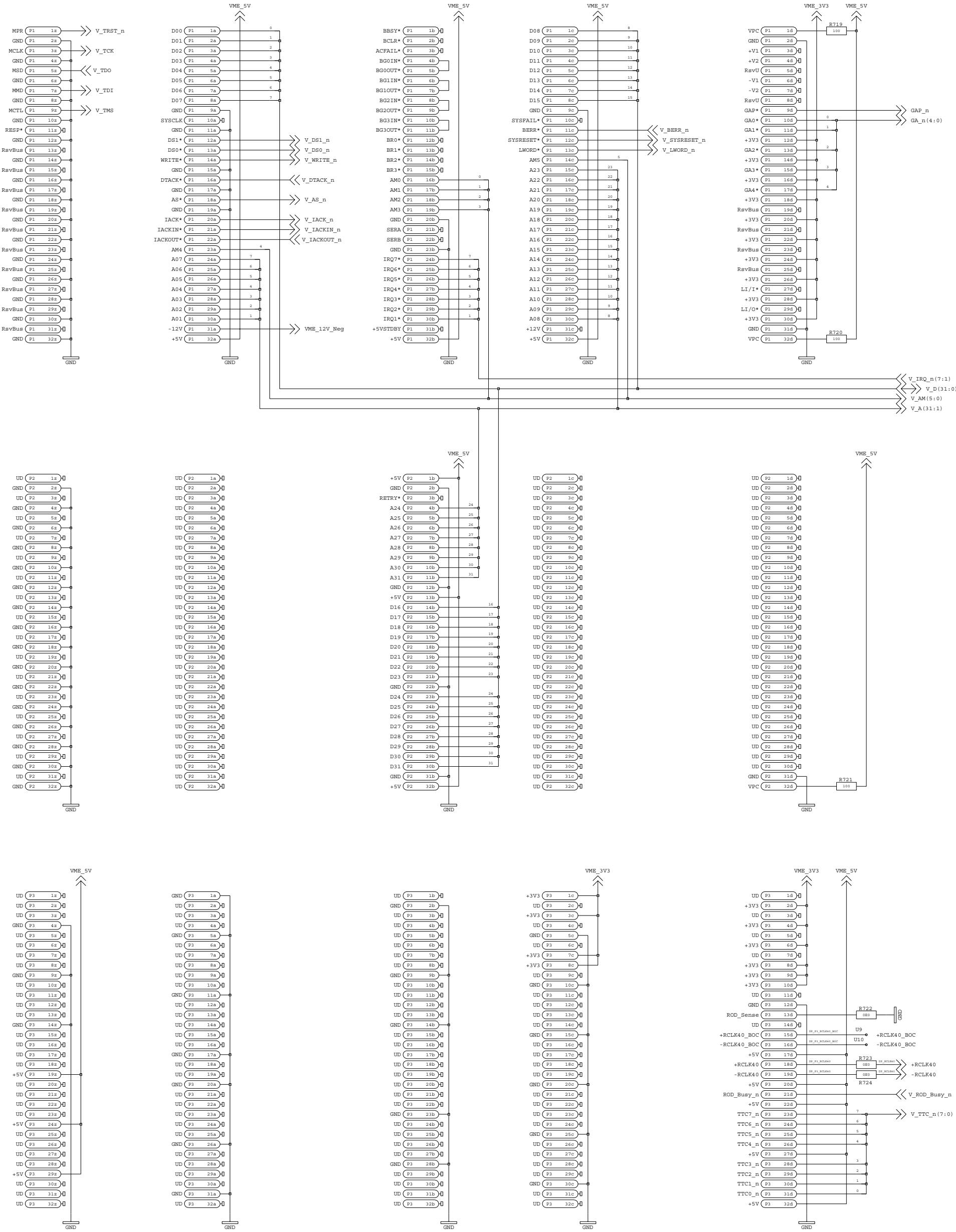

MROD-Out	
VME Connectors	
Proj: MROD-X	Proj.No: 38405
Peter Janweijer	peterj@nikhef.nl
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND
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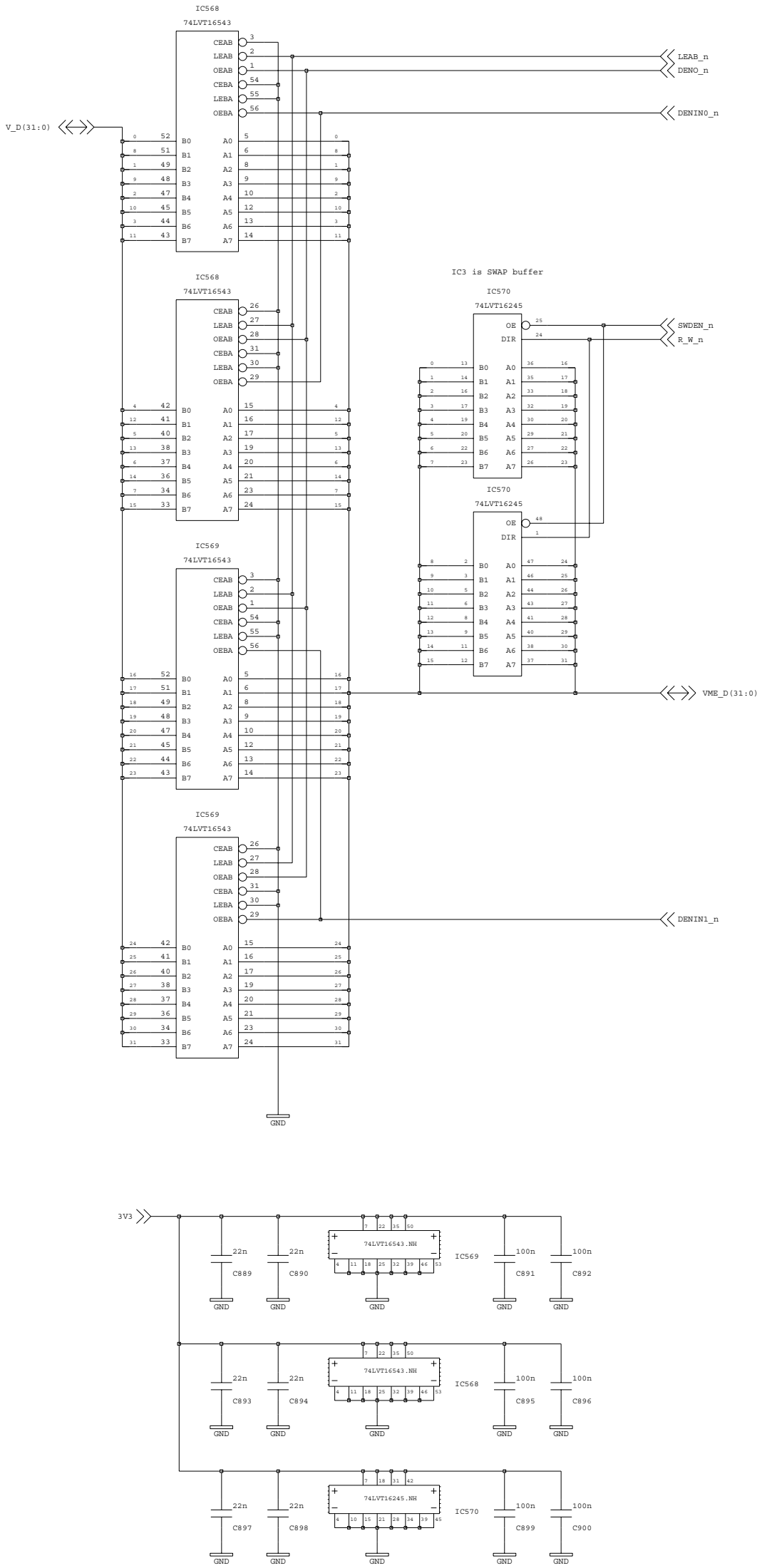
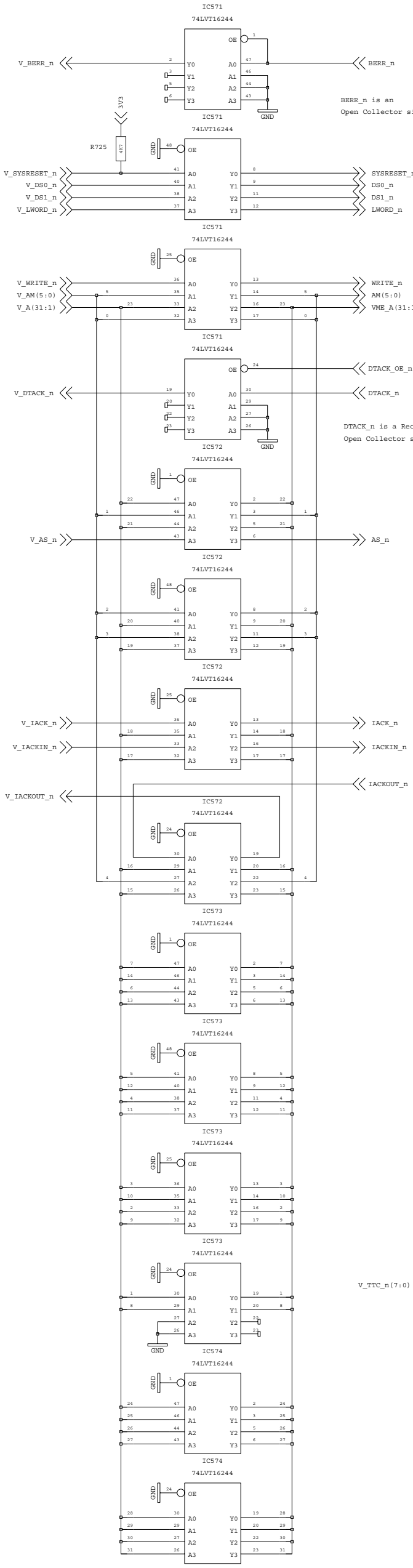
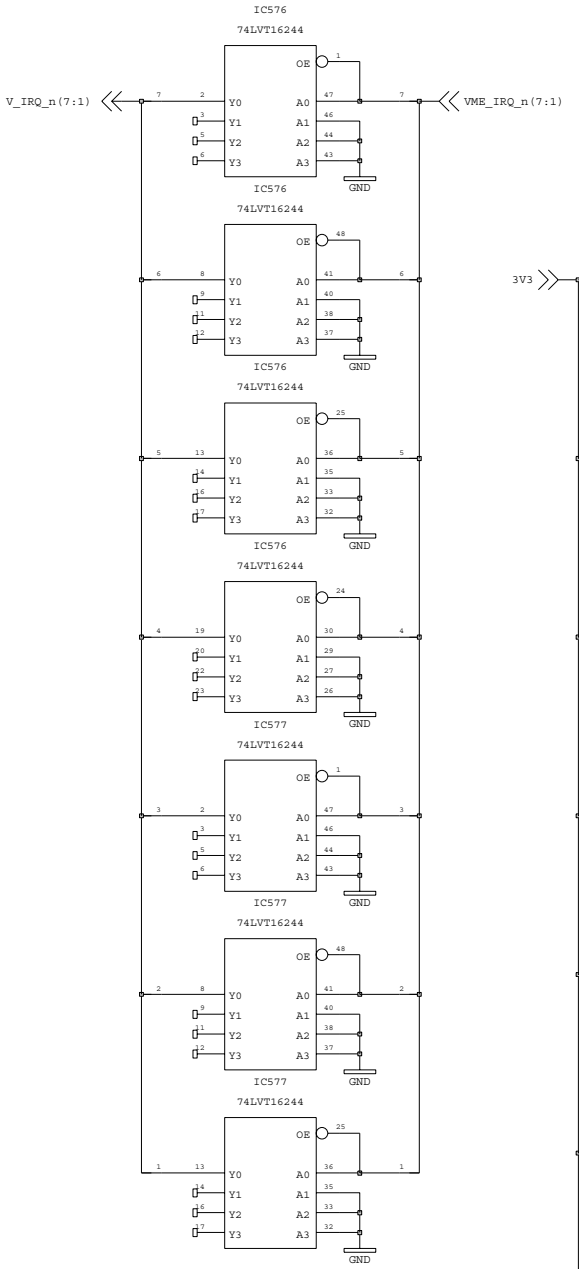
Rev	V2 3
Date	7 Feb 2006
Time	1:34:31 pm
Name	Ton van Reen
Size	A3 4 1 4 A
Dim	297 x 420 mm
Page	15 of 19

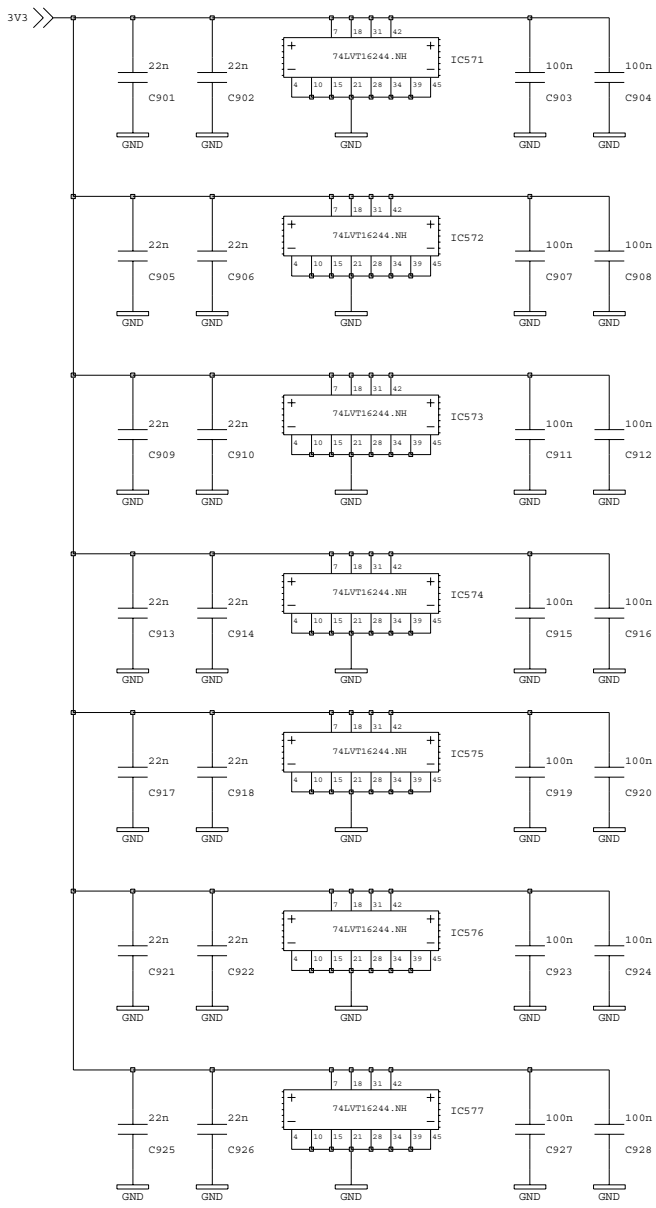


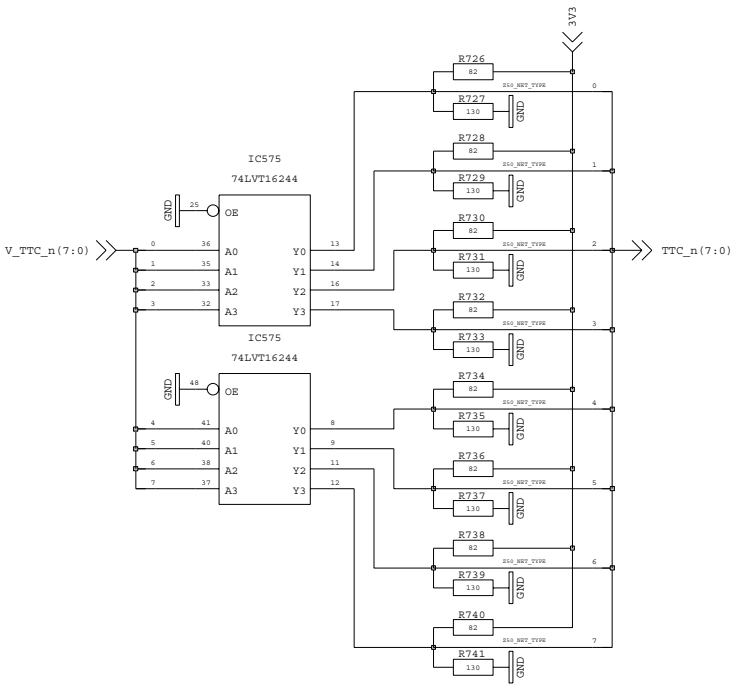
MROD-Out		Rev	V2 3
		Date	7 Feb 2006
VME DataBus Buffers		Time	1:34:59 pm
Proj: MROD-X	Proj.No: 38405	Name	Ton van Reen
peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size	A3 4 1 4 A
		Dim	297 x 420 mm
		Page	16 of 19

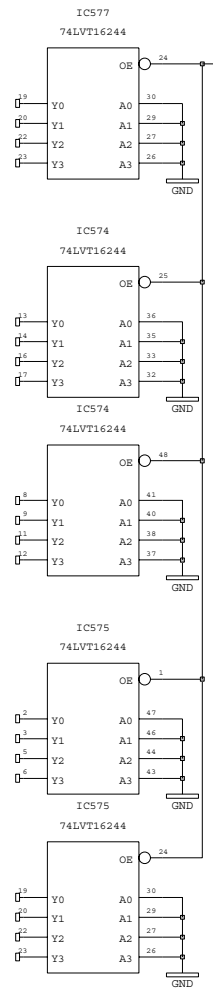
Note: VME signals are 5V.
Most Logic on the MROD is NOT 5V tolerant!
Therefore all VME signals need to be
buffered by a 3V3 (but 5V tolerant) buffer.



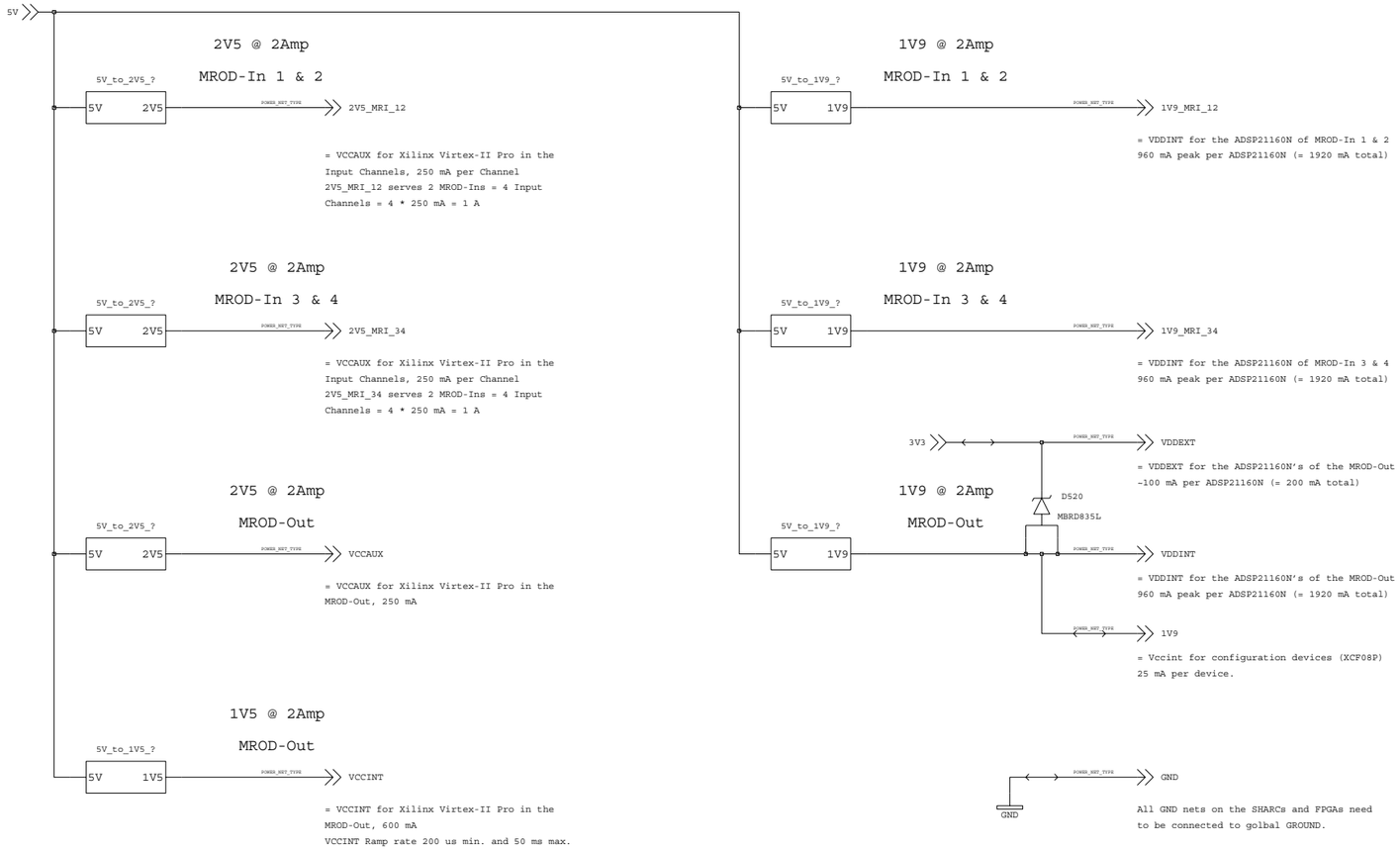




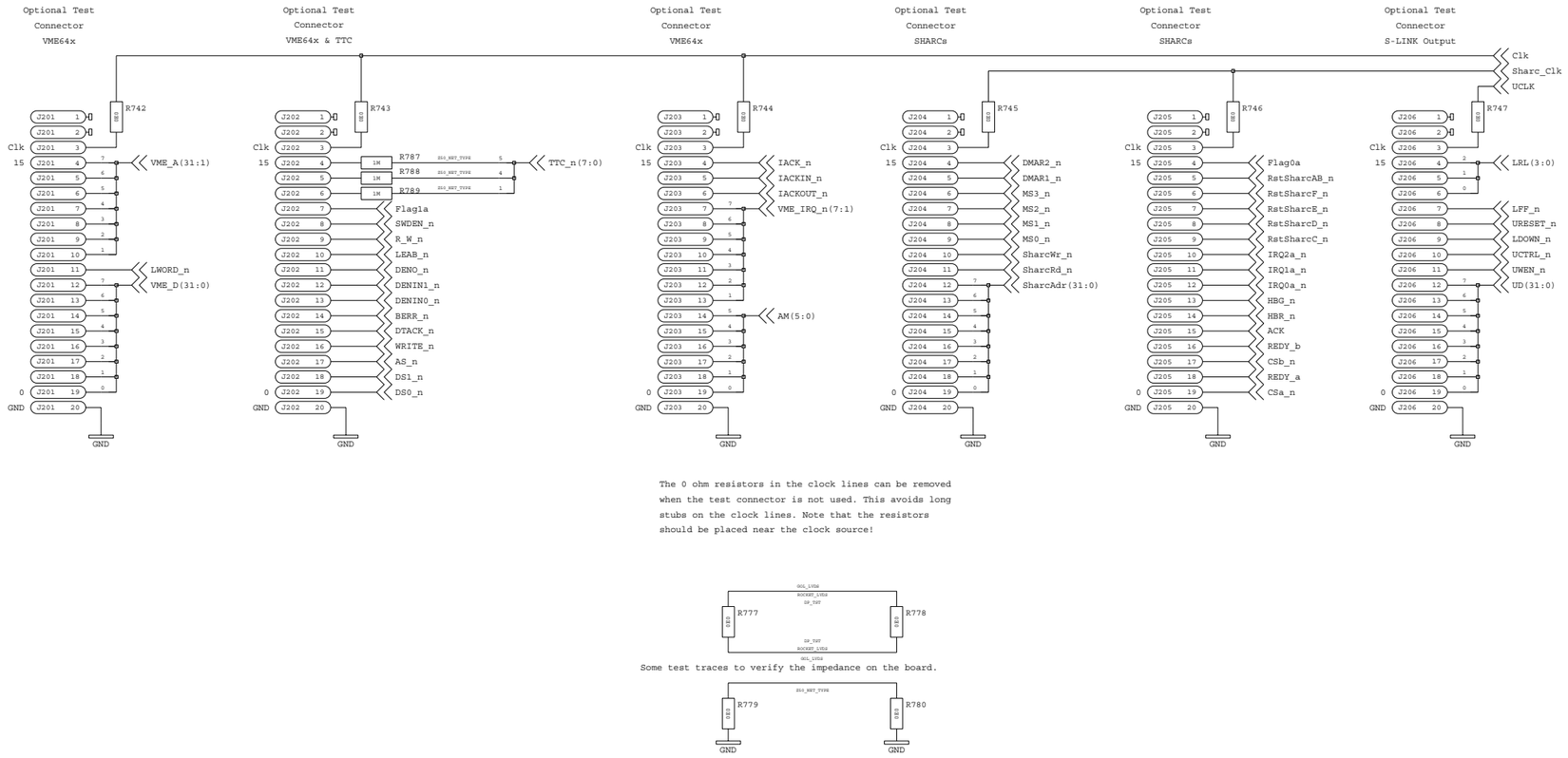




MROD-Out		Rev V2 3
		Date 7 Feb 2006
VME Bus Other Buffers		Time 1:35:25 pm
Proj: MROD-X	Proj.No:	Name Ton van Reen
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 297 x 420 mm
		Page 17 of 19



MROD-Out	Rev V2 3
	Date 7 Feb 2006
Power Supplies	Time 1:35:57 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	
NIKHEF	Size A3 / 4 1 4 A
© ET-Nikhef Amsterdam	Dim 420 x 297 mm
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Page 18 of 19



The 0 ohm resistors in the clock lines can be removed when the test connector is not used. This avoids long stubs on the clock lines. Note that the resistors should be placed near the clock source!

Some test traces to verify the impedance on the board.

MROD-Out

Test connectors

Proj: MROD-X	Proj.No: 38405
Peter Jansweijer	peterj@nikhef.nl

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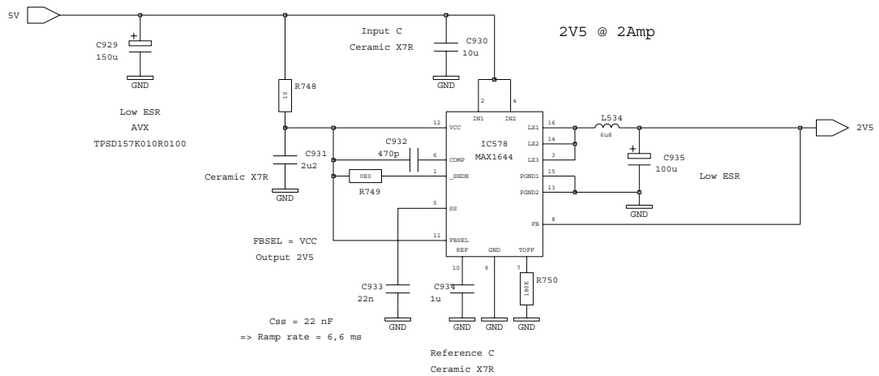
Rev	V2 4
Date	7 Feb 2006
Time	1:36:13 pm
Name	tonvr
Size	A3 4 1 4 A
Dim	420 x 297 mm
Page	19 of 19



Power Supply	Rev V2 2
	Date 7 Feb 2006
5V -> 2V5 @ 2A	Time 1:36:58 pm
Proj: MROD-X	Proj.No: 38405
	Name tonvr
Peter Jansweijer	peterj@nikhef.nl
	Size A3 4 1 4 A
NIKHEF	Dim 420 x 297 mm
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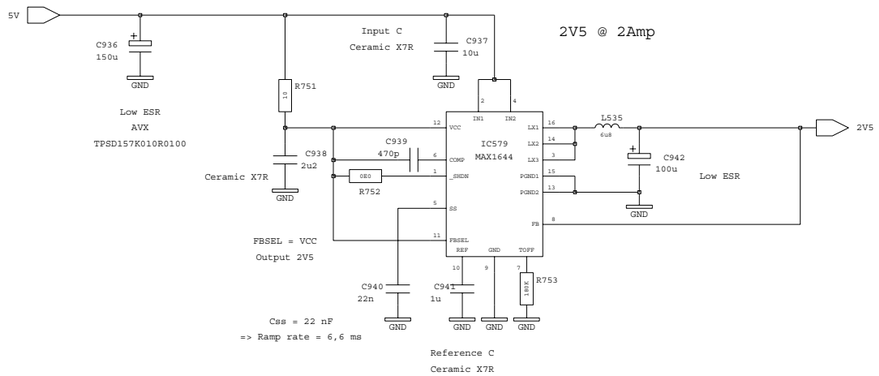

Power Supply	Rev V2 2
	Date 7 Feb 2006
	Time 1:36:58 pm
5V -> 2V5 @ 2A	Name tonvr
Proj: MROD-X / Proj.No: 38405	
Peter Jansweijer / peterj@nikhef.nl	Size A3 / 4 1 4 A
NIKHEF	Dim 420 x 297 mm
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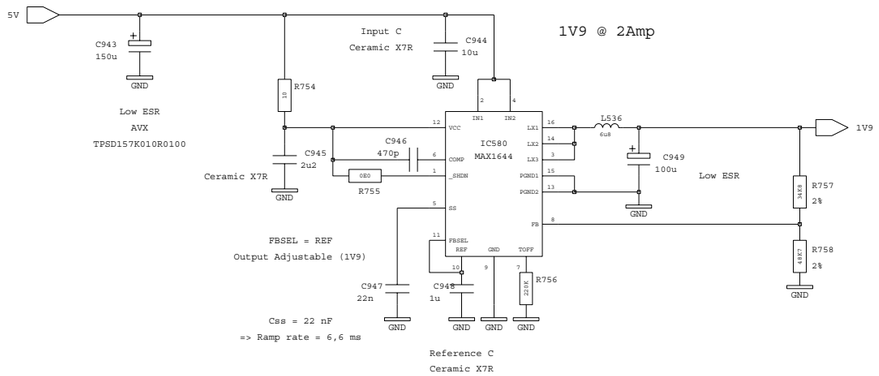
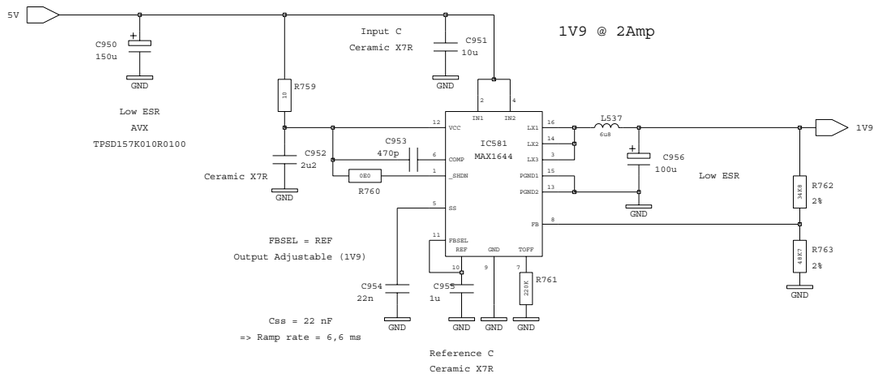


Power Supply		Rev V2 2	
5V -> 1V9 @ 2A		Date 7 Feb 2006	
Proj: MROD_X	Proj.No: 38405	Time 1:39:18 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
		Page 1 of 1	



Power Supply

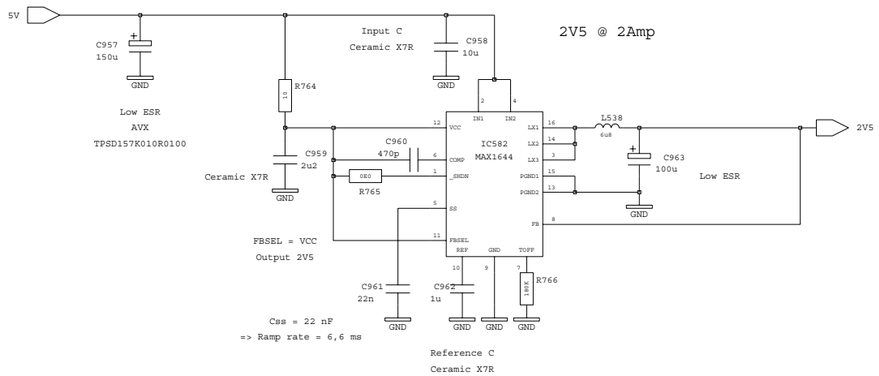
5V -> 1V9 @ 2A

Proj: MROD_X	Proj.No: 38405
Peter Jansweijer	peterj@nikhef.nl

NIKHEF

NATIONAAL INSTITUUT VOOR KERN-
FYSICA EN HOGE ENERGIE-FYSICA
KRUISLAAN 409, 020-592 2000
1098 SJ AMSTERDAM NEDERLAND

Rev	V2 2
Date	7 Feb 2006
Time	1:39:18 pm
Name	tonvr
Size	A3 4 1 4 A
Dim	420 x 297 mm
Page	1 of 1



Power Supply			Rev V2 2
			Date 7 Feb 2006
5V -> 2V5 @ 2A			Time 1:36:58 pm
Proj: MROD-X	Proj.No: 38405		Name tonvr
Peter Jansweijer	peterj@nikhef.nl		
			Size A3 4 1 4 A
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Dim 420 x 297 mm
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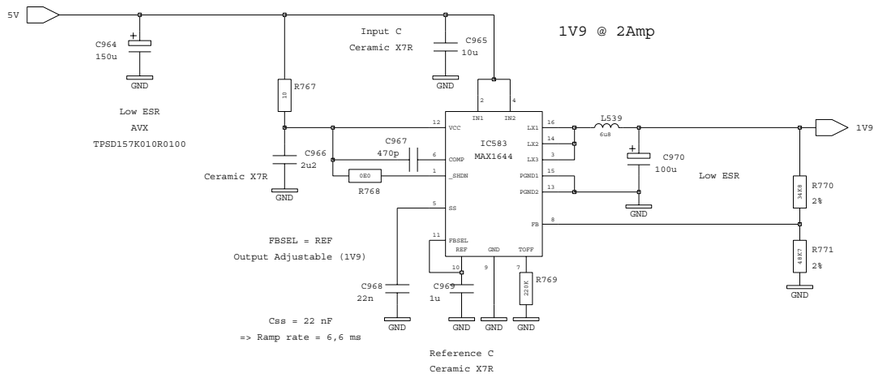
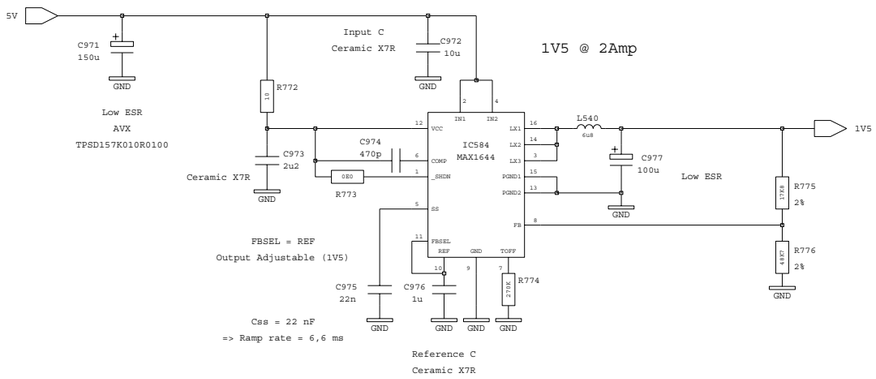


Power Supply		Rev V2 2	
5V -> 1V9 @ 2A		Date 7 Feb 2006	
Proj: MROD_X	Proj.No: 38405	Time 1:39:18 pm	
Peter Jansweijer	peterj@nikhef.nl	Name tonvr	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
		Dim 420 x 297 mm	
		Page 1 of 1	



Power Supply			Rev V2 2
			Date 7 Feb 2006
5V -> 1V5 @ 2A			Time 1:38:24 pm
Proj: MROD-X	Proj.No: 38405		Name tonvr
Peter Jansweijer	peterj@nikhef.nl		
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3	4 1 4 A
© ET-Nikhef Amsterdam		Dim	420 x 297 mm
		Page	1 of 1