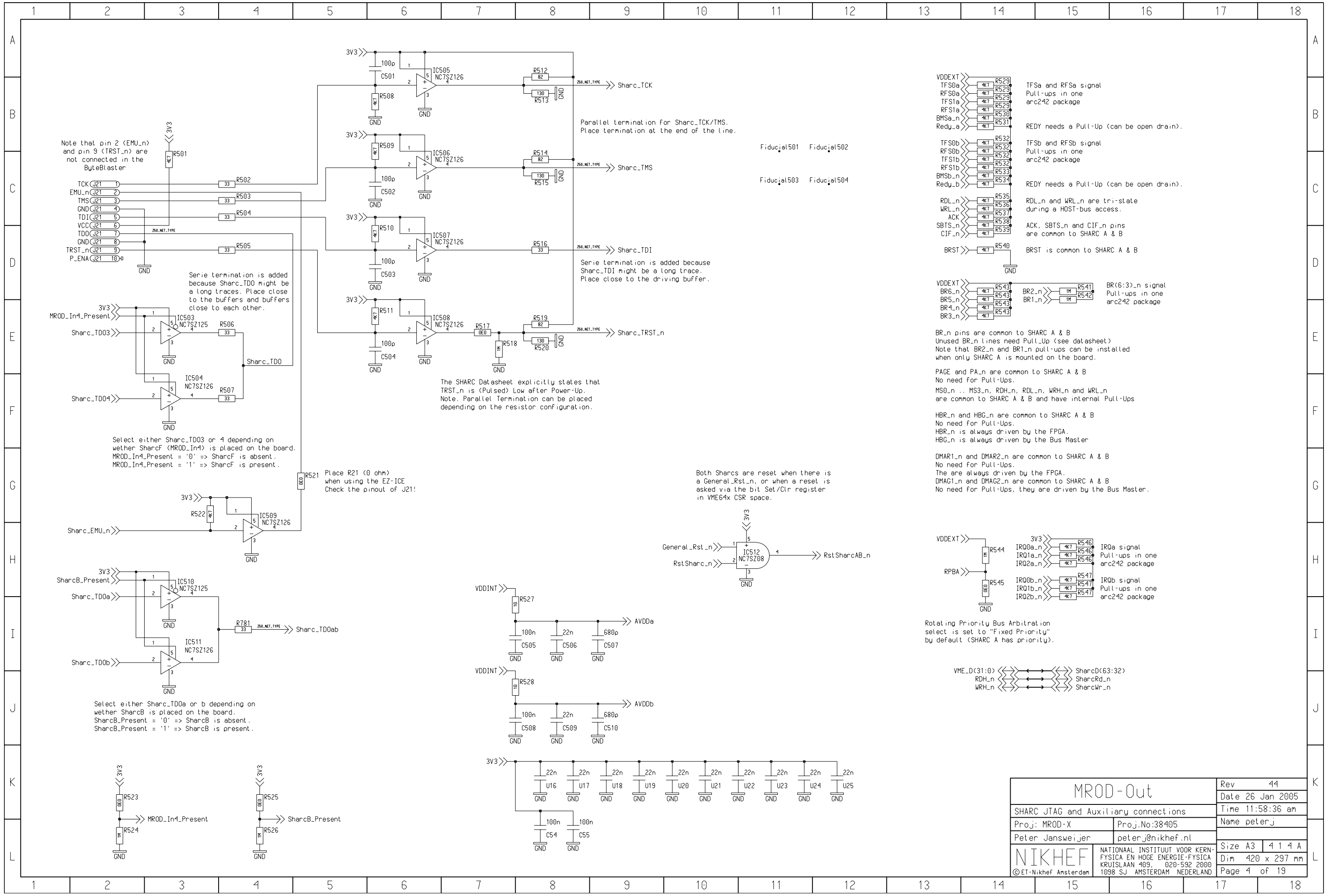
Note that pin 2 (EMU_n) and pin 9 (TRST_n) are not connected in the ByteBlaster
TCK J21 1
EMU_n J21 2
TMS J21 3
GND J21 4
TDI J21 5
VCC J21 6
TDO J21 7
GND J21 8
TRST_n J21 9
P_ENA J21 10
R501 4K7
R502 33
R503 33
R504 33
R505 33
Z50_NET_TYPE
Serie termination is added because Sharc_TDO might be a long traces. Place close to the buffers and buffers close to each other.
3V3
MROD_In4_Present
Sharc_TDO3
IC503 NC7SZ125
R506 33
Sharc_TDO
IC504 NC7SZ126
Sharc_TDO4
R507 33
Select either Sharc_TDO3 or 4 depending on wether SharcF (MROD_In4) is placed on the board.
MROD_In4_Present = '0' => SharcF is absent.
MROD_In4_Present = '1' => SharcF is present.
R521 0E0
Place R21 (0 ohm) when using the EZ-ICE
Check the pinout of J21!
Sharc_EMU_n
R522 4K7
IC509 NC7SZ126
SharcB_Present
Sharc_TDOa
IC510 NC7SZ125
R781 33
Sharc_TDOab
IC511 NC7SZ126
Sharc_TDOb
Select either Sharc_TDOa or b depending on wether SharcB is placed on the board.
SharcB_Present = '0' => SharcB is absent.
SharcB_Present = '1' => SharcB is present.
R523 0E0
R524 1M
MROD_In4_Present
R525 0E0
R526 1M
SharcB_Present
IC505 NC7SZ126
C501 100p
R508 4K7
R512 82
R513 130
Sharc_TCK
IC506 NC7SZ126
C502 100p
R509 4K7
R514 82
R515 130
Sharc_TMS
IC507 NC7SZ126
C503 100p
R510 4K7
R516 33
Sharc_TDI
IC508 NC7SZ126
C504 100p
R511 4K7
R517 0E0
R518 1M
R519 82
R520 130
Sharc_TRST_n
Parallel termination for Sharc_TCK/TMS.
Place termination at the end of the line.
Serie termination is added because Sharc_TDI might be a long trace.
Place close to the driving buffer.
The SHARC Datasheet explicitly states that TRST_n is (Pulsed) Low after Power-Up.
Note. Parallel Termination can be placed depending on the resistor configuration.
Fiducial501
Fiducial502
Fiducial503
Fiducial504
Both Sharcs are reset when there is a General_Rst_n, or when a reset is asked via the bit Set/Clr register in VME64x CSR space.
General_Rst_n
RstSharc_n
IC512 NC7SZ08
RstSharcAB_n
VDDINT
R527 10
AVDDa
C505 100n
C506 22n
C507 680p
R528 10
AVDDb
C508 100n
C509 22n
C510 680p
U16 22n
U17 22n
U18 22n
U19 22n
U20 22n
U21 22n
U22 22n
U23 22n
U24 22n
U25 22n
C54 100n
C55 100n
VDDEXT
TFS0a
RFS0a
TFS1a
RFS1a
BMSa_n
Redy_a
R529 4K7
R530 4K7
R531 4K7
TFSa and RFSa signal Pull-ups in one arc242 package
REDY needs a Pull-Up (can be open drain).
TFS0b
RFS0b
TFS1b
RFS1b
BMSb_n
Redy_b
R532 4K7
R533 4K7
R534 4K7
TFSb and RFSb signal Pull-ups in one arc242 package
REDY needs a Pull-Up (can be open drain).
RDL_n
WRL_n
ACK
SBTS_n
CIF_n
R535 4K7
R536 4K7
R537 4K7
R538 4K7
R539 4K7
RDL_n and WRL_n are tri-state during a HOST-bus access.
ACK, SBTS_n and CIF_n pins are common to SHARC A & B
BRST
R540 4K7
BRST is common to SHARC A & B
VDDEXT
BR6_n
BR5_n
BR4_n
BR3_n
R543 4K7
BR2_n
BR1_n
R541 1M
R542 1M
BR(6:3)_n signal Pull-ups in one arc242 package
BR_n pins are common to SHARC A & B
Unused BR_n lines need Pull_Up (see datasheet)
Note that BR2_n and BR1_n pull-ups can be installed when only SHARC A is mounted on the board.
PAGE and PA_n are common to SHARC A & B
No need for Pull-Ups.
MS0_n .. MS3_n, RDH_n, RDL_n, WRH_n and WRL_n are common to SHARC A & B and have internal Pull-Ups
HBR_n and HBG_n are common to SHARC A & B
No need for Pull-Ups.
HBR_n is always driven by the FPGA.
HBG_n is always driven by the Bus Master
DMAR1_n and DMAR2_n are common to SHARC A & B
No need for Pull-Ups.
The are always driven by the FPGA.
DMAG1_n and DMAG2_n are common to SHARC A & B
No need for Pull-Ups, they are driven by the Bus Master.
VDDEXT
R544 1M
RPBA
R545 0E0
IRQ0a_n
IRQ1a_n
IRQ2a_n
R546 4K7
IRQ0a signal Pull-ups in one arc242 package
IRQ0b_n
IRQ1b_n
IRQ2b_n
R547 4K7
IRQb signal Pull-ups in one arc242 package
Rotating Priority Bus Arbitration select is set to "Fixed Priority" by default (SHARC A has priority).
VME_D(31:0)
RDH_n
WRH_n
SharcD(63:32)
SharcRd_n
SharcWr_n
MROD-Out
SHARC JTAG and Auxiliary connections
Proj: MROD-X
Proj.No:38405
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1098 SJ AMSTERDAM NEDERLAND
Rev 44
Date 26 Jan 2005
Time 11:58:36 am
Name peterj
Size A3 4 1 4 A
Dim 420 x 297 mm
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