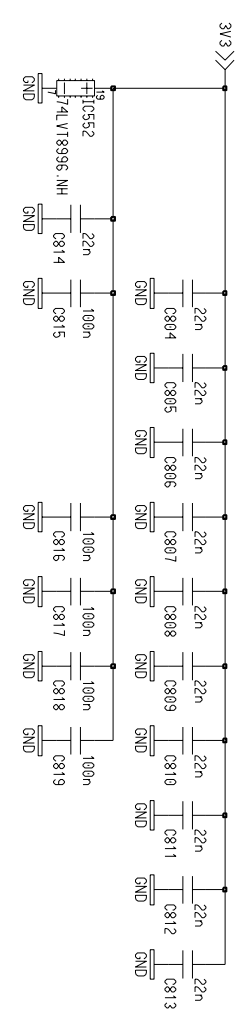


Parallel termination is added because FPGA_T00 might be a long traces. Place termination at end of the line, driving buffers close to each other.

Select either FPGA_T003 or 4 depending on whether input FPGA 7 and 8 (MR0D_In4) are placed on the board.
MR0D_In4-Present = '0' => Input FPGA 7&8 are absent.
MR0D_In4-Present = '1' => Input FPGA 7&8 are present.

Note: On the MR0D-Out level of schematic TCK, TMS, TDI and TDO connect to the Output FPGA JTAG pins.
Some series termination is added because MR0D-Out might be a long trace. Place close to the driving buffer.
Place all the NC7SZ125 buffers close to connector J26



MR0D-Out		Rev	45
Date		26 Jan 2005	
Time		12:04:33 pm	
Name		petern.jansweijer	
Proj. No.		38405	
Proj.		MR0D-X	
Proj. Owner		petern.jansweijer	
Size		A3	4 1 4 A
Dim		420 x 297 mm	
Page		11 of 19	

NIKHEF
 NATIONAAL INSTITUUT VOOR KERN-
 FYSICA EN HOOG ENERGIE-FYSICA
 KRUISLAAN 409, 020-592 2000
 1098 SJ AMSTERDAM NEDERLAND
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