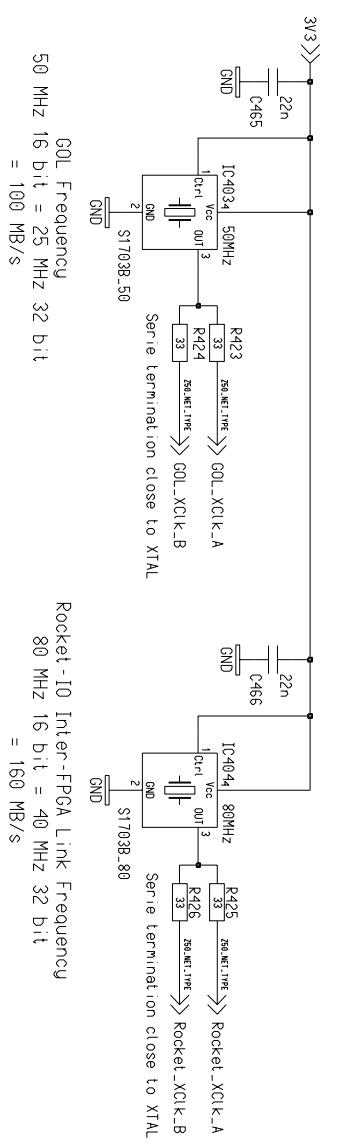
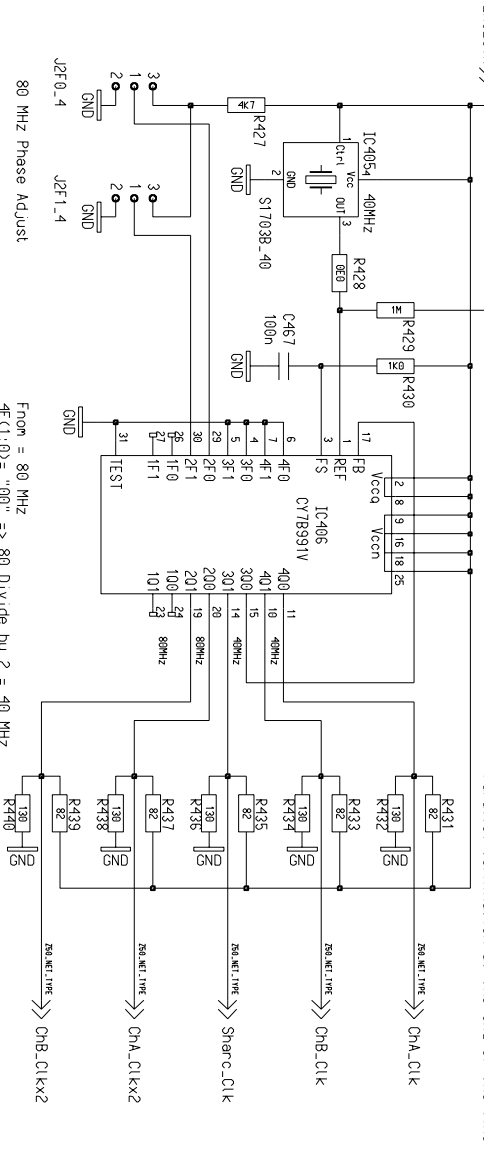


SV_L0_11V5_2
 1V5 = VCCINT for Xilinx Virtex-II Pro in the Input Channels, 500 mA per Channel
 VCCINT Ramp rate 200 us min. and 50 ns max.

3V3 >>> VDDEXT = VDDEXT for the ADSP21160N
 100 mA per ADSP21160N
 Note ADSP21160N Power-On Sequence!
 Time between power-on VDDINT -> VDDEXT = -50 ns to +200 ns
 1V9 >>> VDDINT = VDDINT for the ADSP21160N
 950 mA peak per ADSP21160N
 2V5 >>> VCCAUX for the Xilinx Virtex-II Pro in the Input Channel, 250 mA per Channel
 All GND nets on the SHARC need to be connected to global GROUND.



3V3 >>> LHC_CLK >>> The System Clock can be locked to a crystal or to the LHC_CLK depending on the resistors placed.
 Parallel termination at the end of the line



SHARC and Input Channel System Clock

From = 80 MHz
 fF(1:0) = "00" => 80 Divide by 2 = 40 MHz
 fF(1:0) = "01" => 80 Divide by 2 = 40 MHz
 fF(1:0) = "10" => 80 Divide by 2 = 40 MHz
 fF(1:0) = "11" => 0 tu
 fF(1:0) = "mm" => 0 tu

A	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
B																		
C																		
D																		
E																		
F																		
G																		
H																		
I																		
J																		
K																		
L																		

MR0D-In		Rev	57
Power and Clocks		Date	26 Jan 2005
Proji: MR0D-X		Time	12:09:03 pm
Peter Jansweijer		Name	peter.j
Proji: MR0D-X		Proji.No:	38405
Peter Jansweijer		Size	A3
NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOOG-ENERGIE-FYSICA KRUISLAAN 409, 020-532 2000 1098 SJ AMSTERDAM NEDERLAND		Dim	420 x 297 mm
©ET-Nikhef Amsterdam		Page	4 of 4