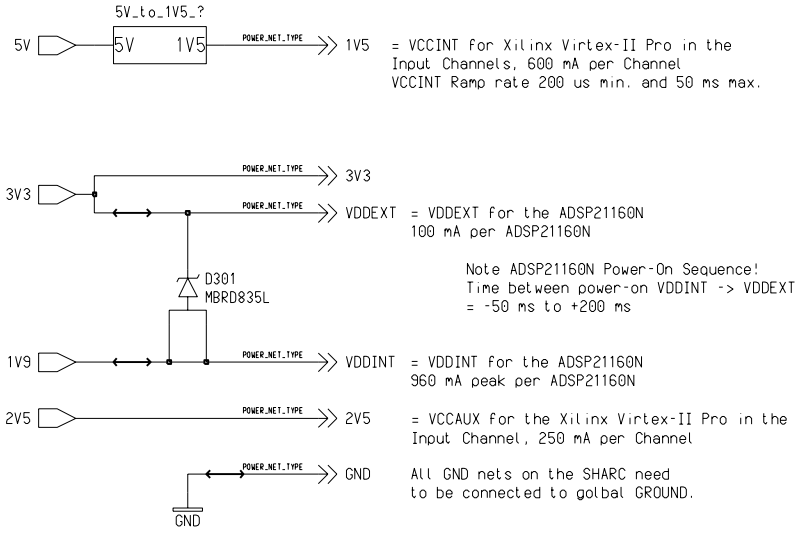
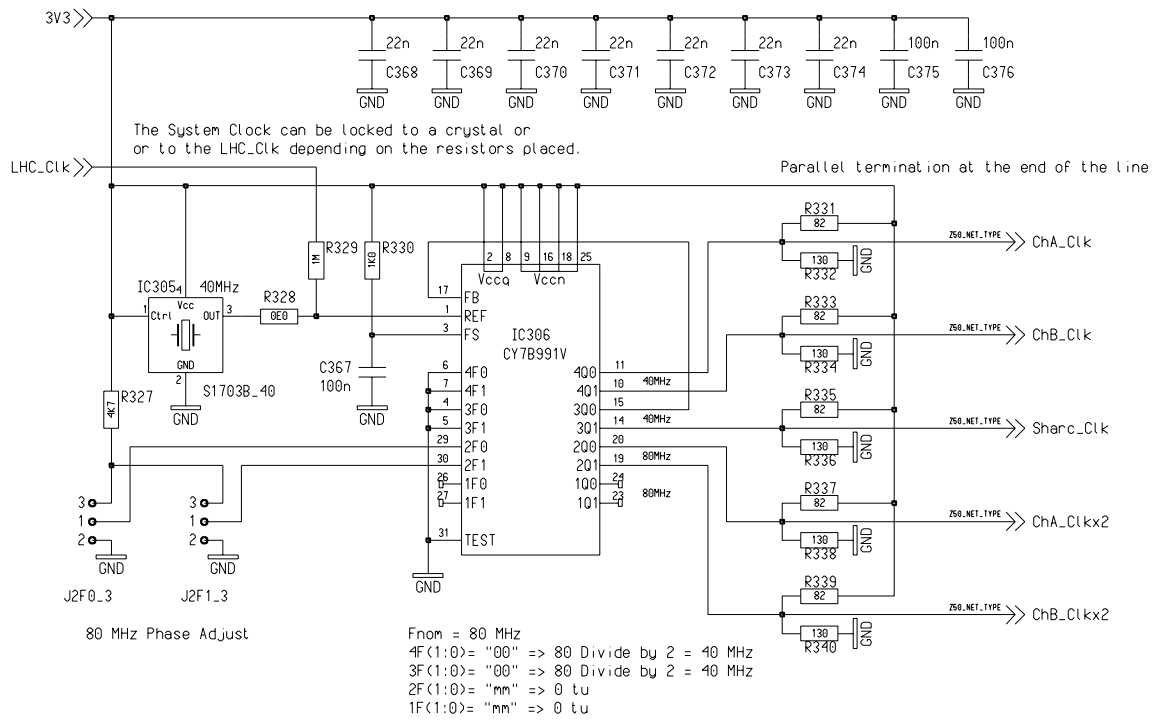
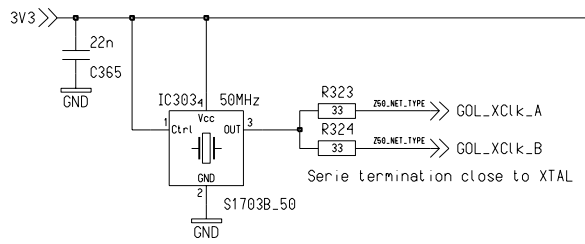
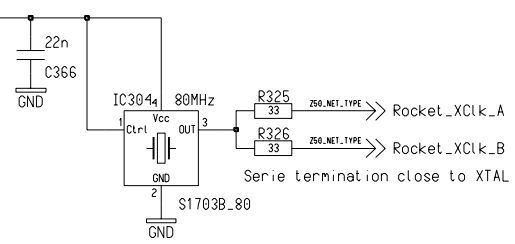




SHARC and Input Channel System Clock



GOL Frequency
50 MHz 16 bit = 25 MHz 32 bit
= 100 MB/s



Rocket-IO Inter-FPGA Link Frequency
80 MHz 16 bit = 40 MHz 32 bit
= 160 MB/s

MROD-In		Rev 57
		Date 26 Jan 2005
		Time 12:09:03 pm
Power and Clocks		Name peterj
Proj: MROD-X	Proj.No:38405	
Peter Jansweijer	peterj@nikhef.nl	Size A3 4 1 4 A
NIKHEF ©ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Dim 420 x 297 mm
		Page 4 of 4