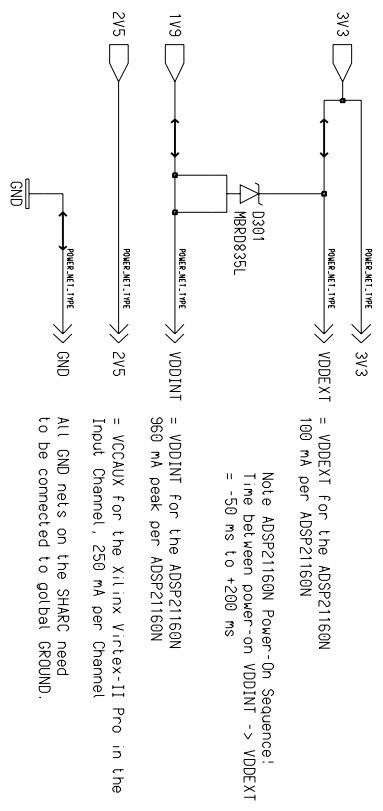
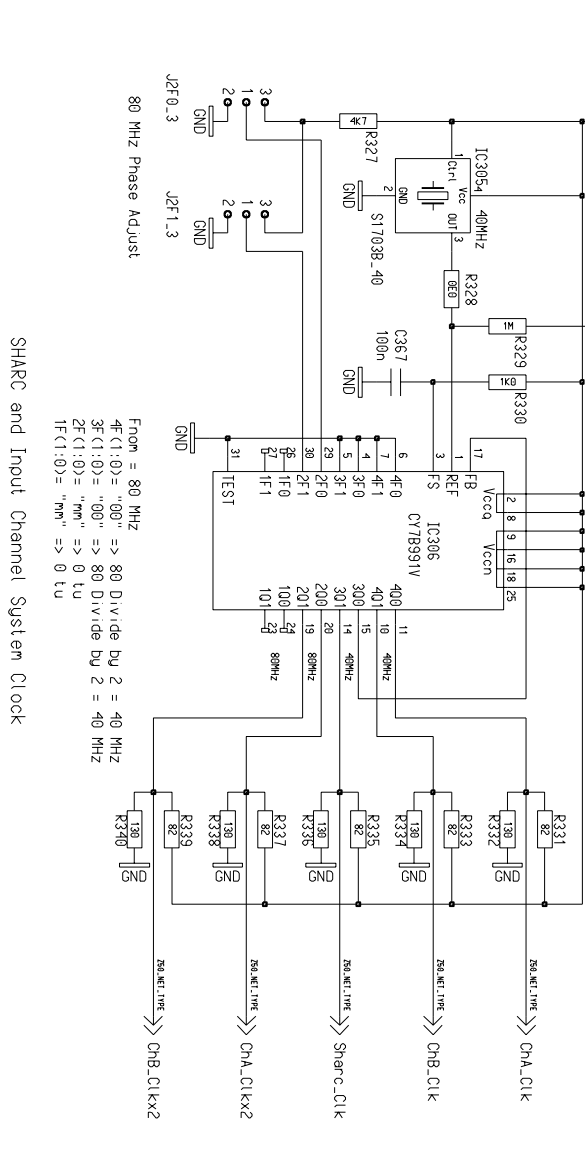
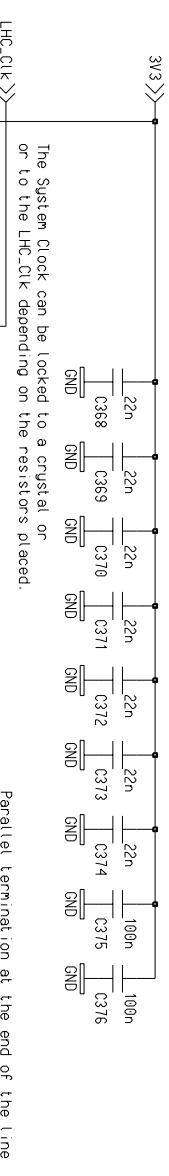
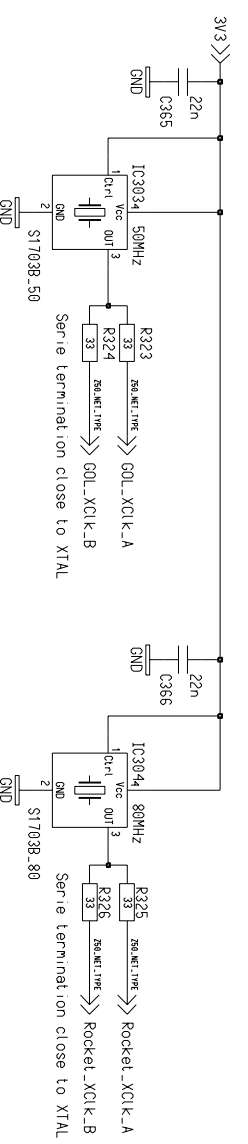


SV\_L0\_11V5\_2  
 1V5 = VCCINT for Xilinx Virtex-II Pro in the Input Channels, 500 mA per Channel  
 VCCINT Ramp rate 200 us min. and 50 ns max.



GOIL Frequency  
 50 MHz 16 bit = 25 MHz 32 bit  
 = 100 MB/s

Rocket-10 Inter-FPGA Link Frequency  
 80 MHz 16 bit = 40 MHz 32 bit  
 = 160 MB/s



A	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
B																		
C																		
D																		
E																		
F																		
G																		
H																		
I																		
J																		
K																		
L																		

MR0D-In		Rev	57
Power and Clocks		Date	26 Jan 2005
Proj: MR0D-X		Time	12:09:03 pm
Peter Jansweijer		Name	peter.j
Proj: No:38405		Size	A3
National Instituut voor Kern-		Dim	420 x 297 mm
Fysica en Hoog-Energie-Fysica		Page	4 of 4
Kruislaan 409, 020-532 2000			
1098 SJ Amsterdam Nederland			

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