IC4004
XC2VP7FF896

GOL_LVDS (DP_GOL_RX2B) — A17, A18; GOL_LVDS (DP_GOL_TX2B) — A19, A20

	A2 VCCAUX	A3 VRP_2	A4	A5	A6	A7	A8	A9 GND	A10	A11	A12	A13	A14	A15 VCCAUX	A16 VCCAUX	A17 GOL_RXN	A18 GOL_RXP	A19 GOL_TXP	A20 GOL_TXN	A21	A22 GND	A23 LEDs(0)	A24	A25	A26	A27	A28 VRP_7	A29 VCCAUX	
B1 VCCAUX	B2 GND	B3 VRN_2	B4 AVCCAUXRX9	B5 VTRXPAD9	B6 AVCCAUXTX9	B7 VTTXPAD9	B8	B9	B10	B11 AVCCAUXRX7	B12 VTRXPAD7	B13 AVCCAUXTX7	B14 VTTXPAD7	B15	B16 GOL_XClk	B17 AVCCAUXRX6	B18 VTRXPAD6	B19 AVCCAUXTX6	B20 VTTXPAD6	B21	B22	B23 LEDs(1)	B24 AVCCAUXRX4	B25 VTRXPAD4	B26 AVCCAUXTX4	B27 VTTXPAD4	B28 VRN_7	B29 GND	B30 VCCAUX
C1	C2	C3 GND	C4	C5	C6 GNDA9	C7	C8	C9	C10	C11	C12 GNDA7	C13	C14 GND	C15	C16	C17 GND	C18 UpLED	C19 GNDA6	C20	C21	C22	C23 LEDs(2)	C24 LEDs(3)	C25 GNDA4	C26 BufA(6)	C27 BufA(7)	C28 GND	C29 BufCE_n	C30 BufA(19)
D1	D2	D3	D4 GND	D5	D6	D7	D8	D9 GND	D10	D11	D12 GND	D13	D14	D15	D16 GOL_RX_LOS	D17 GOL_TX_Disable	D18 ErrLED	D19 GND	D20 GOL_MOD_DEF1	D21 GOL_MOD_DEF0	D22 GND	D23 ChaID(1)	D24 ChaID(0)	D25 DXN	D26 BufD(16)	D27 GND	D28 BufD(33)	D29	D30
E1	E2	E3	E4	E5 GND	E6 VRN_1	E7 VRP_1	E8	E9	E10	E11	E12	E13	E14	E15	E16	E17 GOL_TX_Fault	E18	E19	E20 GOL_MOD_DEF2	E21 GOL_RATE_SEL	E22	E23 ChaID(2)	E24 VRN_0	E25 VRP_0	E26 GND	E27	E28	E29	E30
F1	F2	F3	F4	F5 TDO	F6 GND	F7	F8	F9	F10	F11	F12	F13 GND	F14	F15	F16	F17	F18 GND	F19	F20	F21 TestCon(1)	F22 TestCon(0)	F23	F24	F25 GND	F26 TDI	F27	F28	F29	F30
G1	G2	G3	G4	G5	G6	G7 TCK	G8	G9	G10	G11	G12	G13	G14	G15	G16 Rst_n	G17	G18	G19 TestCon(6)	G20 TestCon(5)	G21 TestCon(4)	G22 TestCon(3)	G23 TestCon(2)	G24 PROG_B	G25 BufD(18)	G26 BufD(17)	G27	G28	G29	G30
H1 GND	H2	H3	H4	H5	H6	H7 VBATT	H8 TMS	H9	H10	H11	H12 TestCon(15)	H13	H14	H15	H16	H17	H18	H19 TestCon(7)	H20 T_Alert_n	H21 SMBData	H22 SMBClk	H23 HSWAP_EN	H24 DXP	H25	H26	H27	H28	H29 BufD(19)	H30 GND
J1	J2	J3	J4	J5	J6	J7	J8 TestCon(14)	J9 VCCO_2	J10 VCCO_1	J11 VCCO_1	J12 VCCO_1	J13 VCCO_1	J14	J15	J16	J17	J18 VCCO_0	J19 VCCO_0	J20 VCCO_0	J21 VCCO_0	J22 VCCO_7	J23 BufD(25)	J24 BufD(24)	J25	J26	J27 BufD(23)	J28 BufD(22)	J29 BufD(21)	J30 BufD(20)
K1	K2	K3	K4	K5	K6	K7	K8	K9 VCCO_2	K10 VCCO_1	K11 VCCO_1	K12 VCCO_1	K13 VCCO_1	K14 VCCO_1	K15 VCCO_1	K16 VCCO_0	K17 VCCO_0	K18 VCCO_0	K19 VCCO_0	K20 VCCO_0	K21 VCCO_0	K22 VCCO_7	K23	K24	K25 BufD(31)	K26 BufD(30)	K27 BufD(29)	K28 BufD(28)	K29 BufD(27)	K30 BufD(26)
L1	L2	L3 GND	L4	L5	L6 GND	L7	L8	L9 VCCO_2	L10 VCCO_2	L11 GND	L12 VCCINT	L13 VCCINT	L14 VCCINT	L15 VCCINT	L16 VCCINT	L17 VCCINT	L18 VCCINT	L19 VCCINT	L20 GND	L21 VCCO_7	L22 VCCO_7	L23	L24	L25 GND	L26 BufA(3)	L27 BufA(4)	L28 GND	L29 BufA(5)	L30 BufD(32)
M1	M2	M3	M4	M5	M6	M7	M8	M9 VCCO_2	M10 VCCO_2	M11 VCCINT	M12 GND	M13 GND	M14 GND	M15 GND	M16 GND	M17 GND	M18 GND	M19 GND	M20 VCCINT	M21 VCCO_7	M22 VCCO_7	M23 BufA(14)	M24 BufA(13)	M25 BufA(12)	M26 BufA(11)	M27 BufA(10)	M28 BufA(0)	M29 BufA(1)	M30 BufA(2)
N1	N2	N3	N4	N5	N6	N7	N8	N9 VCCO_2	N10 VCCO_2	N11 VCCINT	N12 GND	N13 GND	N14 GND	N15 GND	N16 GND	N17 GND	N18 GND	N19 GND	N20 VCCINT	N21 VCCO_7	N22 VCCO_7	N23 BufD(4)	N24 BufD(3)	N25 BufD(2)	N26 BufD(1)	N27 BufD(0)	N28 BufD(35)	N29 BufA(16)	N30 BufA(15)
P1	P2	P3	P4	P5	P6 GND	P7	P8	P9	P10 VCCO_2	P11 VCCINT	P12 GND	P13 GND	P14 GND	P15 GND	P16 GND	P17 GND	P18 GND	P19 GND	P20 VCCINT	P21 VCCO_7	P22 BufD(12)	P23 BufD(11)	P24 BufD(10)	P25 GND	P26 BufD(9)	P27 BufD(8)	P28 BufD(7)	P29 BufD(6)	P30 BufD(5)
R1 VCCAUX	R2	R3	R4	R5	R6	R7	R8	R9	R10 VCCO_2	R11 VCCINT	R12 GND	R13 GND	R14 GND	R15 GND	R16 GND	R17 GND	R18 GND	R19 GND	R20 VCCINT	R21 VCCO_7	R22 BufA(18)	R23 BufA(17)	R24 BufA(8)	R25 BufA(9)	R26 BufD(34)	R27 BufD(15)	R28 BufD(14)	R29 BufD(13)	R30 VCCAUX
T1 VCCAUX	T2	T3	T4	T5 Spare(4)	T6 Spare(3)	T7 Spare(2)	T8 Spare(1)	T9 Spare(0)	T10 VCCO_3	T11 VCCINT	T12 GND	T13 GND	T14 GND	T15 GND	T16 GND	T17 GND	T18 GND	T19 GND	T20 VCCINT	T21 VCCO_6	T22 SDRAM_DQ(6)	T23 SDRAM_DQ(5)	T24 SDRAM_DQ(4)	T25 SDRAM_DQ(3)	T26 SDRAM_DQ(2)	T27 SDRAM_DQ(1)	T28 SDRAM_DQ(0)	T29 BufR_W_n	T30 VCCAUX
U1	U2	U3	U4	U5	U6 GND	U7	U8	U9	U10 VCCO_3	U11 VCCINT	U12 GND	U13 GND	U14 GND	U15 GND	U16 GND	U17 GND	U18 GND	U19 GND	U20 VCCINT	U21 VCCO_6	U22 SDRAM_BA(0)	U23 SDRAM_A(11)	U24 SDRAM_CS_n	U25 GND	U26 SDRAM_RAS_n	U27 SDRAM_CAS_n	U28 SDRAM_WE_n	U29 SDRAM_DQM(0)	U30 SDRAM_DQ(7)
V1 A21_Select	V2	V3	V4	V5	V6	V7	V8	V9 VCCO_3	V10 VCCO_3	V11 VCCINT	V12 GND	V13 GND	V14 GND	V15 GND	V16 GND	V17 GND	V18 GND	V19 GND	V20 VCCINT	V21 VCCO_6	V22 VCCO_6	V23 SDRAM_DQ(17)	V24 SDRAM_DQ(16)	V25 SDRAM_DQM(2)	V26 SDRAM_A(2)	V27 SDRAM_A(1)	V28 SDRAM_A(0)	V29 SDRAM_A(10)	V30 SDRAM_BA(1)
W1 Adr(21)	W2 MS0_n	W3 MS1_n	W4 MS2_n	W5 MS3_n	W6 DMAR_n	W7	W8	W9 VCCO_3	W10 VCCO_3	W11 VCCINT	W12 GND	W13 GND	W14 GND	W15 GND	W16 GND	W17 GND	W18 GND	W19 GND	W20 VCCINT	W21 VCCO_6	W22 VCCO_6	W23 SDRAM_DQ(25)	W24 SDRAM_DQ(24)	W25 SDRAM_DQ(23)	W26 SDRAM_DQ(22)	W27 SDRAM_DQ(21)	W28 SDRAM_DQ(20)	W29 SDRAM_DQ(19)	W30 SDRAM_DQ(18)
Y1 Adr(17)	Y2 Adr(18)	Y3 GND	Y4 Adr(19)	Y5 Adr(20)	Y6 GND	Y7	Y8	Y9 VCCO_3	Y10 VCCO_3	Y11 GND	Y12 VCCINT	Y13 VCCINT	Y14 VCCINT	Y15 VCCINT	Y16 VCCINT	Y17 VCCINT	Y18 VCCINT	Y19 VCCINT	Y20 GND	Y21 VCCO_6	Y22 VCCO_6	Y23	Y24	Y25 GND	Y26 SDRAM_DQ(29)	Y27 SDRAM_DQ(28)	Y28 GND	Y29 SDRAM_DQ(27)	Y30 SDRAM_DQ(26)
AA1 Adr(11)	AA2 Adr(12)	AA3 Adr(13)	AA4 Adr(14)	AA5 Adr(15)	AA6 Adr(16)	AA7	AA8	AA9 VCCO_3	AA10 VCCO_4	AA11 VCCO_4	AA12 VCCO_4	AA13 VCCO_4	AA14 VCCO_4	AA15 VCCO_4	AA16 VCCO_5	AA17 VCCO_5	AA18 VCCO_5	AA19 VCCO_5	AA20 VCCO_5	AA21 VCCO_5	AA22 VCCO_6	AA23	AA24	AA25 SDRAM_A(5)	AA26 SDRAM_A(4)	AA27 SDRAM_A(3)	AA28 SDRAM_DQM(3)	AA29 SDRAM_DQ(31)	AA30 SDRAM_DQ(30)
AB1 Adr(7)	AB2 Adr(8)	AB3 Adr(9)	AB4 Adr(10)	AB5	AB6	AB7	AB8	AB9 VCCO_3	AB10 VCCO_4	AB11 VCCO_4	AB12 VCCO_4	AB13 VCCO_4	AB14	AB15 Data(3)	AB16 IRQ2_n	AB17	AB18 VCCO_5	AB19 VCCO_5	AB20 VCCO_5	AB21 VCCO_5	AB22 VCCO_6	AB23	AB24	AB25	AB26	AB27 SDRAM_A(9)	AB28 SDRAM_A(8)	AB29 SDRAM_A(7)	AB30 SDRAM_A(6)
AC1 GND	AC2 Adr(4)	AC3 Adr(5)	AC4 Adr(6)	AC5	AC6	AC7 CCLK	AC8 DONE	AC9 D0	AC10 Data(16)	AC11 Data(11)	AC12 Data(9)	AC13	AC14	AC15 Data(2)	AC16 IRQ1_n	AC17	AC18	AC19 TestCon(8)	AC20 TestCon(9)	AC21 TestCon(10)	AC22 D7	AC23 M2	AC24 M1	AC25	AC26	AC27 SDRAM_DQM(1)	AC28 SDRAM_A(12)	AC29 SDRAM_CKE	AC30 GND
AD1	AD2	AD3	AD4	AD5 Adr(2)	AD6 Adr(3)	AD7 PWRDWN_B	AD8	AD9 D1	AD10 Data(15)	AD11 Data(10)	AD12 Data(8)	AD13	AD14 Data(7)	AD15 Data(1)	AD16 IRQ0_n	AD17	AD18	AD19 TestCon(11)	AD20 TestCon(12)	AD21 TestCon(13)	AD22 D6	AD23	AD24 M0	AD25 SDRAM_DQ(9)	AD26 SDRAM_DQ(8)	AD27	AD28	AD29	AD30
AE1	AE2	AE3	AE4	AE5	AE6 GND	AE7 Data(25)	AE8 Data(24)	AE9 Data(20)	AE10 Data(14)	AE11	AE12	AE13 GND	AE14 Data(6)	AE15 Data(0)	AE16 Empty	AE17	AE18 GND	AE19	AE20	AE21	AE22	AE23	AE24	AE25 GND	AE26	AE27	AE28	AE29	AE30
AF1	AF2	AF3	AF4	AF5 GND	AF6	AF7 INIT_B	AF8 Data(23)	AF9 Data(19)	AF10 Data(13)	AF11	AF12	AF13	AF14 Data(5)	AF15 SDRAM_CLKin	AF16 SDRAM_CLK	AF17	AF18	AF19	AF20	AF21 TTC_n(7)	AF22 TTC_n(6)	AF23 TTC_n(4)	AF24 RDWR_B	AF25	AF26 GND	AF27	AF28	AF29	AF30
AG1 Data(30)	AG2 Data(31)	AG3 Adr(0)	AG4 GND	AG5 Adr(1)	AG6 DOUT	AG7 D2	AG8 VRP_4	AG9 GND	AG10 Data(12)	AG11	AG12 GND	AG13	AG14 Data(4)	AG15 SharcWr_n	AG16 LHC_Clk	AG17 ChaBusy	AG18	AG19 GND	AG20	AG21 TTC_n(5)	AG22 GND	AG23 VRN_5	AG24 D5	AG25 CS_B	AG26 SDRAM_DQ(13)	AG27 GND	AG28 SDRAM_DQ(12)	AG29 SDRAM_DQ(11)	AG30 SDRAM_DQ(10)
AH1 Data(26)	AH2 Data(27)	AH3 GND	AH4 Data(28)	AH5 Data(29)	AH6 GNDA16	AH7 D3	AH8 VRN_4	AH9 Data(18)	AH10	AH11	AH12 GNDA18	AH13	AH14 GND	AH15 SharcRd_n	AH16 Clk	AH17 GND	AH18	AH19 GNDA19	AH20	AH21	AH22 TTC_n(3)	AH23 VRP_5	AH24 D4	AH25 GNDA21	AH26	AH27	AH28 GND	AH29 SDRAM_DQ(15)	AH30 SDRAM_DQ(14)
AJ1 VCCAUX	AJ2 GND	AJ3 VRP_3	AJ4 AVCCAUXRX16	AJ5 VTRXPAD16	AJ6 AVCCAUXTX16	AJ7 VTTXPAD16	AJ8 Data(22)	AJ9 Data(17)	AJ10	AJ11 AVCCAUXRX18	AJ12 VTRXPAD18	AJ13 AVCCAUXTX18	AJ14 VTTXPAD18	AJ15 Rocket_XClk	AJ16 Clkx2	AJ17 AVCCAUXRX19	AJ18 VTRXPAD19	AJ19 AVCCAUXTX19	AJ20 VTTXPAD19	AJ21	AJ22 TTC_n(2)	AJ23 TTC_n(1)	AJ24 AVCCAUXRX21	AJ25 VTRXPAD21	AJ26 AVCCAUXTX21	AJ27 VTTXPAD21	AJ28 VRP_6	AJ29 GND	AJ30 VCCAUX
	AK2 VCCAUX	AK3 VRN_3	AK4	AK5	AK6	AK7	AK8 Data(21)	AK9 GND	AK10	AK11	AK12	AK13	AK14	AK15 VCCAUX	AK16 VCCAUX	AK17 Rocket_RXN	AK18 Rocket_RXP	AK19 Rocket_TXP	AK20 Rocket_TXN	AK21	AK22 GND	AK23 TTC_n(0)	AK24	AK25	AK26	AK27	AK28 VRN_6	AK29 VCCAUX	

ROCKET_LVDS T — AK17, AK18; ROCKET_LVDS S — AK19, AK20

Input FPGA Power pins:
VCCAUX (2V5) 16 pins
VCCINT (1V5) 32 pins
VCCO_# (3V3) 10 pins each
GND 124 pins

channel_in	Rev 56
Input FPGA	Date 26 Jan 2005
Proj: MROD-X / Proj.No:38405	Time 12:09:48 pm
Peter Jansweijer / peterj@nikhef.nl	Name peterj
NIKHEF — NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA, KRUISLAAN 409, 020-592 2000, 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
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