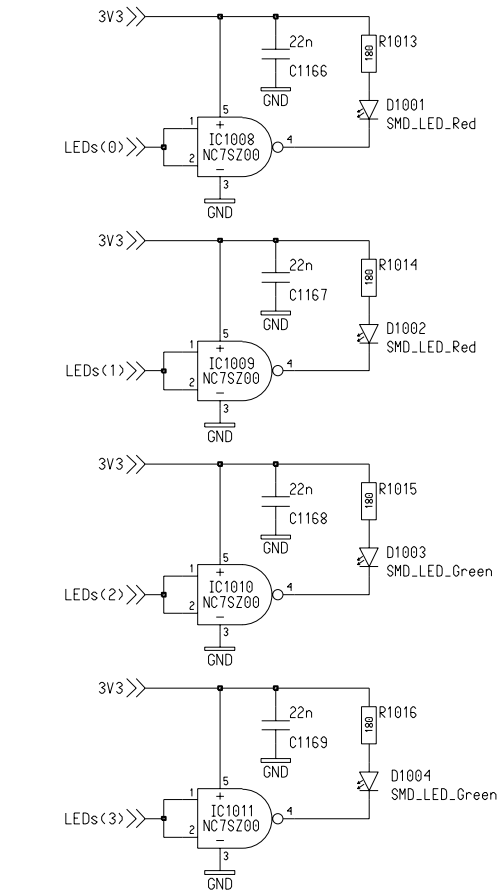
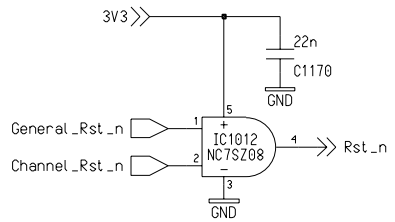
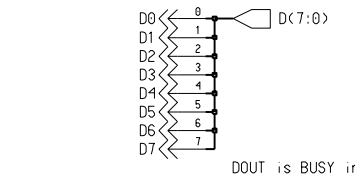


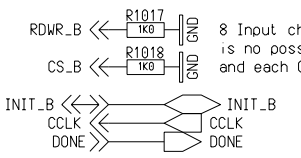


Fiducial1001 Fiducial1002

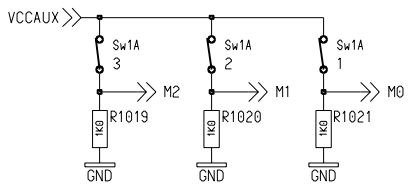


DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices.
See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SlectMAP programming Mode -> BUSY.
Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!

DOUT



8 Input channels are loaded in parallel so there is no possibility for readback (RDWR_B = '0') and each CS_B = '0'



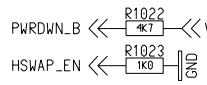
M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.

PROG_B

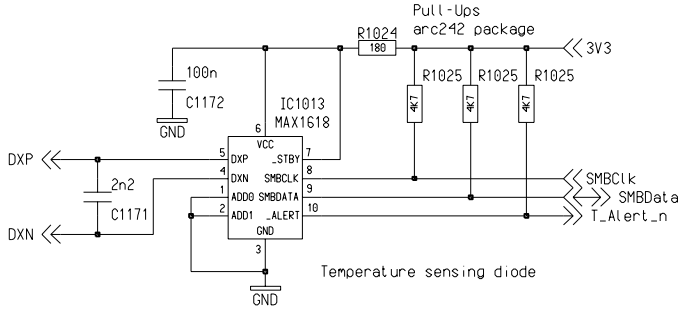
FPGA Configuration Signals



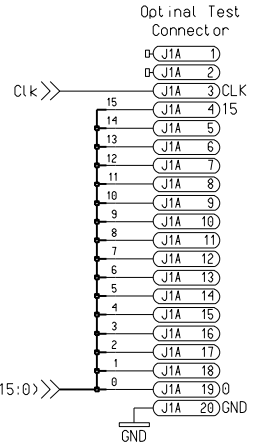
PWRDWN_B is unsupported (should be pulled high)

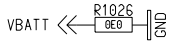
HSWAP_EN = '0' => User IOs have pull-up resistors during configuration

Pull-Ups
arc242 package



Temperature sensing diode





VBATT is decriptor key memory backup supply

FPGA Control signals

A21_Select
Adr(21:0)
Data(31:0)

MS0_n
MS1_n
MS2_n
MS3_n

SharcRd_n
SharcWr_n

IRQ0_n
IRQ1_n
IRQ2_n

Empty
DMAR_n

Sharc Signals

ChaID(2:0)

Input Channel ID bits

Rocket_XClk
Rocket_RXP
Rocket_RXN
Rocket_TXP
Rocket_TXN

Frontend to Backend
Rocket IO Signals

ChaBusy

TTC_n(7:0)
LHC_Clk

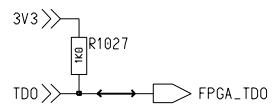
TTC Signals

Clk
Clkx2

Clock Signals

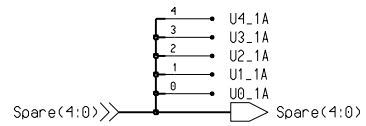
TCK
TMS
TDI

FPGA_TCK
FPGA_TMS
FPGA_TDI



FPGA JTAG Signals

Testpoints force Spare lines to be accessible.



channel_in	Rev 80
Input FPGA Auxiliary Connections	Date 26 Jan 2005
Proj: MROD-X / Proj.No:38405	Time 12:11:01 pm
Peter Jansweijer / peterj@nikhef.nl	Name Peter Jansweijer
NIKHEF ©ET-Nikhef Amsterdam — NATIONAAL INSTITUUT VOOR KERNFYSICA EN HOGE ENERGIE-FYSICA, KRUISLAAN 409, 020-592 2000, 1098 SJ AMSTERDAM NEDERLAND	Size A3 / 4 1 4 A
	Dim 420 x 297 mm
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