ATLAS Muon MDT

MROD Module:

MROD-X Pre-Production Series Test Report

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Abstract

Fifteen pre-production modules were produced. This document describes the issues found during testing.

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1 Introduction

Fifteen pre-production MROD-X modules were produced at PCB Technologies LTD, Israel. All MROD-X modules were of type “6 channel without SHARC-B”.

The modules have been given serial numbers 10-24.

This document describes all the issues found during testing. It may seem that a lot of things went wrong but one should keep in mind that the complexity of the assembled boards is very high. An awful lot of connections should be in perfect shape. If just one single connection on a module fails then the module will not pass the test…

Overall the quality of the soldering joints is very well. Another achievement is that all BGA devices on the fifteen pre-production modules (a total of 15 * 4 = 60, 400-ball devices and 15 * 7 = 105, 896-ball devices) are assembled correctly!

2 First inspection

2.1 Packaging

To ship the MROD-X modules, specially made boxes were ordered in Great-Britain. At the time the fifteen pre-production modules had to be shipped via Geneva to Amsterdam, these boxes were still held at the Israeli customs. Thus it has been agreed not to hold the shipment and to pack the first fifteen modules in another way.

The way the modules were packed was not adequate. Both boxes were subjected to quite some external force which caused them to rip open (figure 1 and 2).

Figure 1: Box ripped open

Figure 2: Other box also ripped open

2.2 Front panel damage

As a result of the poor packaging the front panel of one module was severely damaged (figure 3).

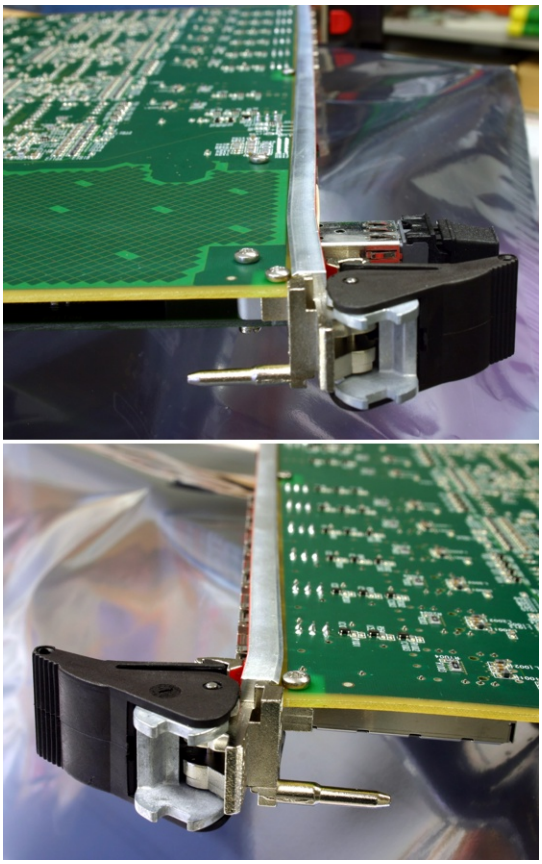

Figure 3: Damaged front panel

2.3 Optical transceivers not mounted

The optical transceivers that should have been assembled were missing on the modules. This issue was quickly solved by PCB Technologies when they sent 90 transceivers (15 modules times 6 transceivers per module) to Amsterdam

2.4 Fuses poorly soldered

Before a closer inspection of the soldering joints, the eye was caught by the soldering joints of the fuses (see figure 4). It should be noted that these fuses are not made to be used as surface mount devices. However, the excessive currents drawn force us to solder the devices directly onto the board, rather then to use a fuse-holder that would cause too much contact resistance.

When heating the fuses, the end-caps tend to be blown off by the expanding hot air inside the fuse. So one need to find an optimum in reflowing the solder and trying to keep the end-caps in place.

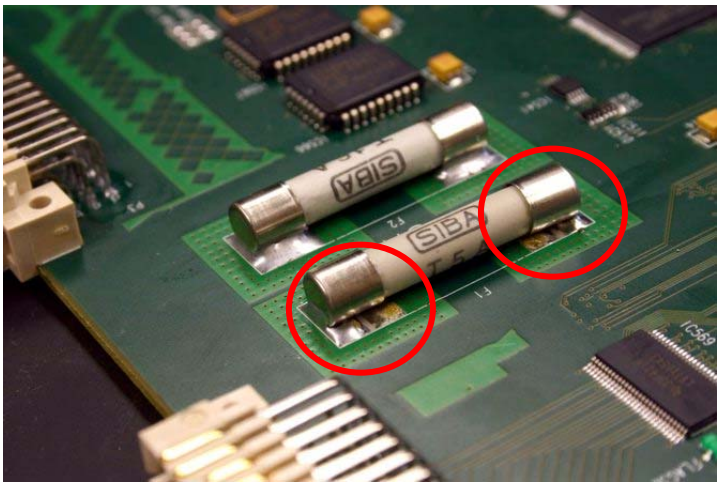

Figure 4: poorly soldered fuses

2.5 Mechanically mounting of P1, P2 and P3

Originally it was asked to mechanically fix the P1, P2 and P3 connectors with rivets. Figure 5 for example, shows how the connectors on our proto type series were mounted.

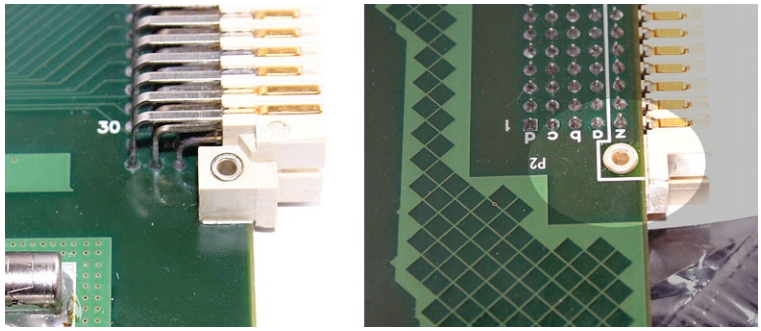

Figure 5: this example shows how the connectors on the prototype (not assembled by PCB Technologies) was mounted with rivets

When the boards were already assembled it became clear that PCB Technologies could not supply these rivets. It has been agreed to ship the pre-production series without a mechanical fixation on P1, P2 and P3 and to fix the connectors in Amsterdam.

For the main series one should first mechanically fix the connectors and than solder the connectors. The other way around may cause stresses in the soldering joint that could cause it to malfunction over time.

3 Closer inspection

As already mentioned in the introduction, the overall quality of the soldering joints is very high. We have put some modules under a microscope to see how the joints look. Perfect work!

A few critical SMD components were checked before the module was put into the VME crate for further testing. These components include special resistors that configure board 'settings' (6 or 8 channel module; yes/no SHARC-B present) and feedback resistors for the power supplies.

3.1 Special resistors

There are 6 resistors that configure the MROD to be a 6 or 8 channel module with or without a SHARC-B processor. As pointed out in the "assembly notes" and the "assembly list", the Mentor Graphics database contains the values for a full featured module (8 channel with SHARC-B). However, the production MROD-X will be of type 6 channel, without SHARC-B.

Pictures of the wrongly placed resistors were made (figures 6 to 9 below)

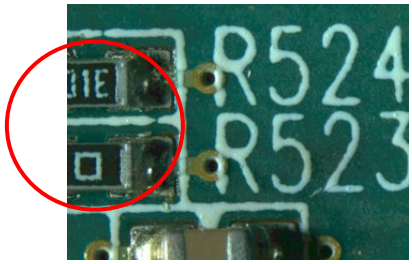

Figure 6: R523 should be 1M (not 0Ω) and R524 should be 0Ω (not 1M)

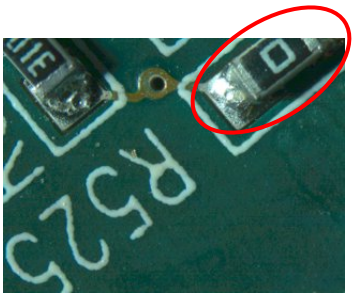

Figure 7: R525 should be 1M (not 0Ω)

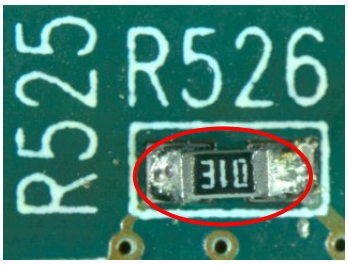

Figure 8: R526 should be 0Ω (not 1M)

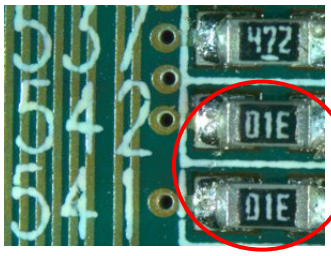

Figure 9: R541 = should be 4K7 (not 1M) and R542 = should be 4K7 (not 1M)

3.2 Power supply feedback resistors

There are many (switched mode) power supplies on the board. The feedback resistors need to have the proper values to avoid over-voltage on the FPGAs or SHARC processors. All resistors had the proper value, except for one. It seems that there was a wrong tape placed on the machine since for all 100 ohm resistors, 10 ohm resistors were placed instead. This involves 15 resistors per module (R605, R608, R609, R610, R719, R720, R721, R1006, R2006, R3006, R4006, R5006, R6006, R7006, R8006)

The proper EIA-96 marking for a 100 ohm smd resistor should read “01A”. However resistors with marking “100” were placed. This is not an EIA-96 marking and should be read as 10 times 10 to the power of 0, thus 10 ohm (see figure 10).

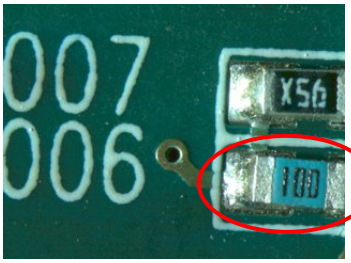

Figure 10: A 10 ohm resistor!

4 Assembly errors found

4.1 General

The MROD module contains an awful lot of connections. If just one single connection on a module fails then the module will not pass the test…

In the pre-production series we have found 8 individual assembly errors.

Below the failures that were encountered in the pre-production series are shown. The pictures below are made with a microscope which is only capable to make pictures from a strait angle. These straight angle pictures might not look very convincing because in order to find solder joints that are not soldered properly it is absolutely necessary to view under an angle. Some pictures are made with a mirror, trying to reach this effect.

4.2 Module 12, IC548 has wrong orientation

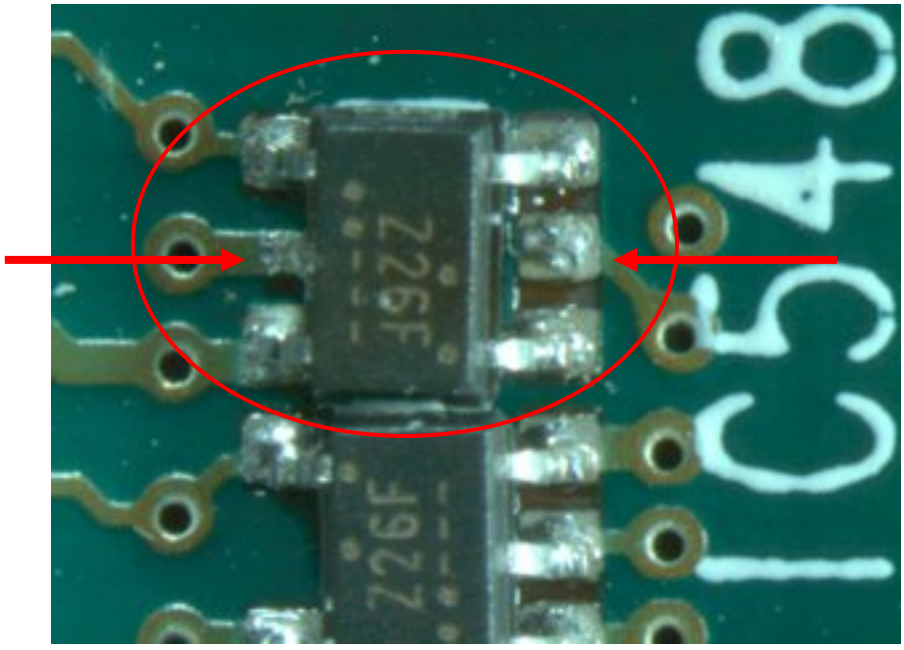

Figure 11: IC548 orientation 180 degrees

This error is most peculiar since the NC7SZ126P5X is delivered in a tape. In the factory these devices are automatically packed into this tape so it is not likely that a device is taped with the wrong orientation… What happened here?

4.3 Module 12, Pad R204 was not soldered propely

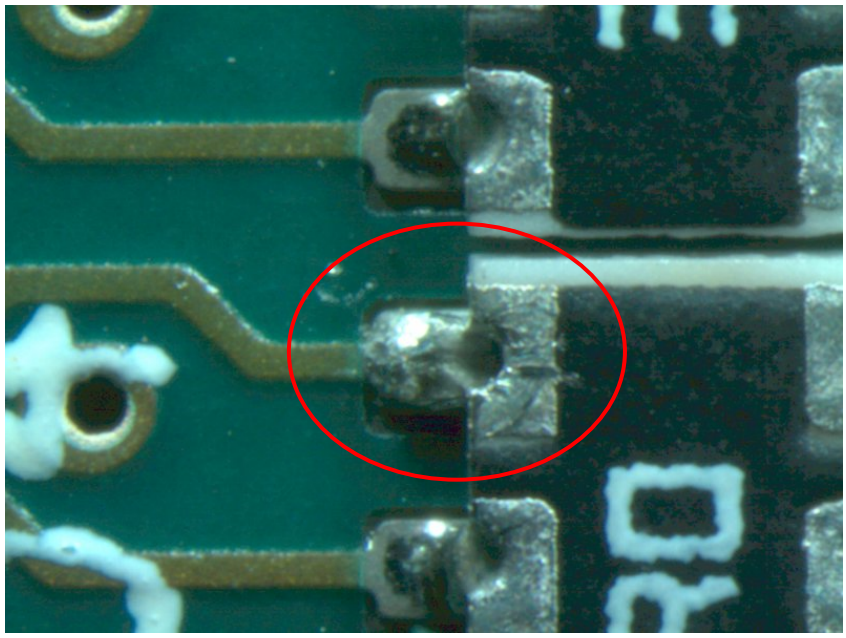

Figure 12: R204 pad not soldered propely

4.4 Module 14, IC588 pin 1 and 5 not soldered properly

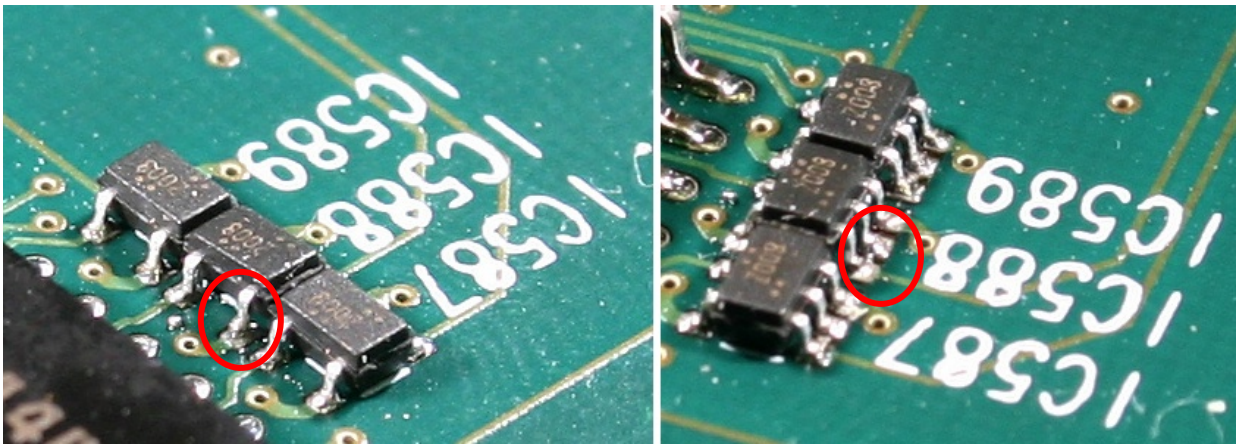

Figure 13: IC588 pin 1 and 5 above the PCB and not soldered

This fault is caused by the package of the NC7SZ00P5X which is not really flat on the PCB thus causing the pins to stand off from the PCB surface.

This seems to be a problem area on the board because the packages are too close together. See also paragraph 4.7. Extra attention is needed to make sure that these ICs are properly soldered.

4.5 Module 16, J24 pin 2 is not soldered

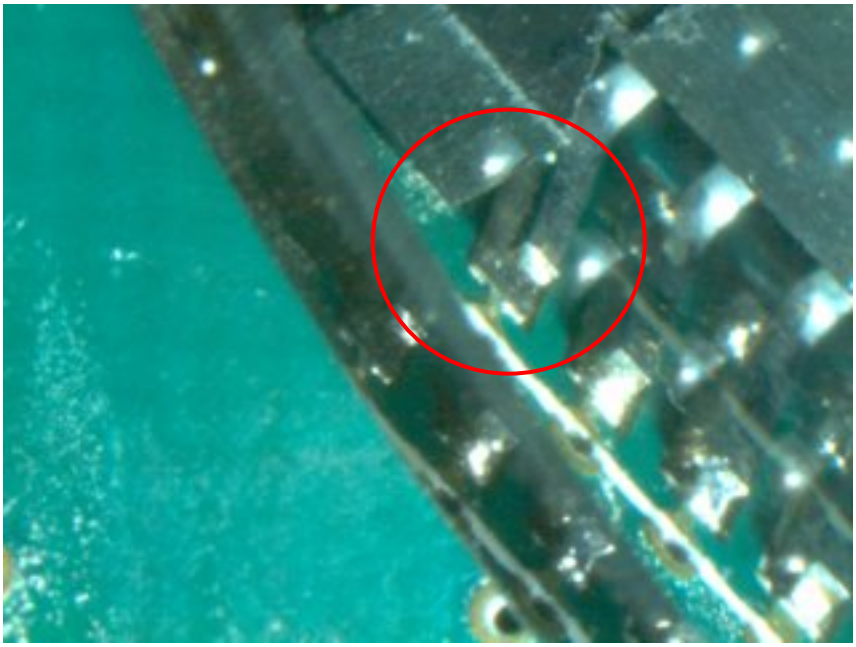

Figure 14: J24 pin 2 is not soldered

This fault is caused by the connector which is not really flat on the PCB thus causing the pin to stand off from the PCB surface. Note the picture was made using a mirror.

4.6 Module 18, SFP Connector IC2001 Loose pin 19

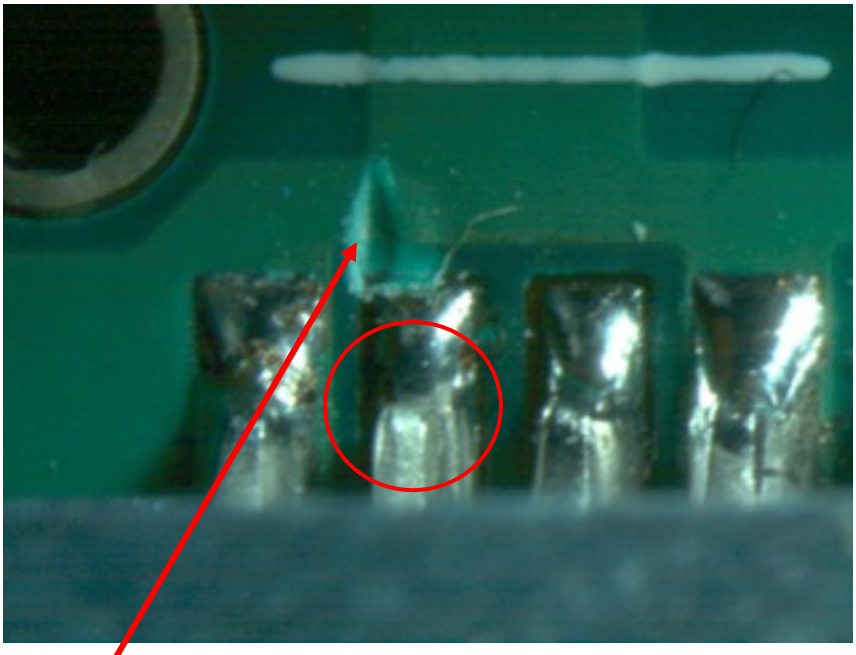

Figure 15:Loose pin 19 on connector IC2001

This is caused by the screw driver, used unlock the cage…

4.7 Module 21, IC588 pin 3 was not soldered properly

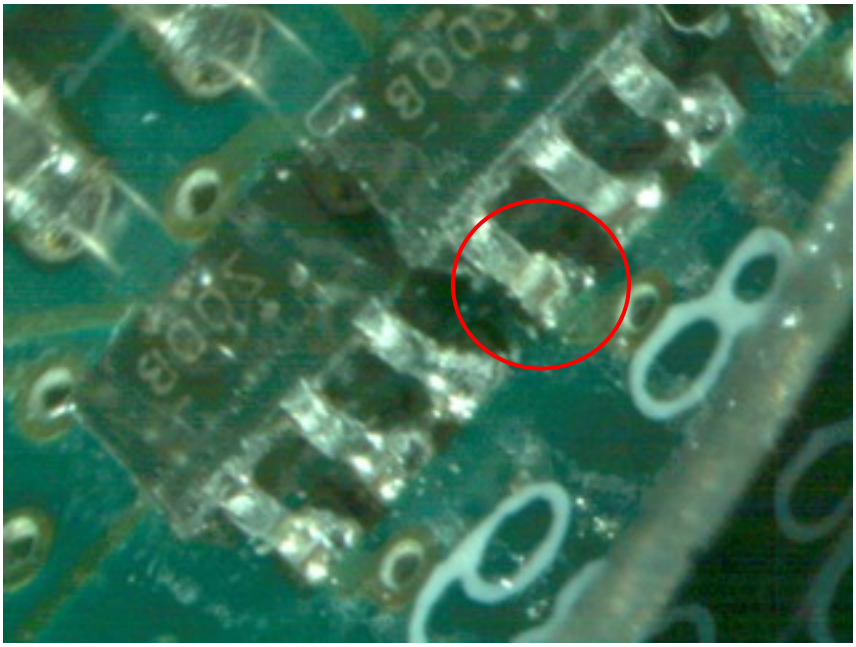

Figure 16: IC588 pin 3 not soldered

Mind the blurred picture; it was made using a mirror. This fault is caused by the package of the NC7SZ00P5X which is not really flat on the PCB thus causing the pins to stand off from the PCB surface.

This seems to be a problem area on the board because the packages are too close together. See also paragraph 4.4. Extra attention is needed to make sure that these ICs are properly soldered.

4.8 Module 22, IC548 pin 2 was not soldered properly

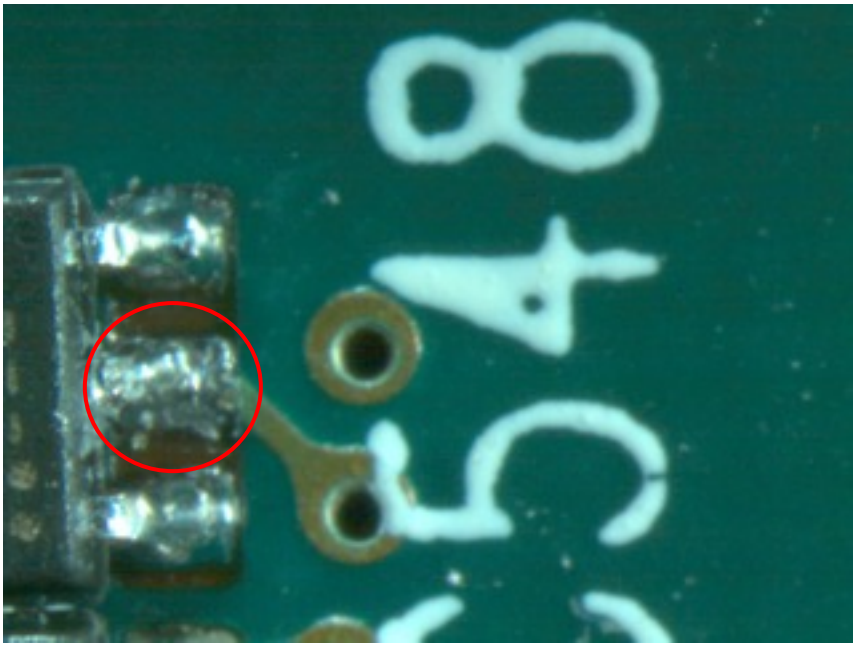

Figure 17: IC548 pin 2 not soldered

This is one of the errors that would have been difficult to find for an Automatic Optical Inspection.

4.9 Module 24: IC305 has wrong orientation

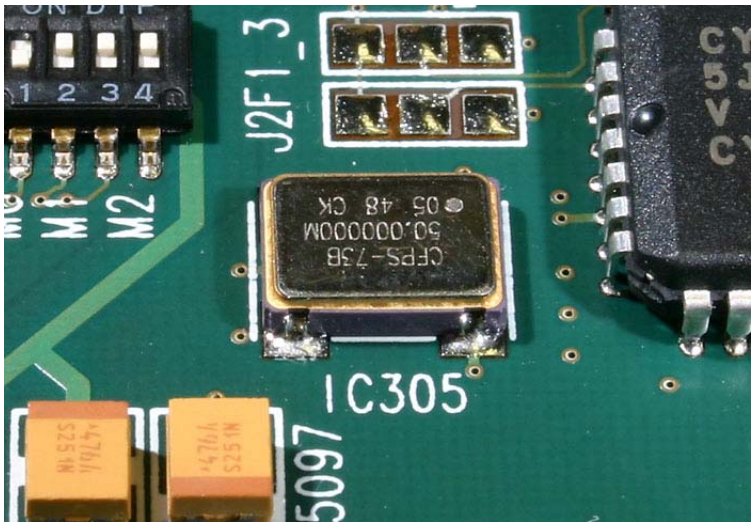

Figure 18: IC305 has wrong orientation

4.10 Conclusions

In the pre-production series 8 individual assembly errors were found. For 15 modules this gives a yield of some 50% which is apparently too low for the main series. The message therefore is: "**the assembly house did a good job, but they need to do better**".

Before starting the pre-production series the options of Automatic Optical Inspection (AOI) were discussed. It has been agreed that AOI was not necessary since the amount of expected failures would be very low. However, the amount of failures found in the pre-production series show clearly that something needs to be done to raise the yield. Therefore we recommend AOI for the main series in order to lower the failure rate considerably.

5 Design issues due to new insight from the pre-production series

5.1 FPGA configuration bus

With the prototype series of MROD-X modules (V1a) it was found that the configuration bus of the MROD-In FPGAs needed parallel termination on the end of the clock and data lines. This was corrected for the (pre-production) series of MROD-X modules (V2).

However, certain modules (V2) sometimes did not configure properly. Investigation of the configuration bus data bits shows that the signals marginally come below 0.8 Volt (see figure 19).

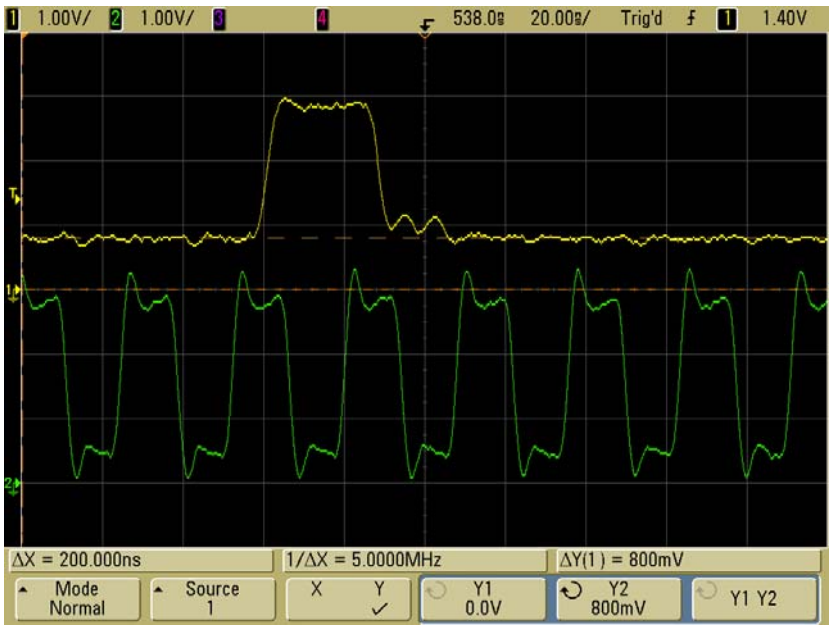

Figure 19: Trace 1: MRI_D4; Trace 2: MRI_CCLK (@ 40 MHz), Cursors at 0.8 Volt. Termination 3V3 -> 82 ohm -> MRI_D4 -> 130 ohm -> Ground

It was chosen to remove the termination resistors (R676a-h, R677a-h) for the data bits and to lower the configuration frequency from 40 to 20 MHz to avoid the reflections on the lines. In fact this same scheme was used successfully on the six prototype modules (V1a).

On the proto type modules (V1a), the clock line was terminated in a 100/100 ohm fashion. For the pre-production (V2) series it was chosen to use a more conventional TTL scheme of 82/130 ohm (resistors R672 and R675). The Thevenin equivalent voltage for this termination is 2 Volt which turns out to be too high since the sink capability of the drivers in the configuration PROM (XCF08P) is not very strong. Therefore the termination scheme was changed to 130/82 ohm which has a Thevenin equivalent voltage of 1.2 Volt. The resulting clock signal can be seen in figure 20.

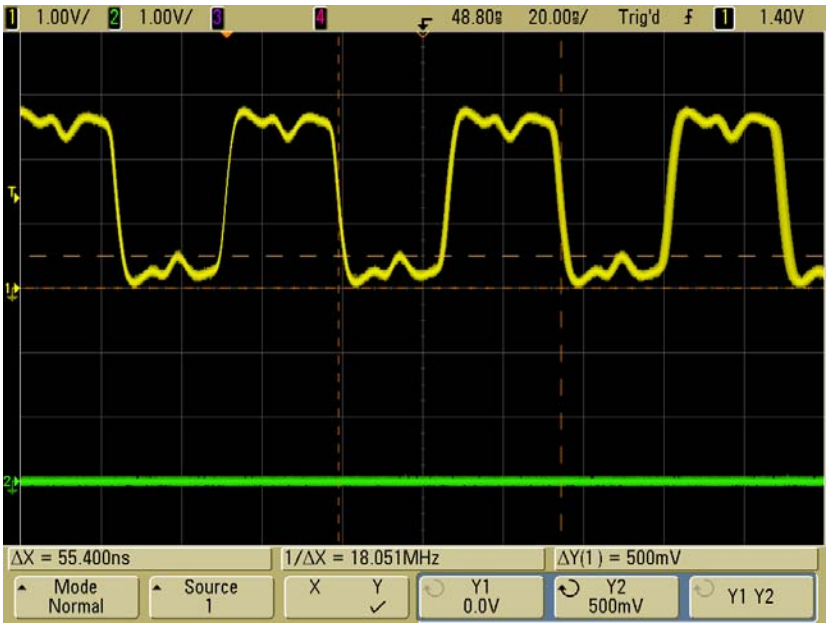

Figure 20: Trace 1: MRI_CCLK (@ 20 MHz), Cursors at 0.5 Volt. Ternmination 3V3 -> 130 hm -> MRI_CCLK -> 82 ohm -> Ground. MRI_CCLK low level stays below 0.5 V

5.2 Test pattern generator trigger

While trying to start a duration test with the MROD-X built in test pattern generator, it was found that the L1-Accept trigger signal that is supplied by the TIM module was not properly interpreted by the FPGA from Channel 2B.

After thorough inspection the problem was reduced to the termination of the LHC_Clk2 line. The FPGA input appears to be very sensitive in the 1.2 Volt region. On the falling edge, a hick-up can be seen (figure 22 below). This hick-up sometimes confuses the flags of the "ttc_bus_bit_fifo_1x15". This FIFO (internal in the FPGA) is used as a bridge for the L1A signal from the LHC-Clock domain to the MROD-In system-clock domain. When the flags of this FIFO get confused then the FIFO behaves like "falling through the empty flag", thus generating 16 spurious triggers on its output (figure 21).

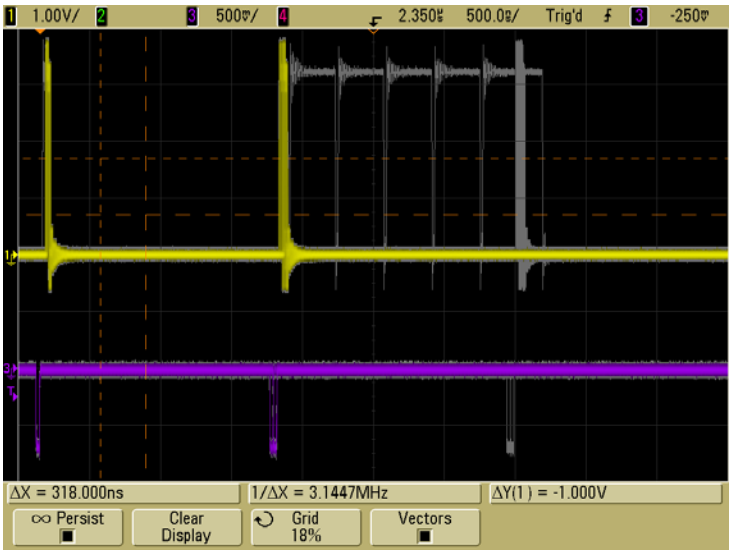

Figure 21: spurious triggers on the output of the ttc_bus_bit_fifo_1x15 (internal in the FPGA)

The hick-up on the LHC_Clk2 line is not caused by a termination problem. The whole line is perfectly 50 ohms which was measured by a Time Domain Reflectometry (TDR). This shows that the Printed Circuit Board was manufactured with great care! The TDR also showed that the trace length is 4.4 ns (80 cm). The hick-up is caused by loss (in the FR4 material) of high frequency components and capacitive loading on the FPGA input pins.

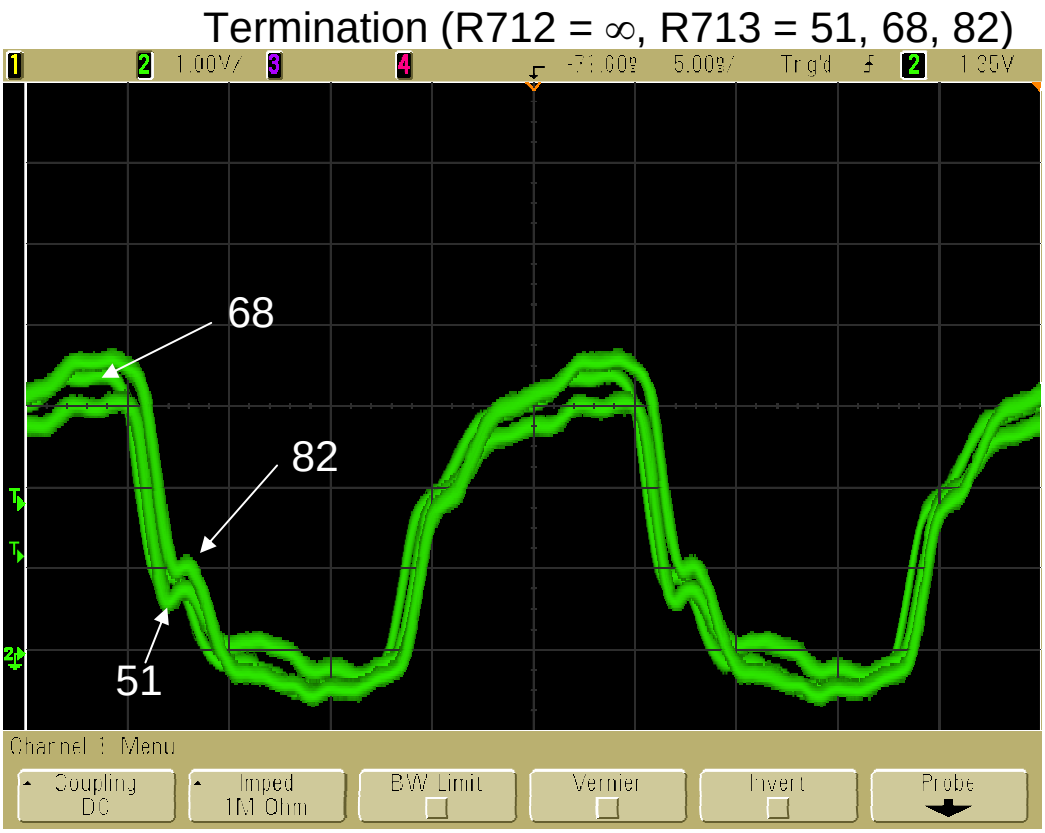

Figure 22: Hick-up in the LHC_Clk2

The LHC_Clk2 signal was compared the other LHC_Clk signals for the other FPGAs on the module as well as the same signal found on the prototype series (V1a). The signals found are comparable although the phenomena is only present on the pre-production series (V2), only on Channel 2B. This shows how marginally this signal is. Differences is trace routing (as compared to the other MROD input channels) or differences in Printed Circuit Board material and/or another batch of FPGAs (as compared to the proto-type series) can explain this behavior.

To solve this problem, the termination of the LHC_Clk lines was changed. The best results are obtained when a resistor is placed to ground thus the Thevenin equivalent voltage is zero in order to get the hick-up as far as possible from the 1.2 V region. Resistors of 82, 68 an 51 ohm all worked fine but 51 ohm is chosen since it is closest to the trace impedance and farthest from the 1.2 V region.

It was checked that the RoboClocks (CY7B9911V) can drive this kind of termination. When the PLL inside the RoboClock is not started (i.e. there is no TIM driving the LHC-Clock in the crate) the clock lines are driven low.

5.3 EMC Gasket

The EMC gaskets that were supplied (RITTAL Number 3686979) are of inferior quality. The springs of the gasket sometimes rip-off components of neighboring boards during insertion or extraction of the modules in the VME crate. There is a new type of gasket (RITTAL Number 3688616) which is made of one piece which does not have this problem.

New EMC gaskets will be ordered and mounted in Amsterdam. To avoid extra work the inferior EMC gaskets (3686979) should not be assembled by PCB Technologies, but returned with the spare components after the complete assembly of the series.

5.4 Connector J22 should not be placed

The fifteen pre-production modules all have a 2x5 pin boxed header placed for J22 (see figure 23) as was wrongly specified in the “assembly list”. For the series we kindly ask **not** to place these connectors.

Note that there were 275 2x5 pin boxed headers delivered to PCB Technologies (for mounting J21 = item 24). This amount included 20 spare connectors. For the pre-production series there are 15 connectors placed (for J22) so the amount of spare connectors is now reduced to 5.

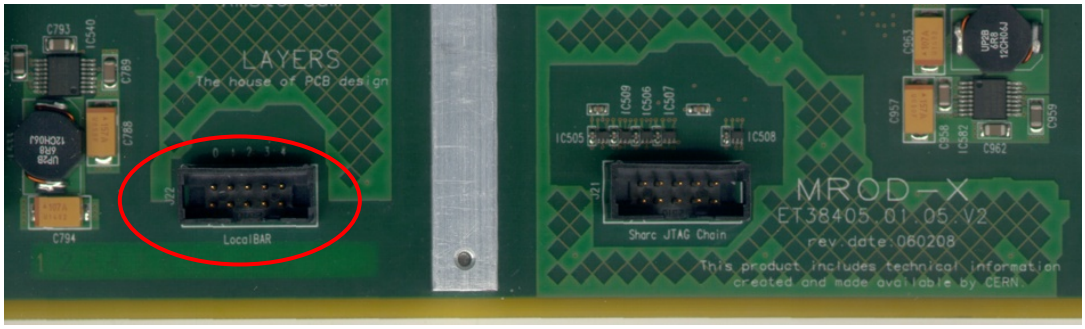

Figure 23: J22 should not have been placed

Appendix: Assembly instruction summary

The most important list of this report:

Improve packaging; Boxes broken (Front panel suffered)

Assemble optical-transceivers

Improve soldering of the Fuses. Try to keep the end-caps in place while reflowing the solder.

Mechanically fix P1, P2 and P3 before soldering

Do not assemble the EMC Gaskets (RITTAL Number 3686979)

Don't place J22 (Bar jumper 2x5)

Pay special attention to IC588 area

Use Automatic Optical Inspection (AOI) of the assembled boards to lower the failure rate

R523 should be 1M (not 0Ω)

R524 should be 0Ω (not 1M)

R525 should be 1M (not 0Ω)

R526 should be 0Ω (not 1M)

R541 = should be 4K7 (not 1M)

R542 = should be 4K7 (not 1M)

R605, R608, R609, R610, R719, R720, R721, R1006, R2006, R3006, R4006, R5006, R6006, R7006, R8006 should be 100 ohm (not 10Ω)

New remarks due to new insights from pre-production series:

Don't place R676a, R676b, R676c, R676d, R676e, R676f, R676g, R676h

Don't place R677a, R677b, R677c, R677d, R677e, R677f, R677g, R677h

Place R672 130 ohm (not 82)

Place R675 82 ohm (not 130)

Don't place R710, R712, R714, R716

Place R711, R713, R715, R717 = 51 ohm (not 130)

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