Preparatory Design Studies
MROD-X

- Use Xilinx Virtex II Pro
  - RocketIO
  - PowerPC
  - Port the current MROD-In design from Altera to Xilinx

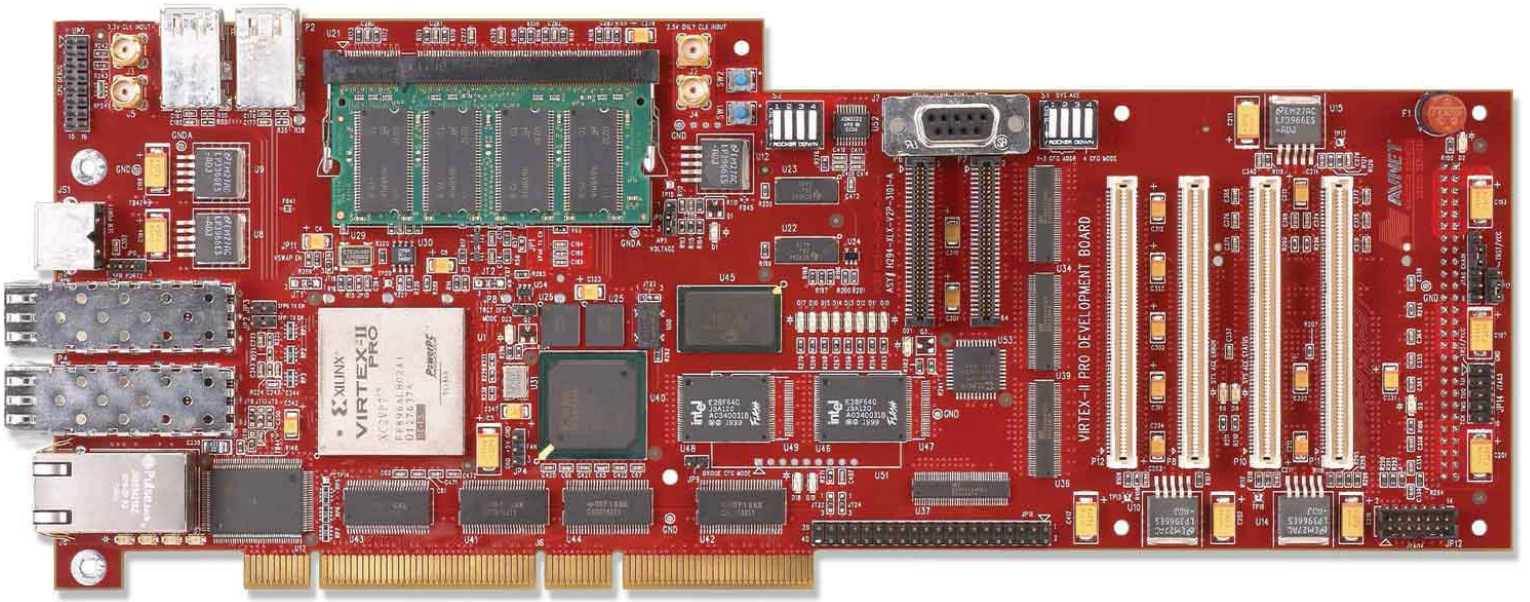
MROD-In design from Altera to Xilinx

Altera APEX20K200EQC240-1	Xilinx XC2VP7FG456-7
• Total logic elements – 5605 / 8320 (67 %)	• Number of SLICEs – 2898 out of 4928 (58%)
• Total ESB bits – 15360 / 106496 (14 %)	• Number of RAMB16s – 3 out of 44 (6%)
• Total pins – 168 / 171 (98 %)	• Number of External IOBs – 168 out of 248 (67%)

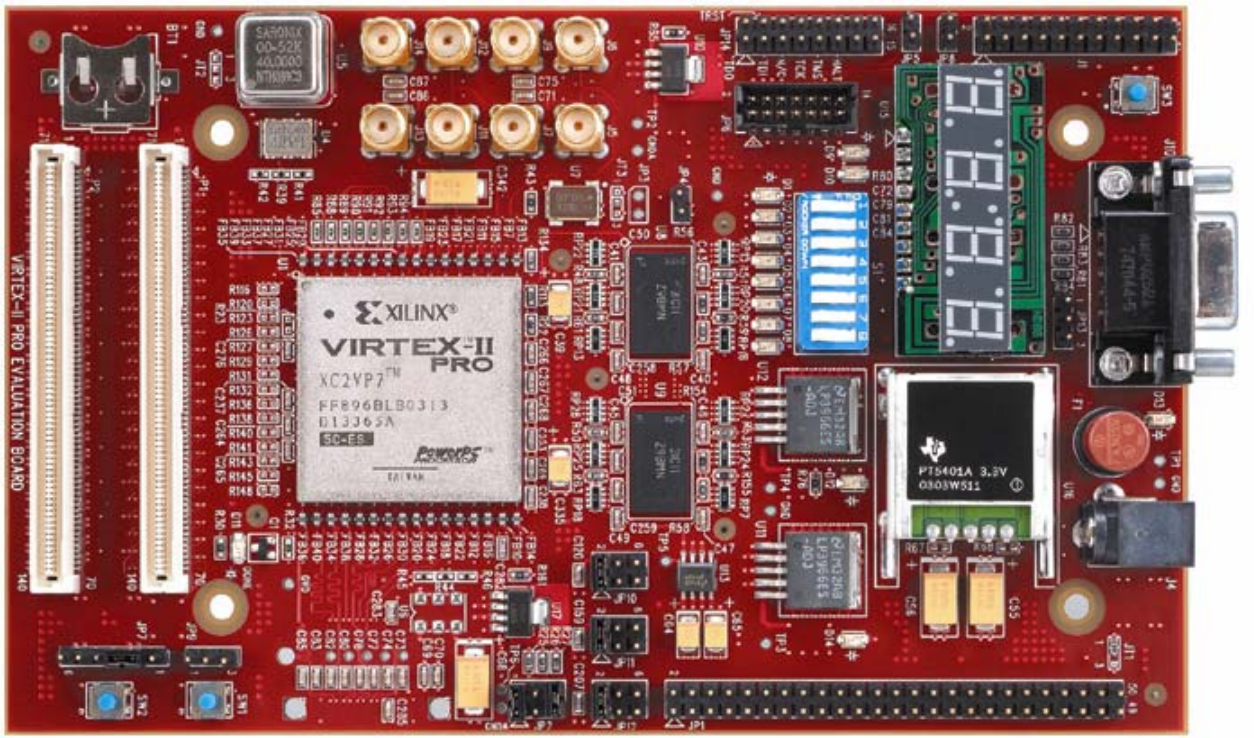
Note 1: Rule of thumb **70 % = FULL.** If you try to put more in your FPGA then you'll probably face routing and timing problems!

Note 2: 1 Xilinx "SLICE" (~ 2 "Logic Cells") ~ 2 Altera "Logic Elements"

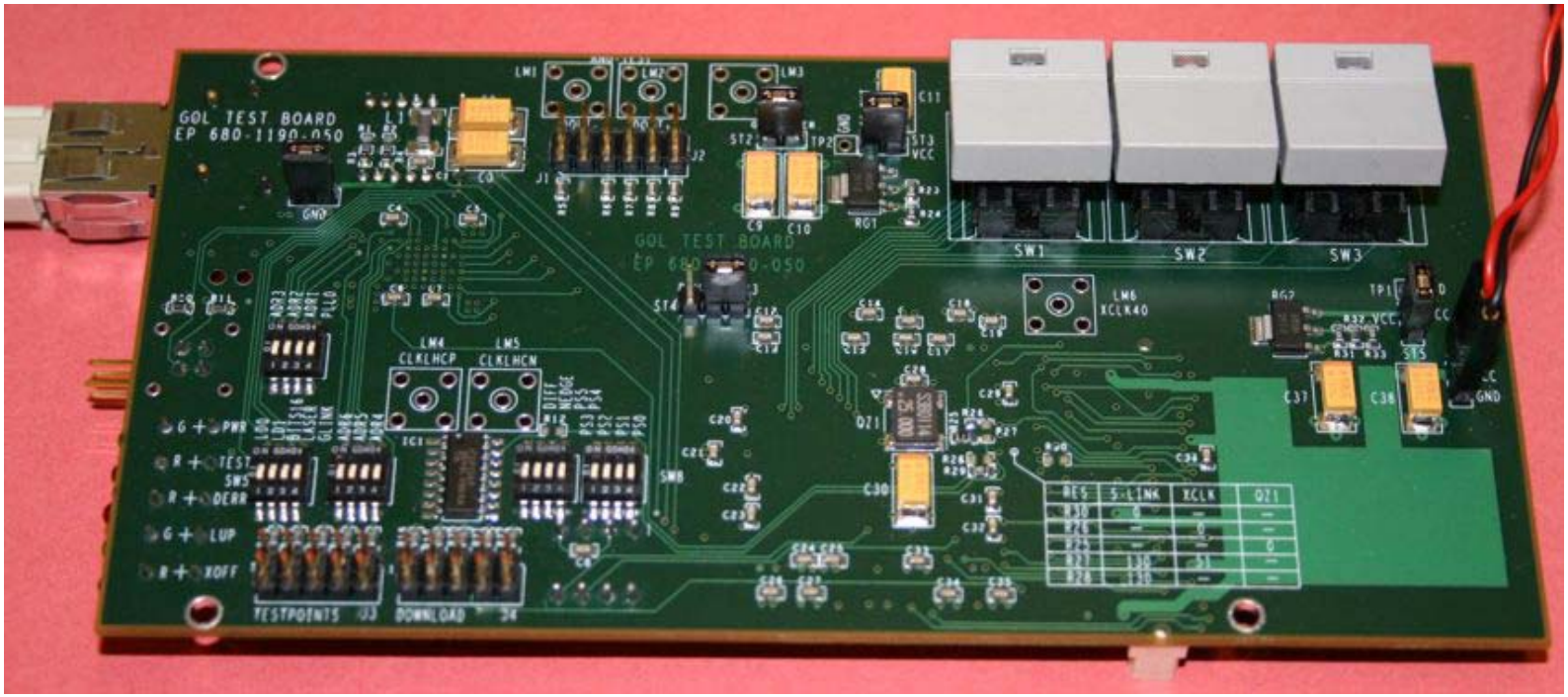
Virtex-II Pro Development Board



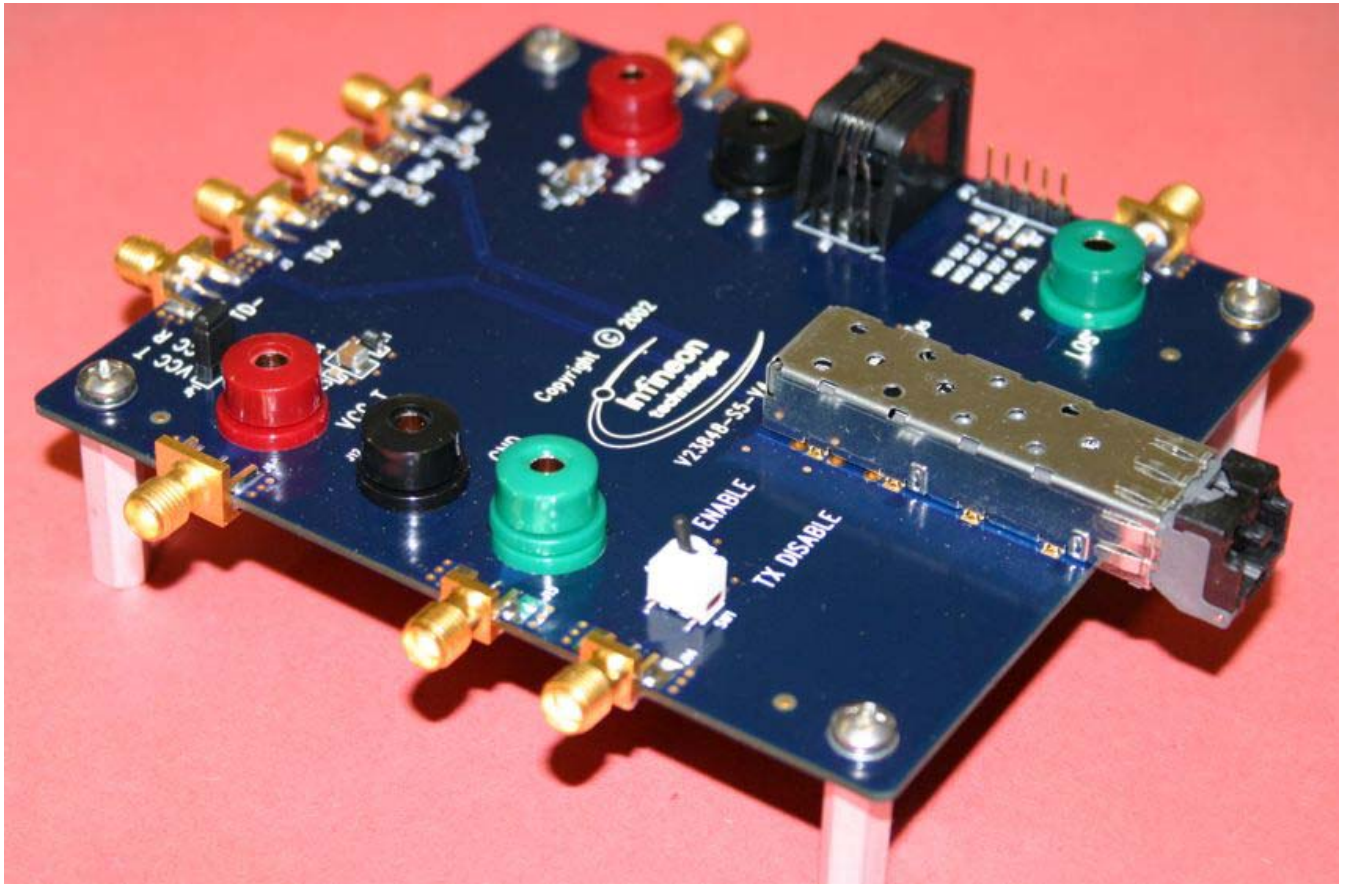
Virtex-II Pro Evaluation Kit



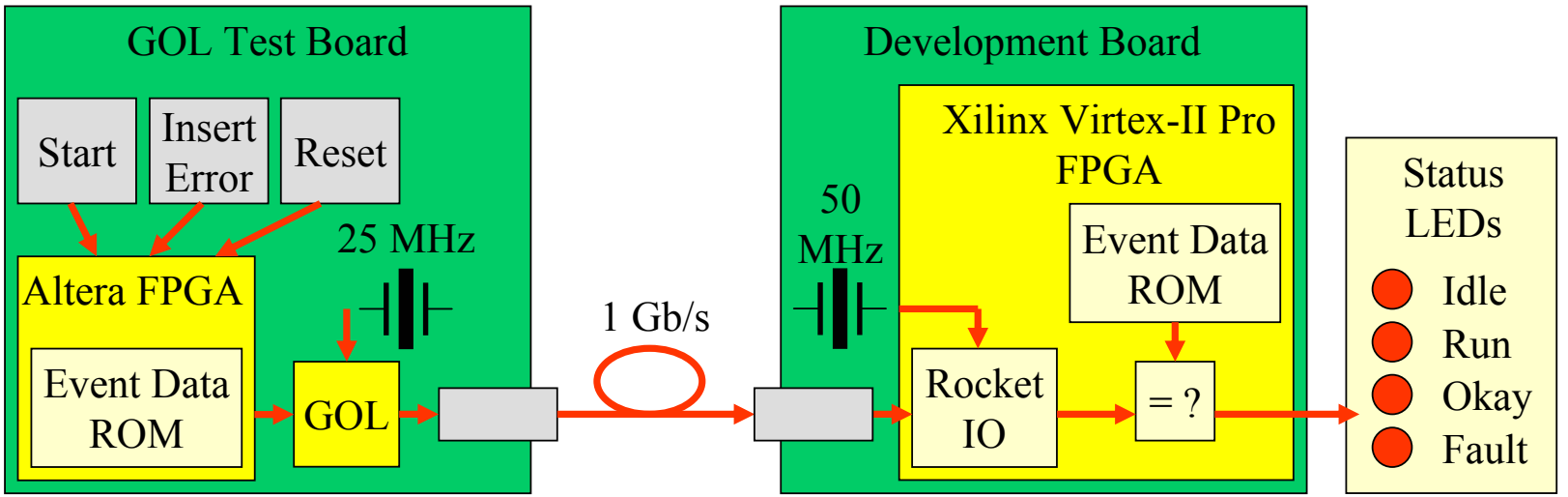
GOL Test Board

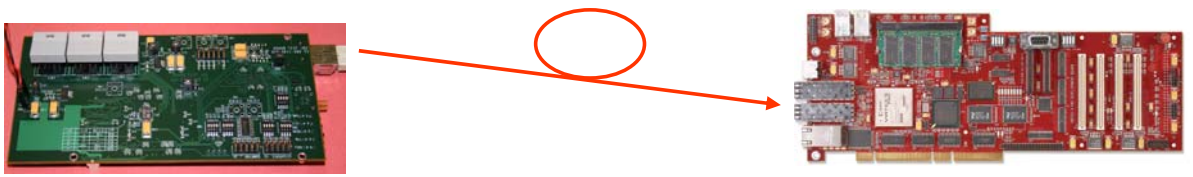


SFP Evaluation Kit

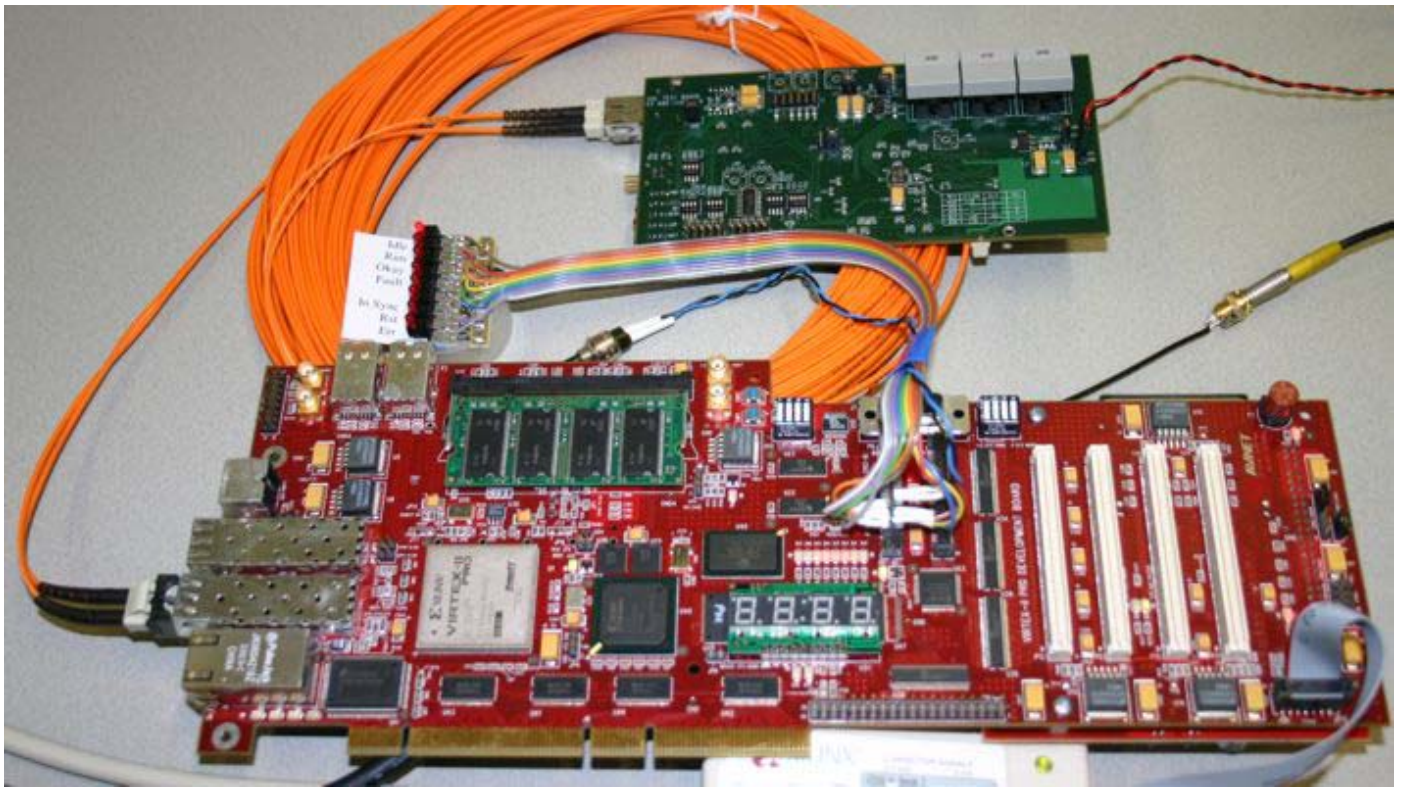


GOL to RocketIO test





GOL to RocketIO test



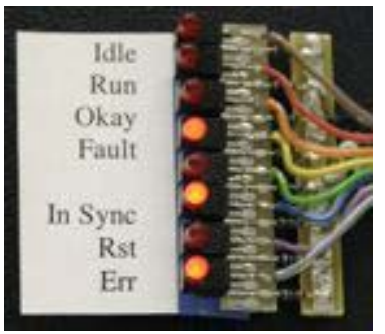
GOL to RocketIO test Results

- Xilinx ISE RocketIO placement problem -> Solved
- Back-annotated simulation (Smart-Models) of the setup -> Okay!

Reset

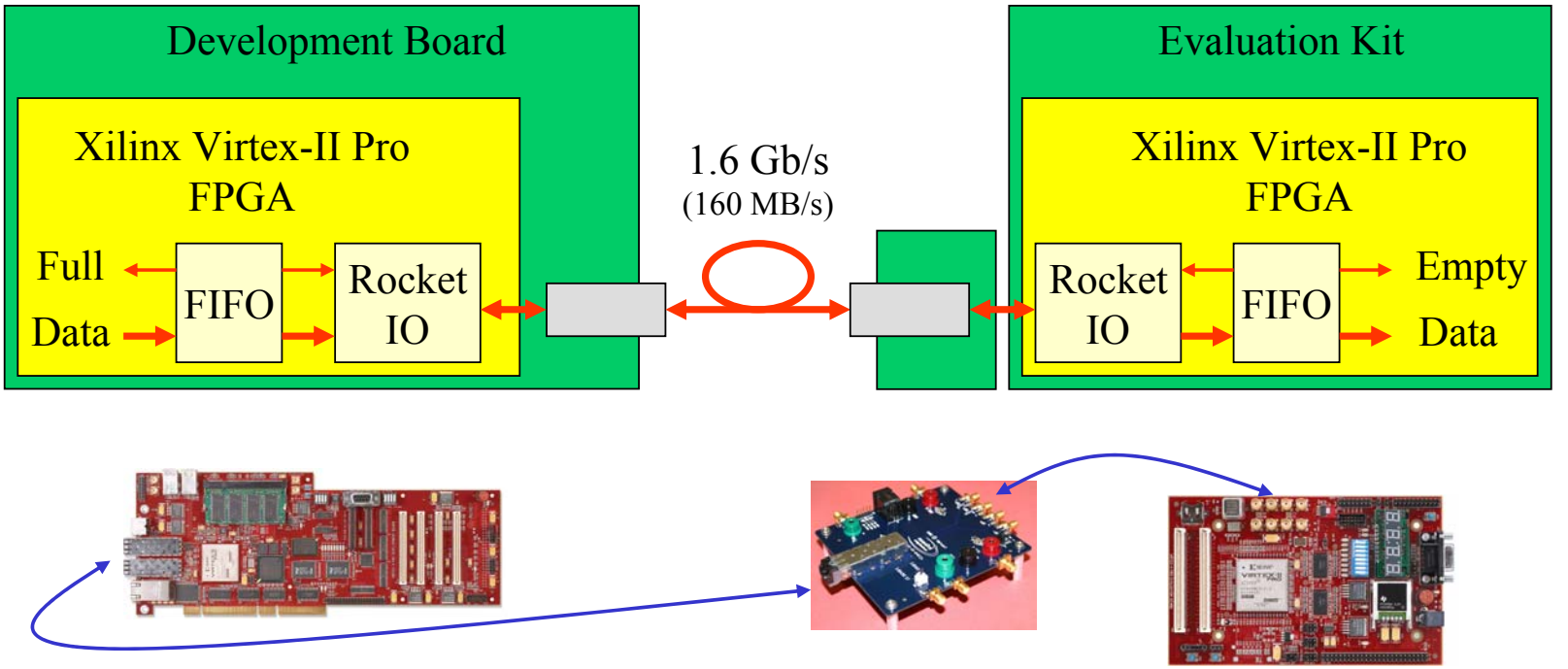
Start

Insert Error + Start



- Real life test -> Okay!

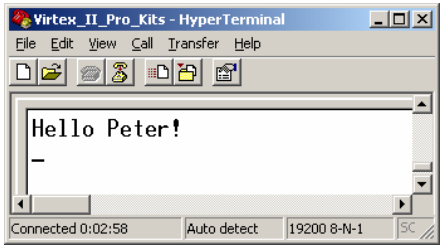
To Be Done:
Test FPGA to FPGA Data Links
Plus Flow Control



PowerPC core Evaluation

- Learn to use Xilinx Embedded Development Kit (EDK)
- Play with the demos that were delivered with the boards
- Made LED On/Off via RS232 system, using PowerPC core + Peripherals.

PowerPC Hello World System



- PPC-Core
- PLB Arbitter
- PLB BRAM Controller
- BRAM
- PLB 2 OPB Bridge
- OPB Arbitter
- Processor Reset
- UART-Lite
- JTAG PPC controller

Xilinx

XC2VP7FF869-6

- PPC405s
  - 1 out of 1 100%
- RAMB16s (2 KByte each)
  - 16 out of 44 36%
- Number of SLICEs
  - 826 out of 4928 16%

Conclusions:

- Design can easily be ported from Altera to Xilinx
- RocketIO
  - GOL Receiver is working.
  - Inter FPGA link to be tested.
- PowerPC
  - Consumes FPGA resources (probably need a XC2VP20 instead of a XC2VP7 device)
  - Needs investment in learning EDK
  - Needs investment in software development