SHORT HARDWARE DESCRIPTION
OF
THE 2TP_VME MODULE

ELECTRONIC DEPARTMENT
NIKHEF-H, AMSTERDAM

Version 2.0
SEPTEMBER 1990

Preface:

The 2TP_VME module is a general purpose VME master/slave module, that can be used in any standard VME bussystem. However, the J2 connector on the VME backplane is used for RS-422 input and output signals, so must be free.
The external connections are made either directly via one 32-pair cable on the J2 connector or via 5- and 7-pair cables on the LinkAdapter module at the J2 connector at the back of the VME crate.
The module provides arbiter functions and a VME SYSCLK for stand alone operations (the 2TP_VME module is the *only* master in the VME crate). However, when more VME masters are present in the crate, a VME arbiter module is necessary.

Versions:

The 2TP_VME module is delivered in the following versions:

Type A	-	VME Motherboard (MTHR-board) with 128 Kbyte trippleport memory plus two PiggyBack boards (PB-boards) with each 4 Mbyte of RAM.
Type AE	-	an extended version (280 mm depth) of version A.
Type B	-	like type A but with 16 Mbyte of RAM on one of the PiggyBack boards.
Type C	-	like type A but with 512 Kbyte of trippleport memory.
Type D	-	like type B but with 512 Kbyte of trippleport memory.
Type E	-	carrier board plus two PiggyBack boards with each 4 Mbyte of RAM.

Power requirements:

2TP_VME module : 5 Amp. max at +5 Volt
LinkAdapter module : 1 Amp. max at +5 Volt

Warranty and liability:

The 2TP_VME modules are warranted by INCAA Computers against defects in materials and workmanship for a period of twelve (12) months from date of shipment. This warranty is limited to servicing, adjusting or replacing any product returned to INCAA Computers with delivery charges prepaid.

The liability of INCAA Computers is strictly limited to the warranty activities as mentioned above. In no case shall the liability exceed the original purchase price.

Any questions with respect to this warranty or requests for repair should be directed to :

INCAA Computers,
Postbus 722,
7300 AS Apeldoorn,
Holland.
Tel: +31 55 425001 , Fax: +31 55 429000

1 Front panel LEDS and Push buttons of the 2TP-VME Module ……page 2
1.1 Explanation of the LEDs ……2
1.2 Front panel reset push buttons ……2

2 Switch and jumper position on the PB-board.……3
3 Switch and jumper settings on the PB-board ……4
3.1 Switch DIL_SW ……4
3.2 Jumper block J1.……7

4 Switch and jumper positions on the MTHR-board.……8
5 Switch and jumper settings on the MTHR-board ……9
5.1 Jumper blocks J_A17 and J_A18.……9
5.2 Hexadecimal switches SW_AHH, SW_AHL, SW_ALH and SW_ALL……10
5.3 Jumper block SLV1-3.……11
5.4 Jumper blocks BG1-6 and BR1-4 ……13
5.5 Jumper block JP_BRIN.……15
5.6 Jumper block JP_RLSE.……16
5.7 Jumper block JP_BGIN ……17
5.8 Jumper block JP_BERR ……18
5.9 Jumper block JP_CLK.……19
5.10 Jumper block JP_IACKOUT.……20
5.11 Jumper block JP_IRQ1-7.……21
5.12 Jumper blocks INTX and INTY ……22
5.13 Jumper block JP_RSTV ……23
5.14 Jumper blocks JP_ERRX and JP_ERRY.……24
5.15 Jumper block JP_PCO ……25

ELECTRONIC DEPARTMENT, NIKHEF-H, AMSTERDAM, SEPTEMBER 1990
S. GOBLE, G. KIEFT, A. DE WAARD

1.1 EXPLANATION OF THE LEDS:

LED:	ON:	OFF:
TX_EVENT	The Event input of transputer X is set by one of the event resources.	The Event input of transputer X is NOT set.
TY_EVENT	The Event input of transputer Y is set by one of the event resources.	The Event input of transputer Y is NOT set.
TX_LOCK	Transputer X has set its LOCK status bit. If transputer X now has access to the TPM then the TPM arbitration is locked to X. After the first access to the VME bus, the address strobe and address is kept active, resulting in either RMW or Block Transfers. If transputer X is Local Bus master then the release of the VME bus is disabled for as long as the lock bit is set.	The LOCK status bit of transputer X is NOT set.
TY_LOCK	Transputer Y has set its LOCK status bit. If transputer Y now has access to the TPM then the TPM arbitration is locked to Y. After the first access to the VME bus, the address strobe and address is kept active, resulting in either RMW or Block Transfers. If transputer Y is Local Bus master then the release of the VME bus is disabled for as long as the lock bit is set.	The LOCK status bit of transputer Y is NOT set.
TX-TPM	Transputer X is accessing the TPM.	Transputer X is NOT accessing the TPM.
TY-TPM	Transputer Y is accessing the TPM.	Transputer Y is NOT accessing the TPM.
VME-TPM	A VME master is accessing the TPM.	No access via VME to the TPM.
TY-LBUS	The direction of the LocalBus arbitration is to transputer Y.	The direction of the LocalBus arbitration is to transputer X.
VME_CYCL	The transputer, which is currently on the LocalBus (see TY-LBUS), is performing a cycle on the VME bus.	No VME cycles are being performed by the module.
PFM_FLAG	Either transputer X and/or transputer Y has set its PostFetchMode status bit.	The PostFetchMode status bit of transputer X and transputer Y is NOT set.
VME_MSTR	The module is the current VME busmaster.	The module is NOT the current VME busmaster.
RESET	The interface Asic Z_VME is reset by the SYSRESET line on VME or, if jumper JP_RSTV is connected, because of a reset on BOTH transputers at the same time.	The reset for the VME interface Asic Z_VME is NOT active.

1.2 FRONT PANEL RESET PUSH BUTTONS.

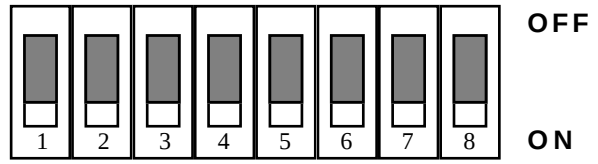
Push button RESET-X resets transputer X and its 'private' Z_LOC asic.
Push button RESET-Y resets transputer Y and its 'private' Z_LOC asic.
If BOTH push buttons are pressed at the SAME time then, if JP_RSTV is connected, the VME bus and the interface Asic Z_VME are reset.

3.1 Switch DIL_SW:

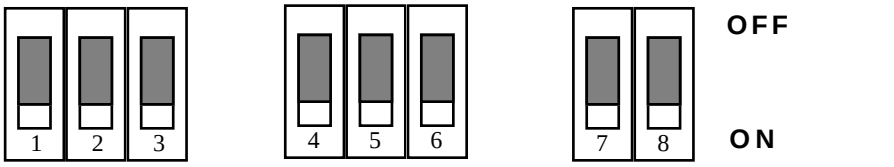
Link speed and clock speed setting of the transputer .

POSITION OF DIL_SW ON THE PB-BOARD:
See figure 1 showing the component layout of the PB-board.

LAYOUT SYMBOL:



SCHEME OF DIL_SW:



FOR SELECTION:

	LINK SPEED:			SWITCH SETTING:						
				SW-1	SW-2	SW-3		SW_1	SW_2	SW_3
A)	Link 0	5	Mbit/s							
	Link 1,2,3	5	Mbit/s	ON	OFF	OFF				
				SW-1	SW-2	SW-3				
B)	Link 0	5	Mbit/s							
	Link 1,2,3	10	Mbit/s	ON	OFF	ON				
				SW-1	SW-2	SW-3				
C)	Link 0	10	Mbit/s							
	Link 1,2,3	5	Mbit/s	ON	ON	OFF				
				SW-1	SW-2	SW-3	or	SW_1	SW_2	SW_3
D)	Link 0	10	Mbit/s							
	Link 1,2,3	10	Mbit/s	OFF	ON	ON		ON	ON	ON

				SW-1	SW-2	SW-3
E)	Link 0	10	Mbit/s			
	Link 1,2,3	20	Mbit/s	OFF	ON	OFF

				SW-1	SW-2	SW-3
F)	Link 0	20	Mbit/s			
	Link 1,2,3	10	Mbit/s	OFF	OFF	ON

				SW-1	SW-2	SW-3
G)	Link 0	20	Mbit/s			
	Link 1,2,3	20	Mbit/s	OFF	OFF	OFF

	CLOCK SPEED:			SWITCH SETTING:		
				SW-4	SW-5	SW-6
H)	Clock Speed	20	MHz	ON	ON	ON

				SW-4	SW-5	SW-6
I)	Clock Speed	17.5	MHz	ON	OFF	OFF

				SW-4	SW-5	SW-6
J)	Clock Speed	22.5	MHz	OFF	ON	ON

Note: The transputer T800 can operate at other clock speeds ,but in this design the maximum clockspeed is 20 Mhz.
DO NOT CHANGE SETTING OF THE CLOCK SPEED TO A VALUE HIGHER THAN 20 MHZ!

	BOOT FROM ROM / LINK:	SWITCH SETTING:
		SW-7
K)	Boot from LINK	ON

		SW-7
L)	Boot from ROM	OFF

Note: The transputer T800 can boot either from one of the links or from rom.
Within this design the transputer must always boot from one of the links.
DO NOT CHANGE SETTING OF THE BOOTFROMROM SWITCH!

DISABLE INTERNAL RAM:	SWITCH SETTING:
	SW-8
M) Enable Internal Ram ON	
	SW-8
N) Disable Internal Ram	OFF

DEFAULT SETTING OF DIL-SW:

	SW-1	SW-2	SW-3	SW-4	SW-5	SW-6	SW-7	SW-8
	OFF	OFF	OFF	ON	ON	ON	ON	ON

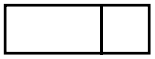
G) Link speed Link 0 20 Mbit/s
Link speed Link 1,2,3 20 Mbit/s
H) Clock speed 20 MHz
K) Boot from link
M) Enable internal ram

3.2 JUMPER BLOCK J1:

Connection of the Errorin pin of the transputer. The Errorin pin can be logically connected either to the ERRIN_P and ERRIN_N differential inputs on the P2 Link connector or , if not used , to ground.

POSITION OF J1 ON THE PB-BOARD:
See figure 1 showing the component layout of the PB-board.

LAYOUT SYMBOL:



J1

PIN 1

SCHEME OF J1:

```
3   2   1
o ═ o ═ o
```

FOR SELECTION:

	ERRORIN OPTION:	JUMPER SETTING:
A)	connected to ERRIN on link connector	3 2 1 o o ═ o
B)	connected to GND	3 2 1 o ═ o o

DEFAULT SETTING:

Option B connected to GND	3 2 1 o ═ o o

5.1 JUMPER BLOCKS J_A17 AND J_A18:

Selection whether address lines A17 and A18 are connected or not to the TripplePort Memory address decoding logic.
In case of a 128 KB TPM the address lines A17 and A18 must be connected.
In case of a 512 KB TPM the address lines A17 and A18 must NOT be connected.

POSITION OF J_A17 AND J_A18 ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:

SCHEME OF J_A17 AND J_A18:

1 2 3
o ═ o ═ o

FOR SELECTION:

OPTION:		JUMPER SETTING:
A)	Address line connected to decoding logic	1 2 3 o o ═ o
B)	Address line NOT connected to decoding logic	1 2 3 o ═ o o

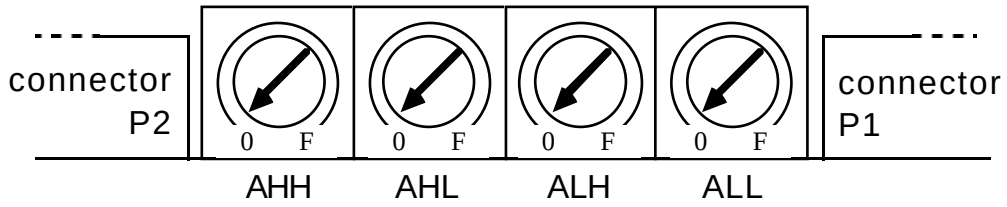
DEFAULT SETTING:
None. The setting of the jumpers depends on the size of the TripplePort Memory.
If the size of the TripplePort Memory is 128 KB then both J_A17 and J_A18 must connect pin 2 to pin 3.
If the size of the TripplePort Memory is 512 KB then both J_A17 and J_A18 must connect pin 1 to pin 2.

5.2 HEXADECIMAL SWITCHES SW_AHH, SW_AHL, SW_ALH, AND SW_ALL:

Selection of address of the TripplePort Memory as seen from the VME bus. Address bits A31-A17.

POSITION OF SW_AHH, SW_AHL, SW_ALH AND SW_ALL ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

FRONTVIEW OF THE SWITCHES:



FOR SELECTION:

Switch SW_AHH:	Address bits A31-A28	(hex 0xxx.xxxx - Fxxx.xxxx)		
Switch SW_AHL:	Address bits A27-A24	(hex x0xx.xxxx - xFxx.xxxx)		
Switch SW_ALH:	Address bits A23-A20	(hex xx0x.xxxx - xxFx.xxxx)		
Switch SW_ALL:	Address bits A19-A17	(hex xxx0.xxxx - xxxE.xxxx)	****	in case of 128 Kb TPM
Switch SW_ALL:	Address bit A19	(hex xxx0.xxxx - xxx8.xxxx)	****	in case of 512 Kb TPM

Total selectable higher address range: from hexadecimal address 0000.xxxx to FFFE.xxxx in case of 128 Kb TPM
Total selectable higher address range: from hexadecimal address 0000.xxxx to FFF8.xxxx in case of 512 Kb TPM

Notice:
Switch SW_ALL only switches 3 address bits A19-17 in case of a 128 KB TPM, since A16-01 are routed to the TripplePort Memory directly.
Switch SW_ALL only switches 1 address bit A19 in case of a 512 KB TPM, since A18-01 are routed to the TripplePort Memory directly.

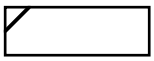
DEFAULT SETTING:
None. The setting of the switches depends on the location of the TripplePort Memory in the VME address map of your VME crate, with regard to your other VME slaves.

5.3 JUMPER BLOCK SLV1-3:

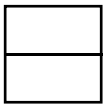
Selection of the AddressModify code(s) to which the TripplePort Memory will respond.
This selection also depend on the way Pal SLV_DEC at position IC 17 is programmed. Described is the selection with Pal SLV_DEC programmed according to the (default) Abelfile S_DEC_4.

POSITION OF SLV1-3 ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:



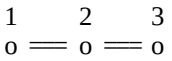
SLV3



SLV2
SLV1

SCHEME OF SLV1-2:

SCHEME OF SLV3:



FOR SELECTION:

	AM-OPTION:	JUMPER SETTING: SLV1	SLV2	SLV3
A)	Respond to: - Supervisory Program access - Supervisory Data access	1 2 o ═ o	1 2 o ═ o	1 2 3 o o ═ o
B)	Respond to: - Supervisory Data access	1 2 o o	1 2 o ═ o	1 2 3 o o ═ o
C)	Respond to: - Non-priviledged Program access - Non-priviledged Data access	1 2 o ═ o	1 2 o o	1 2 3 o o ═ o
D)	Respond to: - Non-privileged Data access	1 2 o o	1 2 o o	1 2 3 o o ═ o
E)	Respond to: - Supervisory Program access - Supervisory Data access - Non-priviledged Program access - Non-priviledged Data access	1 2 o ═ o	1 2 o ═ o	1 2 3 o ═ o o

		SLV1	SLV2	SLV3
F)	Respond to: - Supervisory Data access - Non-priviledged Data access	1 2 o o	1 2 o = o	1 2 3 o = o o
G)	No response Do not use!	1 2 o = o	1 2 o o	1 2 3 o = o o
H)	No response Do not use!	1 2 o o	1 2 o o	1 2 3 o = o o

DEFAULT SETTING:

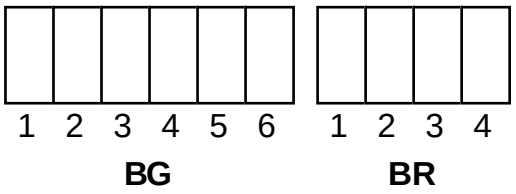
E)	Respond to: - Supervisory Program access - Supervisory Data access - Non-priviledged Program access - Non-priviledged Data access	1 2 o = o	1 2 o = o	1 2 3 o = o o

5.4 JUMPER BLOCKS BG1-6 AND BR1-4:

Selection of the VME bus request level which the 2TP-VME module will use to request the VME bus arbiter.

POSITION OF BG1-6 AND BR1-4 ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:



SCHEME OF BG1-6 AND BR1-4:

```
o   o   o   o   o   o  |  o   o   o   o
||  ||  ||  ||  ||  ||  |  ||  ||  ||  ||
o   o   o   o   o   o  |  o   o   o   o
1   2   3   4   5   6  |  1   2   3   4
```

BUS GRANT DAISY CHAIN BUS REQUEST LINE

FOR SELECTION:

BUS REQUEST LEVEL: JUMPER SETTING:

A) Bus request level 0

```
o ═ o   o   o   o   o  |  o   o   o   o
        ||  ||      ||  |  ||
o ═ o   o   o   o   o  |  o   o   o   o
1   2   3   4   5   6  |  1   2   3   4
```

B) Bus request level 1

```
o   o ═ o   o   o   o  |  o   o   o   o
||      |   ||      ||  |      ||
o   o ═ o   o   o   o  |  o   o   o   o
1   2   3   4   5   6  |  1   2   3   4
```

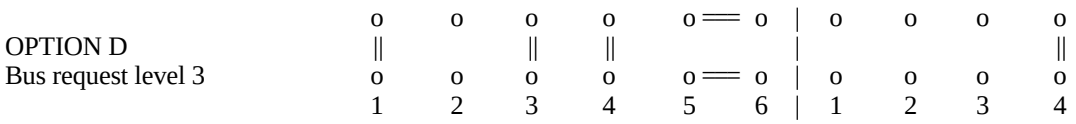
C) Bus request level 2

```
o   o   o   o ═ o   o  |  o   o   o   o
||      ||      ||  |          ||
o   o   o   o ═ o   o  |  o   o   o   o
1   2   3   4   5   6  |  1   2   3   4
```

D) Bus request level 3

```
o   o   o   o   o ═ o  |  o   o   o   o
||      ||  ||      |  |              ||
o   o   o   o   o ═ o  |  o   o   o   o
1   2   3   4   5   6  |  1   2   3   4
```

DEFAULT SETTING:

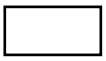


5.5 JUMPER BLOCK JP_BRIN:

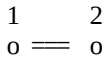
Selection of the fair request option for VME busmaster requests.
If fair request is enabled, then the module will NOT drive the selected VME BusRequest line (see jumper block BR1-4) if it sees that another VME module already drives the same Bus Request line.

POSITION OF JP_BRIN ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

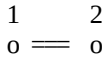
LAYOUT SYMBOL:



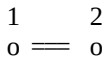
SCHEME OF JP_BRIN:



FOR SELECTION:

		JUMPER SETTING:
A)	Enable fair request option	
B)	Disable fair request option	

DEFAULT SETTING:

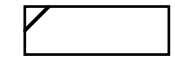
OPTION A Enable fair request option	

5.6 JUMPER BLOCK JP_RLSE:

Selection between ROR (release on request) and RWD (release when done) for the VME bus requester.
During ROR the VME bus is released if the module sees a Bus Request on one or more of the bus request lines.
During RWD the VME bus is released every time a cycle on the VME bus has started (release always).

POSITION OF JP_RLSE ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:



SCHEME OF JP_RLSE:

```
1   2   3
o ═ o ═ o
```

FOR SELECTION:

		JUMPER SETTING:
A)	Select ROR (release on request)	1 2 3 o o═ o
B)	Select RWD (release always)	1 2 3 o═ o o

DEFAULT SETTING:

OPTION A Select ROR (release on request)	1 2 3 o o═ o

5.7 JUMPER BLOCK JP_BGIN:

Connection of BusRequest send out by the module to BusGrantIn received by the module.
This is one of the jumpers necessary to let the module (or other slave modules) work if there is NOT a System Controller board in the VME crate. Only ONE 2TP_VME module and NO other masters may be used in the VME crate in this case!

POSITION OF JP_BGIN ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:

SCHEME OF JP_BGIN:

```
1   2   3
o ═ o ═ o
```

FOR SELECTION:

		JUMPER SETTING:
A)	NO connection of BR with BGIN	1 2 3 o o═ o
B)	Connect BR with BGIN	1 2 3 o═ o o

DEFAULT SETTING:

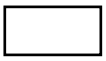
OPTION A NO connection of BR with BGIN	1 2 3 o o═ o

5.8 JUMPER BLOCK JP_BERR:

Selection whether to generate BERR via a watchdog timeout if one or both datastrobes on the VME bus stay (s) acitve longer then a certain time (default time is approximate 0.5 msec).
This is one of the jumpers necessary to let the module (or other slave modules) work if there is NOT a System Controller board in the VME crate.

POSITION OF JP_BERR ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:



SCHEME OF JP_BERR:

```
1   2
o ═ o
```

FOR SELECTION:

		JUMPER SETTING:
A)	Never generate BERR	1 2 o o
B)	Generate BERR after timeout	1 2 o ═ o

DEFAULT SETTING:

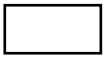
OPTION A Never generate BERR	1 2 o o

5.9 JUMPER BLOCK JP_CLK:

Selection whether to drive the SYSCLK line on the VME bus with a 16 Mhz clock.
This is one of the jumpers necessary to let the module (or other slave modules) work if there is NOT a System Controller board in the VME crate. Only ONE 2TP_VME module and NO other masters may be used in the VME crate in this case!

POSITION OF JP_CLK ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:



SCHEME OF JP_CLK:

```
1   2
o ═ o
```

FOR SELECTION:

		JUMPER SETTING:
A)	Never drive SYSCLK	1 2 o o
B)	Drive SYSCLK with 16 Mhz clock	1 2 o ═ o

DEFAULT SETTING:

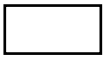
OPTION A Never drive SYSCLK	1 2 o o

5.10 JUMPER BLOCK JP_IACKOUT:

Selection whether to generate IACKOUT on the interrupt acknowledge out daisy chain line, if the 2TP_VME module is performing an interrupt acknowledge cycle on the VME bus.
This is one of the jumpers necessary to let the module (or other slave modules) work if there is NOT a System Controller board in the VME crate. Only ONE 2TP_VME module and NO other masters may be used in the VME crate in this case!

POSITION OF JP_IACKOUT ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:



SCHEME OF JP_IACKOUT:

```
1   2
o ═ o
```

FOR SELECTION:

		JUMPER SETTING:
A)	Never drive IACKOUT	1 2 o o
B)	Drive IACKOUT active during int. cycles	1 2 o ═ o

DEFAULT SETTING:

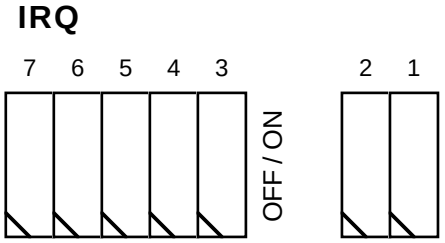
OPTION A Never drive IACKOUT	1 2 o o

5.11 JUMPER BLOCK JP_IRQ1-7:

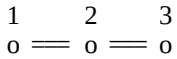
Selection of which interrupt request lines IRQ1 through IRQ7 to be handled by the module. An arbitrary selection between the seven interrupt request lines can be made. JP_IRQ1 is connected with the IRQ1 line on VME, etc.

POSITION OF JP_IRQ1-7 ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

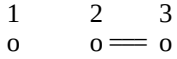
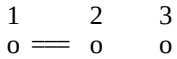
LAYOUT SYMBOL:



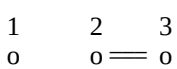
SCHEME OF JP_IRQ1-7:



FOR SELECTION:

		JUMPER SETTING:
A)	IRQ line is selected	
B)	IRQ line is NOT selected	

DEFAULT SETTING:

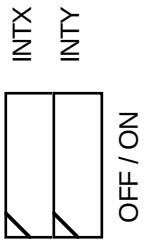
OPTION A All IRQ lines are selected	

5.12 JUMPER BLOCKS INTX AND INTY:

Selection between transputer X or transputer Y as VME interrupt handler of the interrupt lines as selected by JP_IRQ1-7. Only ONE transputer can be interrupt handler so INTX and INTY must NEVER connect the same two pin numbers!

POSITION OF INTX AND INTY ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:



SCHEME OF INTX AND INTY:

```
                1   2   3
                o ═ o ═ o      INTX

                o ═ o ═ o      INTY
```

FOR SELECTION:

JUMPER SETTING:

A) A VME interrupt request is routed to the EventReq pin of transputer X

```
                1   2   3
                o   o ═ o      INTX

                o ═ o   o      INTY
```

B) A VME interrupt request is routed to the EventReq pin of transputer Y

```
                1   2   3
                o ═ o   o      INTX

                o   o ═ o      INTY
```

DEFAULT SETTING:

OPTION B
A VME interrupt request is routed to the EventReq pin of transputer Y

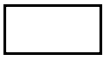
```
                1   2   3
                o ═ o   o      INTX

                o   o ═ o      INTY
```

5.13 JUMPER BLOCK JP_RSTV:

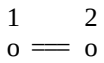
Enable or disable driving of the SYSRESET line on the VME bus by the module.
If enabled, the SYSRESET line is active if BOTH transputer X AND transputer Y are reset at the same time, either by the frontpanel switches Reset X and Reset Y, or by the differential RSTINX_P / RSTINX_N and RSTINY_P / RSTINY_N lines on the P2 LINK-connector.
NOTE: If the SYSRESET line is driven active by some other module on the VME bus, then always both transputer X and transputer Y will be reset as well as the Z_VME interface Asic on the module.

POSITION OF JP_RSTV ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

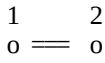
LAYOUT SYMBOL:



SCHEME OF JP_RSTV:



FOR SELECTION:

		JUMPER SETTING:
A)	Enable driving of the SYSRESET line	
B)	Disable driving of the SYSRESET line	

DEFAULT SETTING:

OPTION A Enable driving of the SYSRESET line	

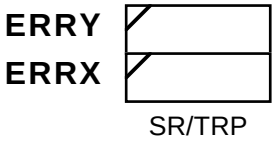
5.14 JUMPER BLOCKS JP_ERRX AND JP_ERRY:

Selection between - handling an external error via the EvntReq-pin and status register of transputer X or Y.
- handling an external error via the ErrorIn-pin of transputer X or Y.

An external error is an error coming from the ERRIN_P and ERRIN_N differential inputs on the P2 Link connector. ERRINX for transputer X and ERRINY for transputer Y.

POSITION OF JP_ERRX AND JP_ERRY ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:



SCHEME OF JP_ERRX AND JP_ERRY:

1 2 3
o ═ o ═ o

FOR SELECTION:

JUMPER SETTING:

A)
ERROR HANDLING VIA THE STATUS REGISTER AND EVNTREQ-PIN OF THE TRANSPUTER.
Errors from external devices, coming in on the P2 Link connector, are handled by the transputer via its status register and EventReq pin.

1 2 3
o ═ o o

B)
ERROR HANDLING VIA THE ERRORIN-PIN.
Errors from external devices, coming in on the P2 Link connector are handled by the transputer via its ErrorIn pin.
Note: When using the optional 2TP_VME_LA board, this option makes it possible to daisy-chain the ErrorIn and Error(Out) pins of several transputers in a network. More information about the daisy-chain, see hardware description of the 2TP_VME_LA board.

1 2 3
o o ═ o

DEFAULT SETTING:

OPTION A
Error handling via the status register and EvntReq-pin of the transputer.

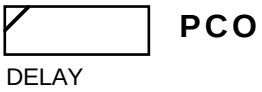
1 2 3
o ═ o o

5.15 JUMPER BLOCK JP_PCO:

The Asic Z_VME runs on the same clock as transputer Y. This jumper gives the option to delay the clock of Asic Z_VME in relation to the clock of transputer Y.

POSITION OF JP_PCO ON THE MTHR-BOARD:
See figure 2 showing the component layout of the MTHR-board.

LAYOUT SYMBOL:



SCHEME OF JP_PCO:

```
1   2   3
o ═ o ═ o
```

FOR SELECTION:

		JUMPER SETTING:
A)	NO delay of ZVMECLK	1 2 3 o o ═ o
B)	Delay ZVMECLK by app. 14 ns	1 2 3 o ═ o o

DEFAULT SETTING:

OPTION B Delay ZVMECLK	1 2 3 o ═ o o