CSB_GSLTB,
checking (internal) connections

Version 1.0

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1 Introduction

The base addresses of the boards in the **CSB_GSLTB** are as follows:

- first **ARE**-board at #7400
- second **ARE**-board at #7500
- first **LKBT2**-board at #7700
- second **LKBT2**-board at #7800, etc, etc
- eighth **LKBT2**-board at #7E00

First to eighth LKBT2 T222 are connected to the first ARE board connection 0 to 7 respectively.

First to eighth LKBT2 T222 are connected to LKS link 0 to link 7 respectively. First LKBT2 T222 is connected to *SLT component data* input 0 and 1, second LKBT2 T222 to *SLT component data* input 2 and 3, etc, etc.
Summarizing:

```
LKBT2 #0  <===> ARE #1 connection 0, LKS link 0, SLT 0 and 1
LKBT2 #1  <===> ARE #1 connection 1, LKS link 1, SLT 2 and 3
...
LKBT2 #7  <===> ARE #1 connection 7, LKS link 7, SLT 14 and 15
```

All Subtrigger transputers are connected to the second ARE board. First transputer of Subtrigger 0 is connected to ARE board connection 0, second transputer of Subtrigger 0 is connected ARE board connection 1, first transputer of Subtrigger 1 is connected to ARE board connection 2, second transputer of Subtrigger 1 is connected ARE board connection 3, first transputer of Subtrigger 2 is connected to ARE board connection 4, etc, etc.

Subtrigger modules have 2 transputers each. Links 0 to 3 of first Subtrigger transputer are connected to first to fourth LKBT2 board respectively. Links 0 to 3 of second Subtrigger transputer are connected to fifth to eighth LKBT2 board respectively.

Subtrigger 0 is connected to LKBT2 broadcast output 0, Subtrigger 1 to LKBT2 broadcast output 1, etc, etc.
Summarizing:

```
Subtrigger #0 Tx/Ty <===> ARE #2 connection 0/1
Subtrigger #1 Tx/Ty <===> ARE #2 connection 2/3
...                       ...
Subtrigger #7 Tx/Ty <===> ARE #2 connection 14/15

Subt #0 Tx link 0   <===> LKBT2 #0 broadcast 0
Subt #0 Tx link 1   <===> LKBT2 #1 broadcast 0
Subt #0 Tx link 2   <===> LKBT2 #2 broadcast 0
Subt #0 Tx link 3   <===> LKBT2 #3 broadcast 0
Subt #0 Ty link 0   <===> LKBT2 #4 broadcast 0
Subt #0 Ty link 1   <===> LKBT2 #5 broadcast 0
Subt #0 Ty link 2   <===> LKBT2 #6 broadcast 0
Subt #0 Ty link 3   <===> LKBT2 #7 broadcast 0
Subt #1 Tx link 0   <===> LKBT2 #0 broadcast 1
Subt #1 Tx link 1   <===> LKBT2 #1 broadcast 1
...                       ...
Subt #1 Ty link 3   <===> LKBT2 #7 broadcast 1
...                       ...
Subt #7 Tx link 0   <===> LKBT2 #0 broadcast 7
...                       ...
Subt #7 Ty link 3   <===> LKBT2 #7 broadcast 7
```

Testing all internal connections of the **CSB_GSLTB** is done in three steps:

1. testing of external 10-pins and 14-pins connections:
   - **TRP** connections; there is a separate small testprogram for each type of connection or signal:
     - ◇ **trpreset**: to test the ARI reset signal,
     - ◇ **trpana**: to test the ARI analyse signal,
     - ◇ **trplinkreset**: to test the reset signal via the links,
     - ◇ **trpevt**: to test the external event input/output (TRP-EVT),
     - ◇ **trperrorout**: to test the ARI error-out signal,
     - ◇ **trperrorin**: to test the ARI and ARO error-in signals.
   - **LKS** connections:
     - ◇ **lks**: to test LKS link connections.
   - **ARE** connections; there is a separate testprogram for each signal:
     - ◇ **arereset**: to test an ARE reset signal,
     - ◇ **areanalyse**: to test an ARE analyse signal,
     - ◇ **areerror**: to test an ARE error signal.
2. testing of the connections of the LKBT2 T222 transputer, except for its connection to the broadcast link of the LKBT2 board: see section 2.
3. testing of the connections to the Subtrigger 2TP-VME modules, including the broadcast capability of the LKBT2 T222 transputer: see section 3.

All tests have as a basic configuration a T800 host connected to the VAX and the TRP T222 connected to the T800 host. The T800 interacts with the user, reads in files containing program code with which LKBT2 T222 and Subtrigger T800 transputers are booted and displays messages received from the TRP T222 (which originate from the TRP T222 or the LKBT2 T222).

2 Test of LKBT2 T222 Connections

The connections of the TRP T222 should be (to be made by the user):

- 0 : T800 host transputer
- 1 : MSLK
- 2 : LKS30

The connections of the LKBT2 T222 should be (CSB internal):

- 0 : LKS
- 1 : SLT component
- 2 : SLT component
- 3 : MBLK
- + ARE

The testsequence performed on

- connection to **LKS**:
  1. LKBT2 T222 is reset by TRP T222 through the ARE #1 board
  2. TRP T222 connects LKS link 30 to the appropriate link on LKS associated with the LKBT2 T222 under test
  3. LKBT2 T222 is booted by TRP T222 via LKS with program **t2echo.btl**
  4. TRP T222 sends a linknumber via LKS to the LKBT2 T222
  5. TRP T222 sends a block of 256 INTs via LKS to LKBT2 T222
  6. LKBT2 T222 echos bytes sent to it across the link which number it previously received
  7. TRP T222 receives and checks the block of data
- connections to **SLT component**
  1. LKBT2 T222 is reset by TRP T222 through the ARE #1 board
  2. TRP T222 connects LKS link 30 to the appropriate link on LKS associated with the LKBT2 T222 under test
  3. LKBT2 T222 is booted by TRP T222 via LKS with program **t2lnktolnk.btl**
  4. TRP T222 sends two linknumbers via LKS to the LKBT2 T222
  5. LKBT2 T222 sends a small block of data out on each of the two links (which should be connected to one another, directly or via a transputer running a program that copies bytes from one link to another and viceversa) and receives a block of data on the same two links
  6. received datablocks are checked by the LKBT2 T222 and the result is sent to the TRP T222
- **ARE Analyse** signal
  1. LKBT2 T222 is reset and analyse asserted by TRP T222 through the ARE #1 board
  2. TRP T222 connects LKS link 30 to the appropriate link on LKS associated with the LKBT2 T222 under test

3. LKBT2 T222 is booted by TRP T222 via LKS with program **t2getana.btl**
4. LKBT2 T222 checks if analyse was asserted and reports this to TRP T222
5. test is repeated 5 times

- **ARE Error** signal

1. LKBT2 T222 is reset and analyse asserted by TRP T222 through the ARE #1 board
2. TRP T222 connects LKS link 30 to the appropriate link on LKS associated with the LKBT2 T222 under test
3. LKBT2 T222 is booted by TRP T222 via LKS with program **t2seterr.btl**
4. LKBT2 T222 sets its error flag
5. TRP T222 waits for an event and checks whether the correct interrupt flag and correct error flag in the ARE errorin-register is set
6. test is repeated 5 times

3 Test of Subtrigger Connections

Connections of the TRP T222 and LKBT2 T222 should be as mentioned in the previous section.
The testsequence performed on

- connections to **LKBT2** #0 to #7:

1. TRP T222 sets the broadcast select registers of the 8 LKBT2 boards to broadcast to only one Subtrigger module (interactively selected by the user)
2. LKBT2 T222 is reset by TRP T222 through the ARE #1 board
3. TRP T222 connects LKS link 30 to the appropriate link on LKS associated with the LKBT2 T222 to be used
4. LKBT2 T222 is booted by TRP T222 via LKS with program **t2broadc.btl**
5. TRP T222 resets appropriate Subtrigger transputer through the ARE #2 board, but only when first or fifth LKBT2 is used (LKBT2 #0: reset first transputer of Subtrigger module; LKBT2 #4: reset second transputer of Subtrigger module)
6. TRP T222 sends **t8receive.btl** program code and the number of the link along which the broadcast is to take place to LKBT2 T222
7. LKBT2 T222 boots Subtrigger transputer via LKBT2 MBLK link with program **t8receive.btl** and reports result to TRP T222
8. LKBT2 T222 sends a block of data to the booted Subtrigger transputer and reports the result to TRP T222
9. repeat steps 2 to 8 for each LKBT2 board

- **ARE Error** signal of first **Subtrigger** transputer:

1. TRP T222 sets the broadcast select registers of the first LKBT2 board to broadcast to only one Subtrigger module (interactively selected by the user)

2. first LKBT2's T222 is reset by TRP T222 through the ARE #1 board
3. TRP T222 connects LKS link 30 to the appropriate link on LKS associated with the first LKBT2 T222
4. LKBT2 #0 T222 is booted by TRP T222 via LKS with program **t2boot.btl**
5. TRP T222 resets first Subtrigger transputer through the ARE #2 board
6. TRP T222 sends **t8seterr.btl** program code and the number of the link along which the broadcast is to take place to LKBT2 T222
7. LKBT2 T222 boots Subtrigger transputer via LKBT2 MBLK link with program **t8seterr.btl** and reports result to TRP T222
8. Subtrigger transputer sets its error flag
9. TRP T222 waits for an event and checks whether the correct interrupt flag and correct error flag in the ARE errorin-register is set

- **ARE Error** signal of second **Subtrigger** transputer:

1. TRP T222 sets the broadcast select registers of the fifth LKBT2 board to broadcast to only one Subtrigger module (interactively selected by the user)
2. fifth LKBT2's T222 is reset by TRP T222 through the ARE #1 board
3. TRP T222 connects LKS link 30 to the appropriate link on LKS associated with the fifth LKBT2 T222
4. LKBT2 #4 T222 is booted by TRP T222 via LKS with program **t2boot.btl**
5. TRP T222 resets second Subtrigger transputer through the ARE #2 board
6. TRP T222 sends **t8seterr.btl** program code and the number of the link along which the broadcast is to take place to LKBT2 T222
7. LKBT2 T222 boots Subtrigger transputer via LKBT2 MBLK link with program **t8seterr.btl** and reports result to TRP T222
8. Subtrigger transputer sets its error flag
9. TRP T222 waits for an event and checks whether the correct interrupt flag and correct error flag in the ARE errorin-register is set