CSB_xCAL, checking (internal) connections

Version 1.1

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1 Introduction

The tests described in this document are not long-duration tests, but merely check quickly whether a connection is present and is functioning according to expectation. If the user wants to have complete control over each individual cycle in the CSB-crate performed by the TRP T222 he can use the peek-and-poke program **peekt2**.

The base addresses of the boards in the **CSB_xCAL** are as follows:

- **EVT**-boards at #7100, #7200 and #7300
- **ARE**-boards at #7400, #7500 and #7600
- **LKB**-board at #7700
- **LKC**-boards at #7E00 and #7F00

The following summarizes the connections of the Readout and Trigger transputers to the **CSB_FCAL** and **CSB_BCAL**:

```
Readout #0  <==> EVT/ARE #1 connection  0, LKC #1 link  0,
                 LKB broadcast  0, LKS #1 link  0 and  8,
Readout #1  <==> EVT/ARE #1 connection  1, LKC #1 link  1,
                 LKB broadcast  1, LKS #1 link  1 and  9,
Readout #2  <==> EVT/ARE #1 connection  2, LKC #1 link  2,
                 LKB broadcast  2, LKS #1 link  2 and 10,
...              ...                     ...
Readout #7  <==> EVT/ARE #1 connection  7, LKC #1 link  7,
                 LKB broadcast  7, LKS #1 link  7 and 15,
Readout #8  <==> EVT/ARE #1 connection  8, LKC #1 link  8,
                 LKB broadcast  8, LKS #2 link  0 and  8,
...              ...                     ...
Readout #15 <==> EVT/ARE #1 connection 15, LKC #1 link 15,
                 LKB broadcast 15, LKS #2 link  0 and 15,

Trigger #0  <==> EVT/ARE #2 conn  0, LKC #2 link  0, LKS #1 link 16,
Trigger #1  <==> EVT/ARE #2 conn  1, LKC #2 link  1, LKS #1 link 17,
...              ...                     ...             ...
Trigger #7  <==> EVT/ARE #2 conn  7, LKC #2 link  7, LKS #1 link 23,
Trigger #8  <==> EVT/ARE #2 conn  8, LKC #2 link  8, LKS #2 link 16,
...              ...                     ...             ...
Trigger #15 <==> EVT/ARE #2 conn 15, LKC #2 link 15, LKS #2 link 23,
```

Testing all internal connections of the **CSB_xCAL** is done in two steps:

1. testing the external 10-pins and 14-pins connections:
   - **TRP** connections; there is a separate small testprogram for each type of connection or signal:
     - ◇ **trpreset**: to test the ARI reset signal,
     - ◇ **trpana**: to test the ARI analyse signal,
     - ◇ **trplinkreset**: to test the reset signal via the links,
     - ◇ **trpevt**: to test the external event input/output (TRP-EVT),
     - ◇ **trperrorout**: to test the ARI error-out signal,
     - ◇ **trperrorin**: to test the ARI and ARO error-in signals.
     - ◇ **pmt2test**: to test the 64 KByte of TRP onboard private memory.
   - **EVT** connections:
     - ◇ **evt**: to test EVT in/outputs.
   - **ARE** connections; there is a separate testprogram for each signal:
     - ◇ **arereset**: to test an ARE reset signal,
     - ◇ **areanalyse**: to test an ARE analyse signal,
     - ◇ **areerror**: to test an ARE error signal.
   - **LKS** connections:
     - ◇ **lks**: to test LKS link connections.
2. testing the connections of the **Readout** and **Trigger** transputers: see section 2.

All tests have as a basic configuration a T800 host connected to the host-computer and the TRP T222 connected to the T800 host. The T800 interacts with the user, reads in files containing program code with which Readout and Trigger T800 transputers are booted (or with which a transputer is booted which is connected directly to the TRP T222, e.g. in tests **arereset**, **areanalyse**, **areerror**) and displays messages received from the TRP T222 (which originate from the TRP T222, Readout, Trigger or other connected transputer).

2 Test of Readout and Trigger Connections

The connections of the TRP T222 should be (to be made by the user):

- 0 : T800 host transputer
- 1 : MBLK
- 2 : MSLK
- 3 : LKS30

The connections of the Readout transputer should be (CSB internal):

- 0 : LKC
- 1 : LKB
- 2 : LKS (n+8)
- 3 : LKS (n)

- + ARE + EVT

The connections of the Trigger transputer should be:

- 0 : LKC (CSB internal)
- 1 : LKS (CSB internal)
- 2 : Trigger Layer 2 (externally to be connected to LKS #1 link 29 or LKS #2 link 29)
- + ARE + EVT

The testsequence performed on

- connection to **LKC**:
  1. Readout/Trigger is reset by TRP T222 through the ARE #1/#2 board
  2. Readout/Trigger is booted by TRP T222 via LKC #1/#2 with program **t8echo.btl**
  3. TRP T222 sends a linknumber via LKC to Readout/Trigger
  4. TRP T222 sends a block of 256 INTs via LKC to Readout/Trigger
  5. Readout/Trigger echos bytes sent to it across the link which number it previously received
  6. TRP T222 receives and checks the block of data
- connection to **LKS**:
  1. Readout/Trigger is reset by TRP T222 through the ARE #1/#2 board
  2. Readout/Trigger is booted by TRP T222 via LKC #1/#2 with program **t8echo.btl**
  3. TRP T222 connects LKS #1/#2 link 30 to the appropriate link on LKS #1/#2 associated with the Readout/Trigger under test
  4. TRP T222 sends a linknumber via LKC to Readout/Trigger
  5. TRP T222 sends a block of 256 INTs via LKS to Readout/Trigger
  6. Readout/Trigger echos bytes sent to it across the link which number it previously received
  7. TRP T222 receives and checks the block of data
- connection to **Trigger Layer 2**:
  1. Trigger is reset by TRP T222 through the ARE #2 board
  2. Trigger is booted by TRP T222 via LKC #2 with program **t8echo.btl**
  3. TRP T222 connects LKS #1/#2 link 30 to LKS #1/#2 link 29, the last being connected to Trigger Layer 2
  4. TRP T222 sends a linknumber via LKC to Trigger
  5. TRP T222 sends a block of 256 INTs via LKS to Trigger
  6. Trigger echos bytes sent to it across the link which number it previously received
  7. TRP T222 receives and checks the block of data
- connection to **LKB**:

1. Readout is reset by TRP T222 through the ARE #1 board
2. Readout is booted by TRP T222 via LKC #1 with program **t8getblock.btl**
3. TRP T222 sets the LKB broadcast select register to the Readout transputer selected by the user
4. TRP T222 sends the number of the link along which the broadcast is to be received via LKC to Readout
5. TRP T222 sends a block of data to Readout via the LKB MBLK link
6. Readout receives and checks the datablock and reports result to TRP T222 via LKC

- **ARE Analyse** signal
  1. Readout/Trigger is reset by TRP T222 through the ARE #1/#2 board
  2. Readout/Trigger is booted by TRP T222 via LKC #1/#2 with program **t8getana.btl**
  3. Readout/Trigger checks if analyse was asserted and reports this to TRP T222
  4. test is repeated 5 times
- **ARE Error** signal
  1. Readout/Trigger is reset by TRP T222 through the ARE #1/#2 board
  2. Readout/Trigger is booted by TRP T222 via LKC #1/#2 with program **t8seterr.btl**
  3. Readout/Trigger sets its error flag
  4. TRP T222 waits for an event and checks whether the correct interrupt flag and correct error flag in the ARE errorin-register is set
  5. test is repeated 5 times
- connection to **EVT**:
  1. Readout/Trigger is reset by TRP T222 through the ARE #1/#2 board
  2. Readout/Trigger is booted by TRP T222 via LKC #1/#2 with program **t8genevt.btl**
  3. TRP T222 generates an event-out to the booted Readout/Trigger through EVT #1/#2
  4. Readout/Trigger waits for the external event-in and then generates an external event-out
  5. TRP T222 waits for an event and checks whether the correct interrupt flag and correct event-in flag is set